Linear Circuits Data Book 1996

Power+™ Products, Peripheral Drivers/Actuators

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Printed in U.S.A. by
Custom Printing Company
Owensville, Missouri

INTRODUCTION

Texas Instruments offers an extensive line of the industy-standard integrated circuits designed to provide highly reliable circuits for switching inductive loads such as lamps, solenoids, motors, valves, and relays.

TI power devices represent technologies from the classic bipolar process to the Texas Instruments PRISM process, which offer improvements in power consumption and temperature stability.

This data book provides information on the following types of products:

- Power+ Arrays™ – integrated multiple, rugged power FETs in surface-mount packaging
- Power+ Logic™ – control logic integrated on same substrate with multiple power FETs
- Power+™ Control – integrated power ICs and pre-FET drivers to complement the Power+ Array family
- Peripheral drivers/actuators

TI continues to enhance quality and reliability of integrated circuits by improving materials, processes, test methods, and test equipment. Quality and performance are monitored throughout all phases of manufacturing; quality specifications and programs are continuously enhanced.

The Alphanumeric Index provides a method of quickly locating the correct device type. The Selection Guide includes a functional description of each device providing key parameter information and packaging types. Ordering Instructions and Mechanical Data are in the last section of this data book.

While this data book offers design and specification data for TI power integrated circuits, complete technical data for any TI semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by writing directly to:

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LITERATURE RESPONSE CENTER
P.O. Box 809066
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We believe the new 1996 Linear Circuits Data Book is a significant addition to your library of technical literature from Texas Instruments.

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Power+ Arrays™

DEVICE	DESCRIPTION	V_{DS} MAX (V)	I_{CONT} (A)	I_{PEAK} (A)	$r_{DS(on)}$ TYP (Ω)	t_{rr} TYP (ns)	Q_g TYP (nC)	PKG	PAGE
TPIC1301†	3-Half H-bridge	60	2.25	11.25	0.23	50	6.2	DW	2–3
TPIC1321L‡	3-Half H-bridge	60	1.25	4	0.35	45	4.6	DW	2–15
TPIC1501A§	H-Bridge & 3-phase bridge	20	3 & 1.5	12 & 6	0.1 & 0.4	70 & 60	5.6 & 1.6	DW	2–27
TPIC2202	2-Channel common-source	60	7.5	15	0.09	200	13.6	KC	2–51
TPIC2301	3-Channel common-source	60	7.5	15	0.09	200	13.6	KV	2–61
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TPIC2322L¶	3-Channel common-source	60	0.75	2.25	0.6	85	1.8	D	2–79
TPIC2701	7-Channel common-source	60	0.5	3	0.5	165	2.8	N	2–95
TPIC3302	3-Channel common-drain	60	1	5	0.4	35	3.1	D	2–105
TPIC3322L¶	3-Channel common-drain	60	0.75	2.25	0.6	30	1.8	D	2–115
TPIC5201	2-Channel independent	60	7.5	15	0.09	200	13.6	KV	2–125
TPIC5203†	2-Channel independent	60	1.6	8	0.26	50	4.7	D	2–133
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TPIC5302	3-Channel independent	60	1.4	7	0.3	35	8	D	2–153
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TPIC5621L¶	3-Phase bridge	60	1	3	0.4	65	3.1	DW	2–273

† Gate-protected
‡ Gate-protected and 5-V logic-level interface
§ Preliminary data only
¶ 5-V Logic-level interface

Power+ Logic™

DEVICE	DESCRIPTION	V_{DS} MAX (V)	I_{CONT} (mA)	I_{PEAK} (A)	$r_{DS(on)}$ TYP (Ω)	t_{PLH} TYP (ns)	INPUT COMP.	PKG	PAGE
TPIC6259	8-Bit addressable latch	45	250	1.5	1.3	625	CMOS	DW, N	2–283
TPIC6273	Octal D-type latch	45	250	1.5	1.3	625	CMOS	DW, N	2–293
TPIC6595	8-Bit shift register	45	250	1.5	1.3	650	CMOS	DW, N	2–301
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TPIC6E585¶	4-Bit shift register	40	§	1	1	650	CMOS	NE	2–391

† Short-circuit and current-limit protection
‡ Current-limit capability
§ User-programmable from 300 mA – 1 A
¶ Preliminary data only

Power+™ Control

DEVICE	DESCRIPTION	V_{bat} (V)	I_{bat} TYP (mA)	$f_{(osc)}$ (kHz)	I_{GD} MAX (mA)	t_r/t_f MAX (μs)	Fault Protection	PKG	PAGE
TPIC2101	Single-phase low-side pre-FET	8-16	4	20	50	1/0.8	Yes	D, N	2–33

DEVICE	DESCRIPTION	V_{bat} (V)	f TYP (MHz)	V_{DS} MAX (V)	I_D/I_{PEAK} (A)	$r_{DS(on)}$ TYP (Ω)	Diagnostics	PKG	PAGE
TPIC2603¶	6-Channel serial interface low-side	5.5 - 25	4	70	0.35/2.25	1.7	Yes	DW, NE	2–89

¶ Preliminary data only

general-purpose drivers and actuators

SWITCHING VOLTAGE MAX (V)	OFF-STATE VOLTAGE MAX (V)	PEAK OUTPUT CURRENT (mA)	DRIVERS PER PKG	OUTPUT CLAMP DIODES	INPUT COMP.	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
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						NOR	27	SN55454B	FK, JG	3–15
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						OR		SN75478		3–87
60	60	100	4	Yes	TTL, CMOS	Telecom Relay Driver	1000	DS3680	D, N	3–3

motor drivers and power actuators

SWITCHING VOLTAGE MAX (V)	OFF-STATE VOLTAGE MAX (V)	PEAK OUTPUT CURRENT (mA)	DRIVERS PER PKG	OUTPUT CLAMP DIODES	INPUT COMP.	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
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		2000		No				L293		3–7
				Yes	TTL, CMOS			SN754410		3–61

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and the buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

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ULN2004	TPIC2701	2–95

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FAIRCHILD	SUGGESTED TI REPLACEMENT	PAGE NO.
μA75451	SN75451B	3–15
μA75452	SN75452B	3–15
μA75453	SN75453B	3–15
μA75454	SN75454B	3–15
μA75461	SN75461	3–23
μA75462	SN75462	3–23
MC1412	ULN2002A	3–93
MC1413	ULN2003A	3–93
μA3680	DS3680	3–3
μA9665	ULN2001A	3–93
μA9666	ULN2002A	3–93
μA9667	ULN2003A	3–93
μA9668	ULN2004A	3–93
μA75471	SN75471	3–81
μA75472	SN75472	3–82
μA75473	SN75473	3–81

MOTOROLA	SUGGESTED TI REPLACEMENT	PAGE NO.
MC1411	ULN2001A	3–93
MC1412	ULN2002A	3–93
MC1413	ULN2003A	3–93
MC1413T	SN75468	3–73
MC1416	ULN2004A	3–93
MC1471	SN75476	3–87
MC1473	SN75478	3–87
SN75451B	SN75451B	3–15
SN75452B	SN75452B	3–15
SN75453B	SN75453B	3–15
SN75454B	SN75454B	3–15
ULN2001	ULN2001A	3–93
ULN2002	ULN2002A	3–93
ULN2003	ULN2003A	3–93
ULN2004	ULN2004A	3–93

NATIONAL	SUGGESTED TI REPLACEMENT	PAGE NO.
DS3611	SN75471	3–81
DS3612	SN75472	3–81
DS3613	SN75473	3–81
DS3658	SN75437A	3–51
DS3680	DS3680	3–3
DS75361	SN75372	3–29
DS75365	SN75374	3–29
DS75451	SN75451B	3–15
DS75452	SN75452B	3–15

NATIONAL	SUGGESTED TI REPLACEMENT	PAGE NO.
DS75453	SN75453B	3–15
DS75454	SN75454B	3–15
DS75461	SN75461	3–23
DS75462	SN75462	3–23
DS75463	SN75463	3–23
LM3611	SN75471	3–81
LM3612	SN75472	3–81
LM3613	SN75473	3–81
LM75453	SN75453B	3–15

RIFA	SUGGESTED TI REPLACEMENT	PAGE NO.
PBD352301	ULN2001A	3–93
PBD352302	ULN2004A	3–93
PBD352303	ULN2003A	3–93
PBD352304	ULN2002A	3–93
PBD352312	SN75469	3–73
PBD352313	SN75468	3–73

SGS-ATES	SUGGESTED TI REPLACEMENT	PAGE NO.
L201	ULN2001A	3–93
L202	ULN2002A	3–93
L203	ULN2003A	3–93
L204	ULN2004A	3–93
L293	L293	3–7
L293D	L293D	3–11
	SN754410	3–61
ULN2001	ULN2001A	3–93
ULN2002	ULN2002A	3–93
ULN2003	ULN2003A	3–93
ULN2004	ULN2004A	3–93

SILICON GENERAL	SUGGESTED TI REPLACEMENT	PAGE NO.
SG2001	ULN2001A	3–93
SG2002	ULN2002A	3–93
SG2003	ULN2003A	3–93
SG2004	ULN2004A	3–93
SG2023	SN75468	3–73
SG2024	SN75469	3–73
SG75451	SN75451B	3–15
SG75452	SN75452B	3–15
SG75453	SN75453B	3–15

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SILICON GENERAL	SUGGESTED TI REPLACEMENT	PAGE NO.
SG75454	SN75454B	3–15
SG75461	SN75461	3–23
SG75462	SN75462	3–23
SG75463	SN75463	3–23
SG75473	SN75473	3–81

SPRAGUE	SUGGESTED TI REPLACEMENT	PAGE NO.
UDN–2541	SN75437A	3–51
UDN–3611	SN75471	3–81
UDN–3612	SN75472	3–81
UDN–3613	SN75473	3–81
UDN–5711	SN75476	3–87
UDN–5713	SN75478	3–87
UDN–5722	SN75477	3–87
ULN–2001	ULN2001A	3–93
ULN–2002	ULN2002A	3–93
ULN–2003	ULN2003A	3–93
ULN–2004	ULN2004A	3–93
ULN–2023	SN75468	3–73
ULN–2024	SN75469	3–73

UNITRODE	SUGGESTED TI REPLACEMENT	PAGE NO.
L293	L293	3–7
L293D	L293D	3–11
	SN754410	3–61

C_{gd} **Gate-Drain Capacitance**
Capacitance measured between the gate and drain with V_{GS} = 0 V ($C_{gd} = C_{rss}$)

C_{ds} **Drain-Source Capacitance**
Capacitance measured between the drain and source with V_{GS} = 0 V ($C_{gs} = C_{iss} - C_{rss}$)

C_{gs} **Gate-Source Capacitance**
Capacitance measured between the gate and source with V_{GS} = 0 V ($C_{ds} = C_{oss} - C_{rss}$)

C_{iss} **Short-Circuit Input Capacitance**
Input capacitance with drain and source shorted ($C_{iss} = C_{gd} + C_{gs}$, C_{ds} shorted)

C_{oss} **Short-Circuit Output Capacitance**
Total capacitance between drain and source with gate and source shorted ($C_{oss} = C_{ds} + C_{gd}$, C_{gs} shorted)

C_{rss} **Short-Circuit Reverse Transfer Capacitance**
Gate-drain capacitance with V_{GS} = 0 ($C_{rss} = C_{gd}$)

E_{AS} **Single-Pulse Avalanche Energy**
Maximum energy dissipation allowed during avalanche breakdown for a single pulse of avalanche current

g_{fs} **Common-Source Small-Signal Transconductance**
Ratio of change in drain current due to a change in gate-to-source voltage

I_{AS} **Peak Avalanche Current**
Maximum allowable current during avalanche breakdown

I_{CC} **Power Supply Current**
Total current from the V_{CC} supply

I_D **DC Drain Current**
Measured dc current into the drain

I_{DM} **Peak-Drain Current, Single Output**
Maximum allowable value of drain current

I_{DSS} **Zero-Gate-Voltage Drain Current**
Current into drain when gate-to-source voltage is zero

I_{DSX} **Off-State Drain Current**
See Zero-Gate-Voltage Drain Current (I_{DSS})

I_F **Clamp Diode Forward Current**
Measurement of current through the clamp diode

I_{GSSF} **Forward Gate Current, Drain-to-Source Short Circuited**
Direct current into gate with forward gate-to-source voltage and drain shorted to source

I_{GSSR}	**Reverse Gate Current, Drain-to-Source Short Circuited** Direct current into gate with reverse gate-to-source voltage and drain shorted to source
I_I	**Input Current** Direct current to the gate
I_{IH}	**High-Level Input Current** Current the device uses to switch state from low to high
I_{IL}	**Low-Level Input Current** Current the device uses to switch state from high to low
I_O	**Continuous Output Current** Direct output current across the drain-to-source junction
$I_{O(chp)}$	**Output Chopping Current** Value at which output current changes from continuous current to low duty cycle pulsed current
I_{OM}	**Maximum Output Current** Maximum output current in the on state
I_R	**Reverse Current** Current flow across reverse-biased junction at specified applied voltage
I_{SD}	**Source-Drain Diode Current** Maximum continuous forward diode current
P_D	**Maximum Off-State Power Dissipation** Amount of power consumed by the die such that maximum junction temperature is not exceeded at held case temperature
Q_g	**Total Gate Charge** Maximum charge drawn by gate at a specified V_{GS}
Q_{gd}	**Gate-Drain Charge** Charge between the gate and drain of the device
Q_{gs}	**Gate-Source Charge** Charge between the gate and source of the device
$r_{DS(on)}$	**Static Drain-Source On-State Resistance** Resistance between the drain and source during on state
r_i	**Input Resistance** Resistance between gate and source
$R_{\theta JA}$	**Junction-to-Ambient Thermal Resistance** Thermal resistance (steady state) from the device case to the ambient (air)

$R_{\theta JC}$ **Junction-to-Case Thermal Resistance**
Thermal resistance (steady state) from the device junction to case

r_o **Output Resistance**
Resistance between drain and source

t_a **Reverse-Recovery-Current Rise Time**
Elapsed time for diode current to reach maximum value during reverse recovery

T_A **Ambient Operating Temperature (Free Air)**
Air temperature measured below a device in an environment cooled only by natural air convention

t_c **Cycle Time**
Time interval between the start and end of a cycle

T_C **Case Operating Temperature**
Temperature measured at a specific location on the case of a device

$t_{d(off)}$ **Turn-Off Delay Time**
Time interval during which an input pulse falls from 90% of its peak value to 10% of its off-state amplitude

$t_{d(on)}$ **Turn-On Delay Time**
Time interval during which an input pulse rises from 10% of its peak value to 90% of its off-state amplitude

t_f **Fall Time**
Time interval for signal to change from 90% to 10% of its peak value

t_h **Hold Time**
Time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

T_J **Virtual Junction Temperature**
Calculated value of the silicon junction(s) temperature based on the thermal and electrical behavior of the device

t_{off} **Turn-Off Time**
Time interval between gate turn off and drain-to-source shutdown

t_{on} **Turn-On Time**
Time interval between gate turn on and drain-to-source turn on

t_{PHL} **Propagation Delay Time, High-to-Low Level Output**
Time interval for drain-to-source signal to fall from 90% to 10% of its peak value

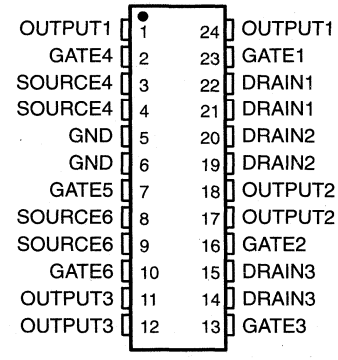
t_{PLH} **Propagation Delay Time, Low-to-High Level Output**
Time interval for drain-to-source signal to rise from 10% to 90% of its peak value

t_r	**Rise Time** Time interval for signal to rise from 10% to 90% of its peak value
t_{rr}	**Reverse-Recovery Time** Time required to remove excess carriers from a diode after reverse of carrier flow
t_{su}	**Setup Time** Time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal
t_v	**Valid Time** Delay time from 50% rising edge of serial clock input to 10% change in serial output
t_w	**Pulse Duration** Active pulse time measured at 50% of steady-state amplitude from leading edge to trailing edge of the same pulse
$V_{(BR)}$	**Breakdown Voltage** Drain-to-source voltage at which device avalanche multiplication occurs
V_{DS}	**Drain-Source Voltage** Voltage measured across the drain to source
V_{GS}	**Gate-Source Voltage** Measurement of the input voltage in reference to the source
V_I	**Input Voltage** Voltage measured from gate to source
V_{IH}	**High-Level Input Voltage** Voltage on gate that initiates drain-to-source turn on
V_{IL}	**Low-Level Input Voltage** Voltage on gate that initiates drain-to-source turn off
V_{OH}	**High-Level Output Voltage** Voltage measured on the source-to-drain in high state
V_{OK}	**Output Clamp Voltage** Voltage measured on the source to clamp input
V_{OL}	**Low-Level Output Voltage** Voltage measured on the drain-to-source in low state
V_{SD}	**Forward On-Voltage** Voltage measured on the source-to-drain in the forward direction
$V_{SD(ov)}$	**Overvoltage Shutdown Voltage** Specified temperature at which overvoltage shutdown circuit is activated
V_{TGS}	**Gate-Source Threshold Voltage** Gate voltage required to produce a specified amount of drain curren

2 Power+™ Products

- **Low $r_{DS(on)}$ . . . 0.23 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 11.25 A Per Channel**
- **Fast Commutation Speed**

DW PACKAGE
(TOP VIEW)

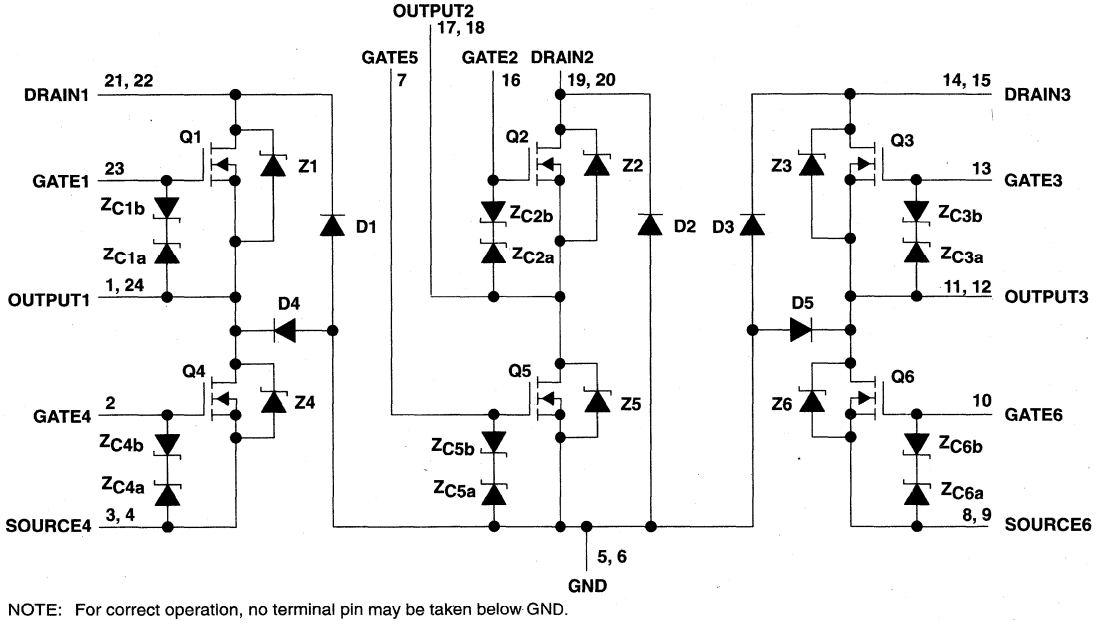


description

The TPIC1301 is a monolithic gate-protected power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as three half H-bridges. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC1301 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-GND voltage, V_{DG}	100 V
Drain-to-source voltage, V_{DS}	60 V
Output-to-GND voltage	60 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	2.25 A
Continuous source-to-drain diode current, T_C = 25°C	2.25 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	11.25 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pule avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	17.2 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1–D5)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2.25 A, See Notes 2 and 3	V_{GS} = 10 V,		0.52	0.62	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2.25 A, V_{GS} = 0 (Z1–Z6), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2.25 A (D1–D5) See Notes 2 and 3			5		V
I_{DSS}	Drain current-gate shorted to source	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V,	V_{DS} = 0		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND Gate shorted to source	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2.25 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.23	0.275	Ω
			T_C = 125°C		0.35	0.4	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 1.125 A,	1.6	2.21		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		200	250	pF
C_{oss}	Short-circuit output capacitance, common source				175	220	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1.125 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, and Z3		50		ns
Q_{RR}	Total diode charge					65		nC

resistive-load switching characteristics, T_C = 25°C

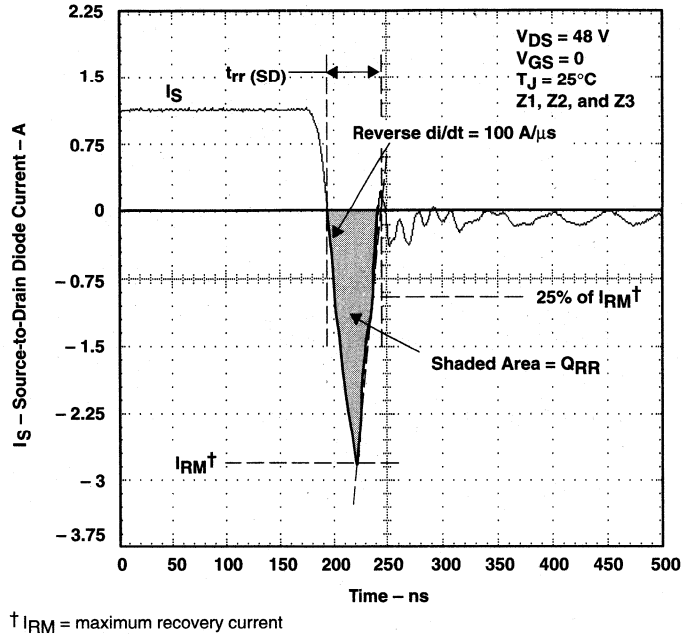
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 20 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			25	50	
t_r	Rise time			15	30	
t_f	Fall time			7	15	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1.125 A, V_{GS} = 10 V, See Figure 3		6.2	7.4	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.7	0.8	
Q_{gd}	Gate-to-drain charge			2.4	2.9	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		45		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		°C/W

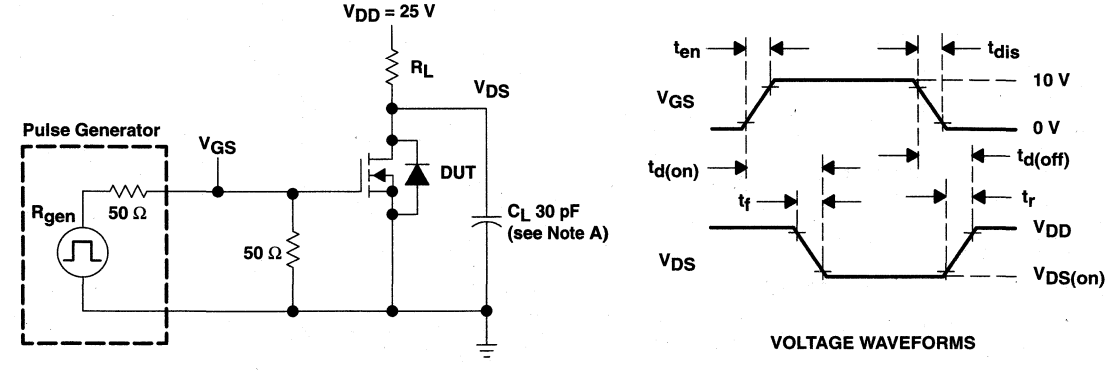
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

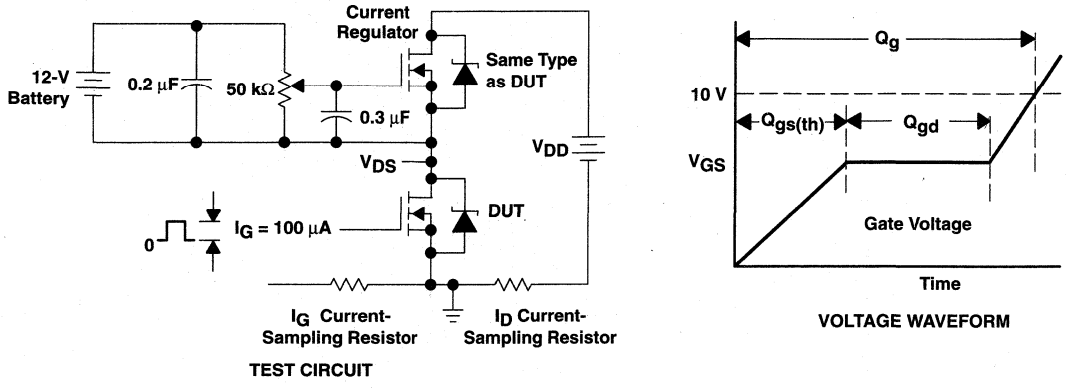
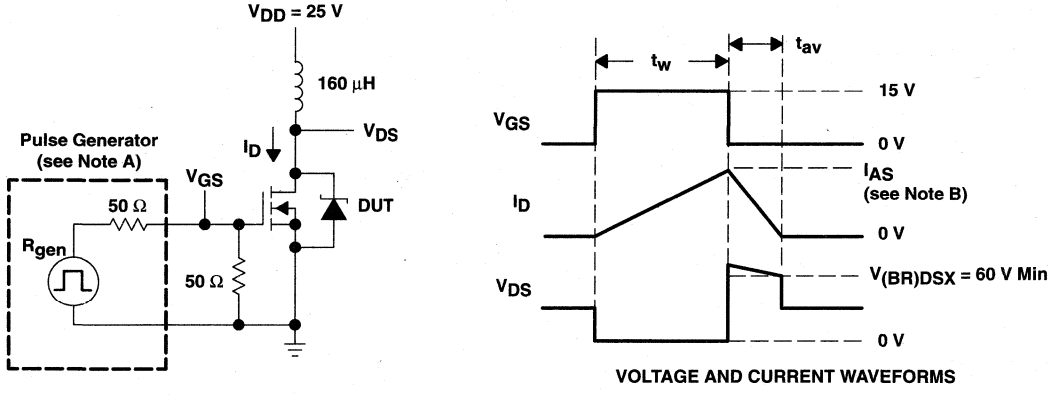


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 11.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 17.2$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

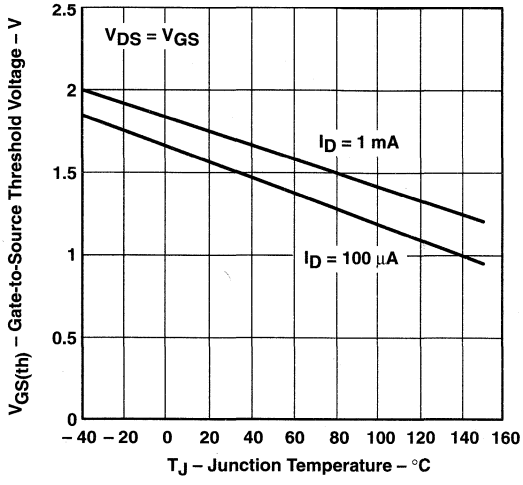


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

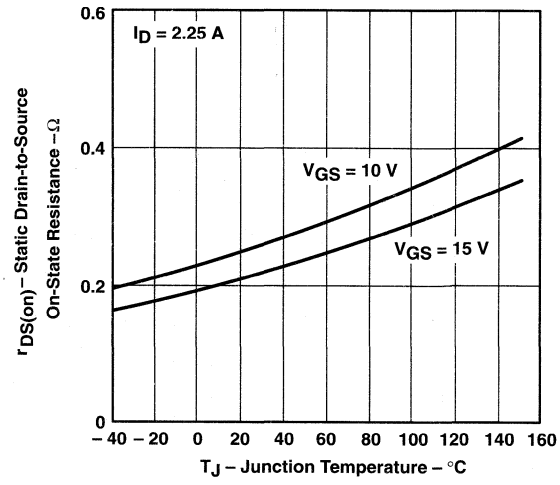


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

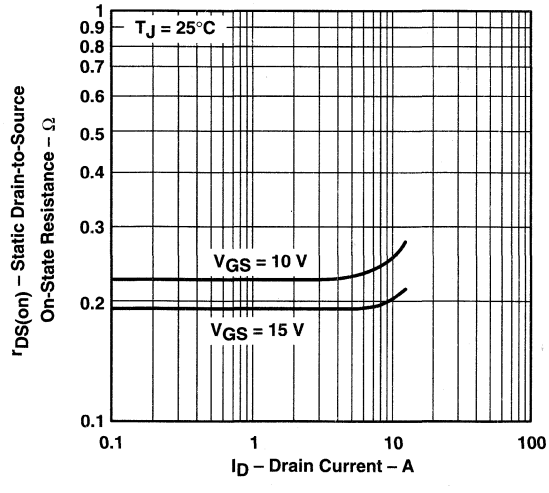


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

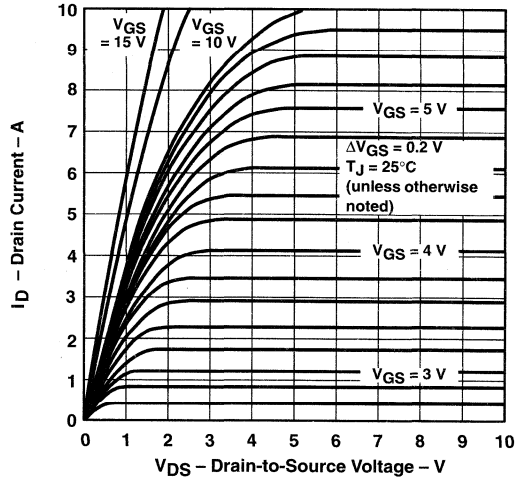


Figure 8

TYPICAL CHARACTERISTICS

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

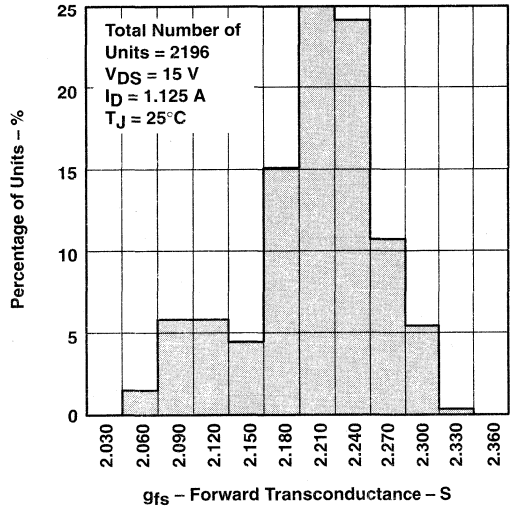


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

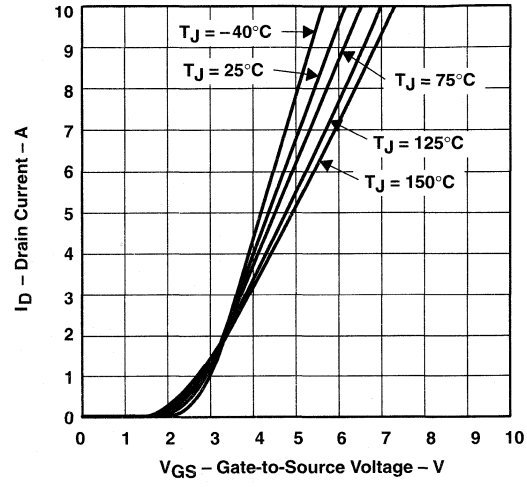


Figure 10

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

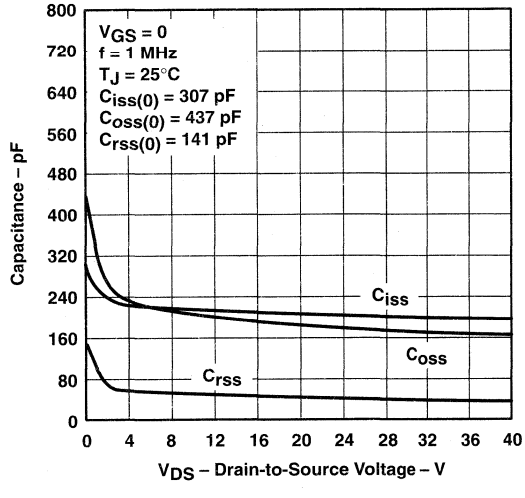


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

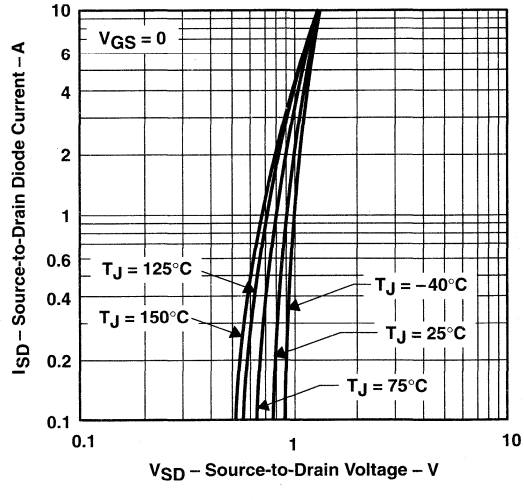


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

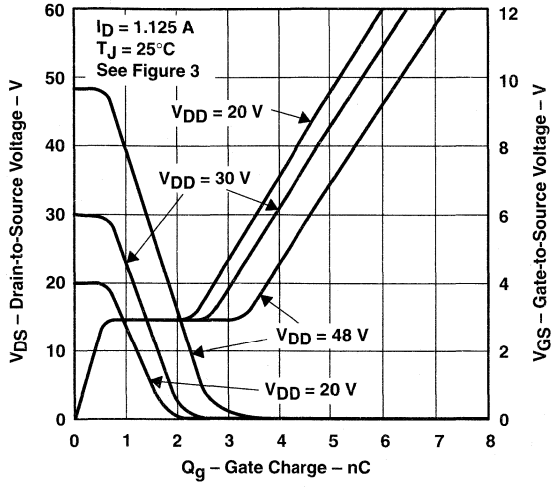


Figure 13

REVERSE RECOVERY TIME
vs
REVERSE di/dt

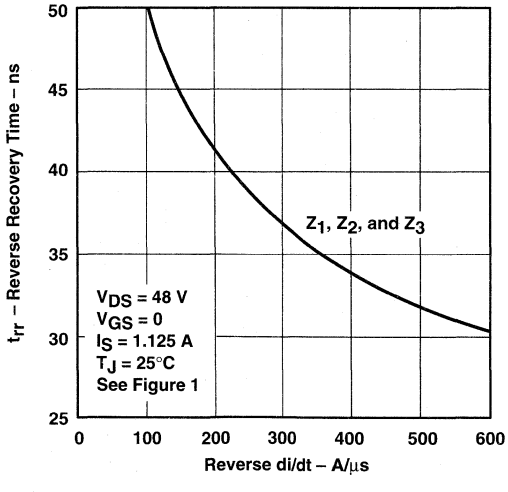
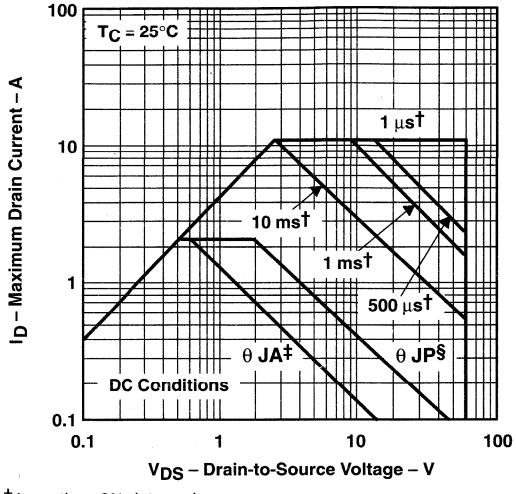


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
§ Device mounted in intimate contact with infinite heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

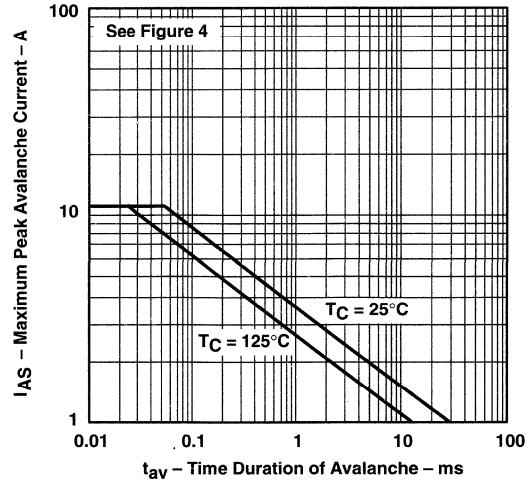
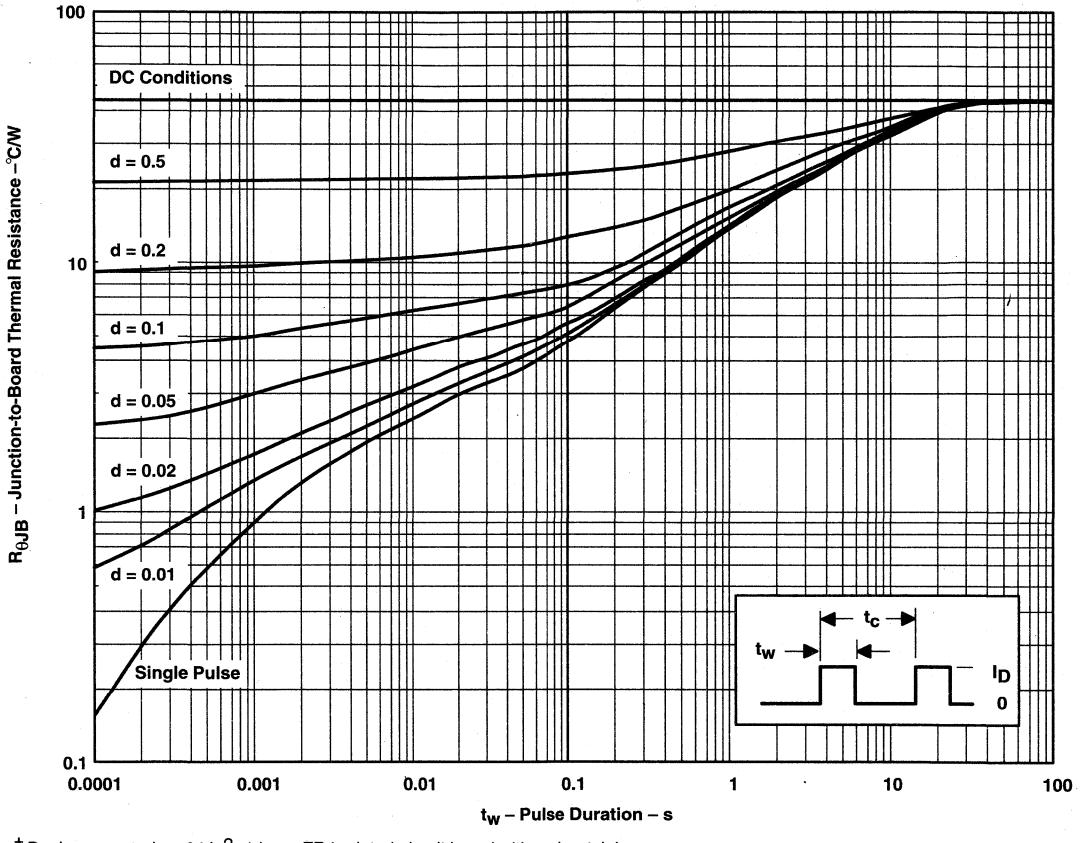


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



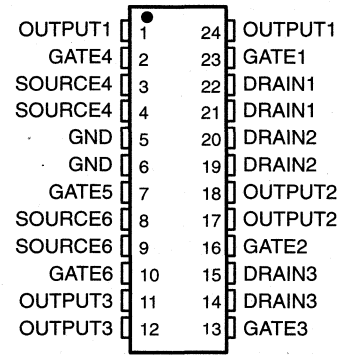
† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink

NOTE A. $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 17

- **Low $r_{DS(on)}$ . . . 0.35 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 4 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)

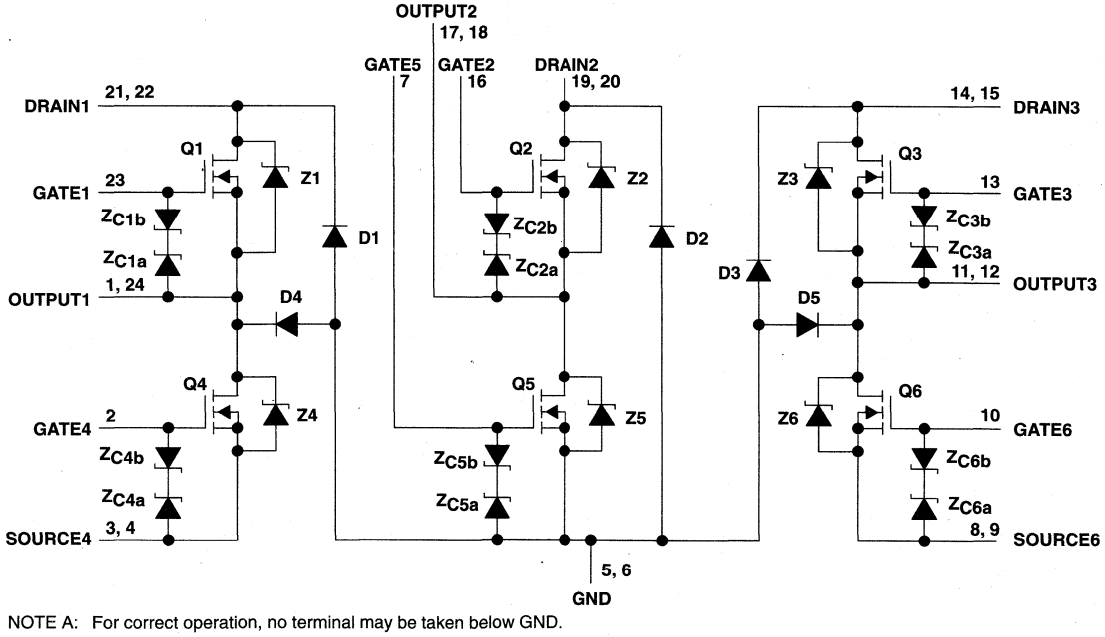


description

The TPIC1321L is a monolithic gate-protected logic-level power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as 3-half H-bridges. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC1321L is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Output-to-GND voltage	60 V
Drain-to-GND voltage	100 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1.25 A
Continuous source-to-drain diode current, T_C = 25°C	1.25 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	4 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	96 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3, D4, D5)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.25 A, V_{GS} = 5 V, See Notes 2 and 3			0.44	0.5	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.25 A, V_{GS} = 0 (Z1 – Z6), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.25 A (D1 – D5) See Notes 2 and 3			4		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1.25 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.35	0.4	Ω
			T_C = 125°C		0.57	0.6	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 625 mA, See Notes 2 and 3 and Figure 9		1.6	1.74		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			200	250	pF
C_{oss}	Short-circuit output capacitance, common source				175	220	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 625 mA, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, and Z3		45		ns
Q_{RR}	Total diode charge					50		nC

resistive-load switching characteristics, T_C = 25°C

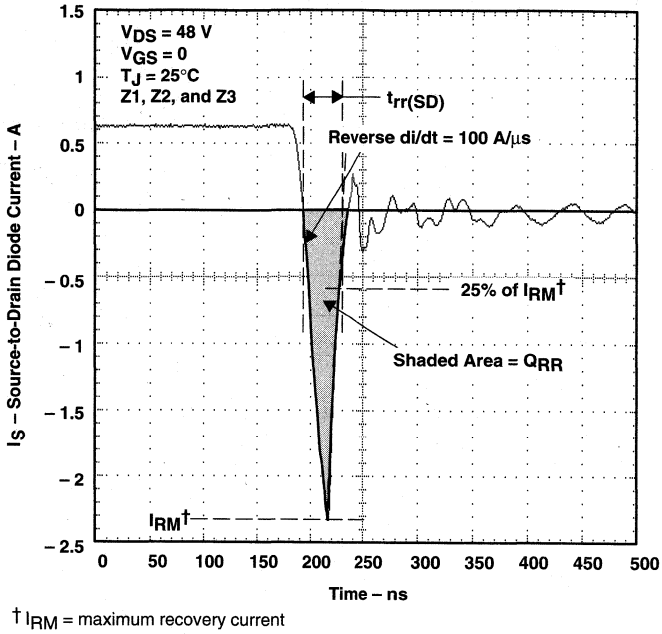
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 40 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		34	70	ns
$t_{d(off)}$	Turn-off delay time			80	150	
t_r	Rise time			28	55	
t_f	Fall time			15	30	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 625 mA, V_{GS} = 5 V, See Figure 3		4.6	5.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.7	0.88	
Q_{gd}	Gate-to-drain charge			2.5	3.13	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		44.5		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		

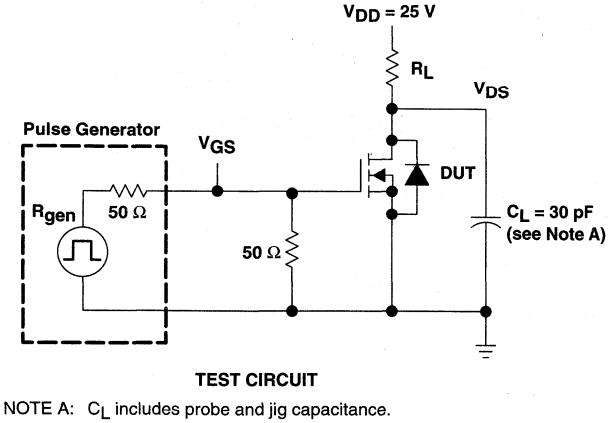
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

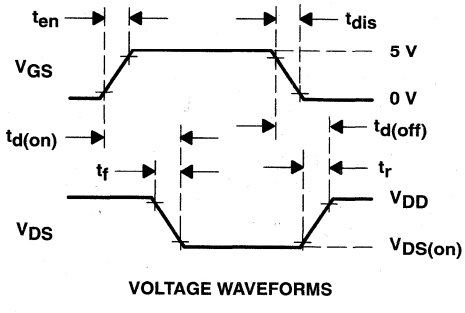
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode





NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

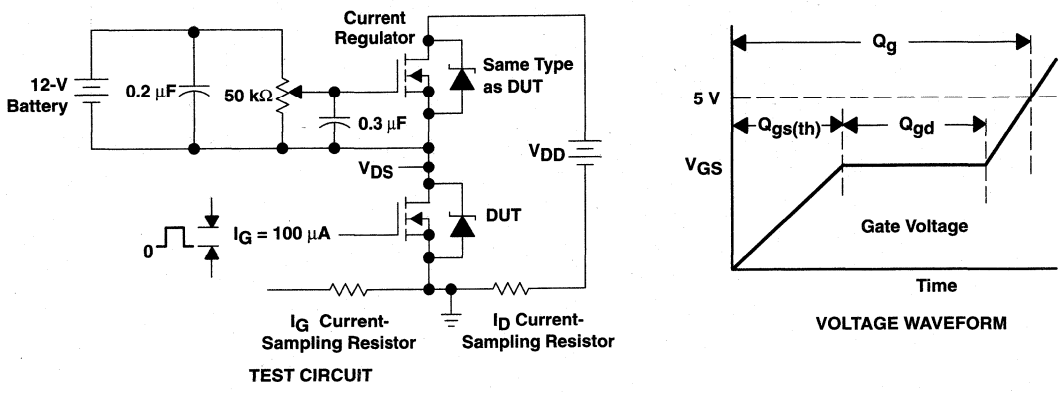
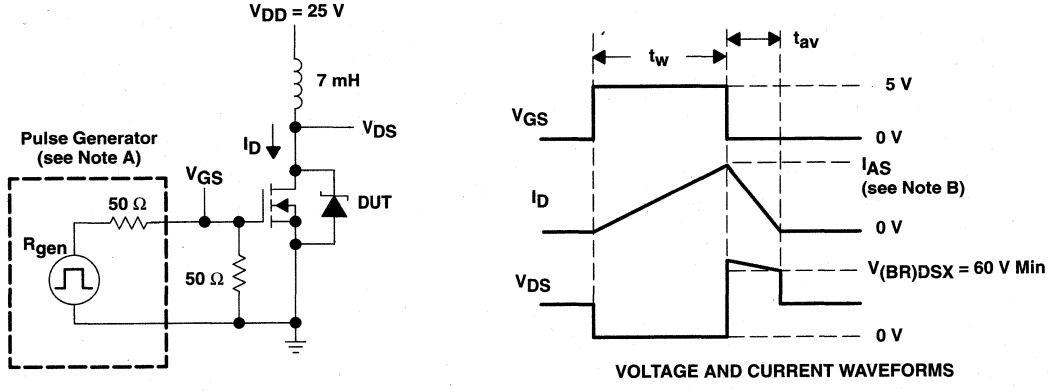


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 4$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 96$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

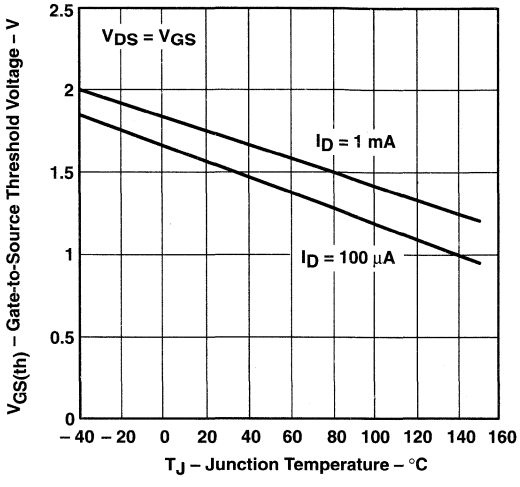


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

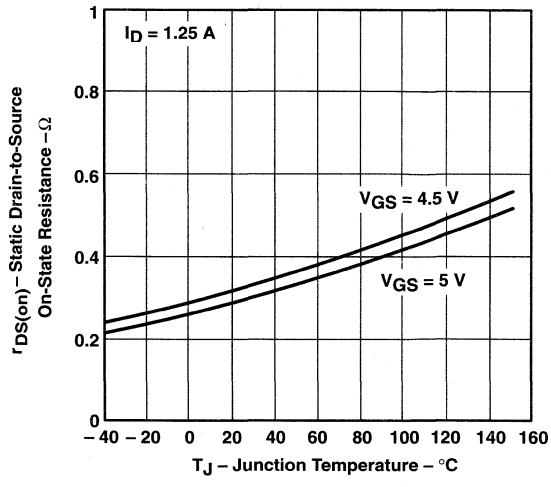


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

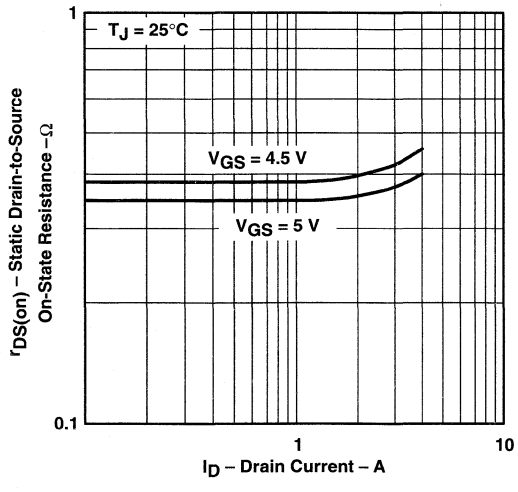


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

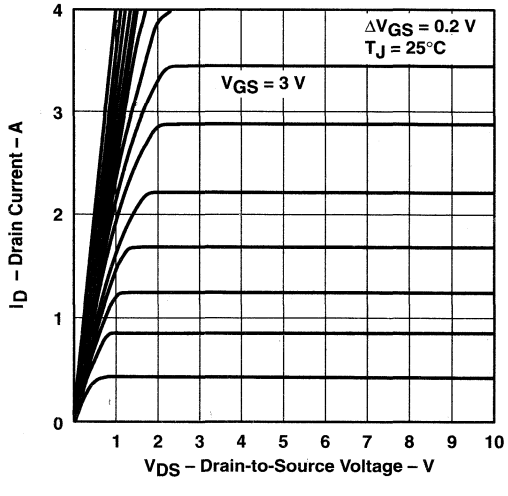


Figure 8

TYPICAL CHARACTERISTICS

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

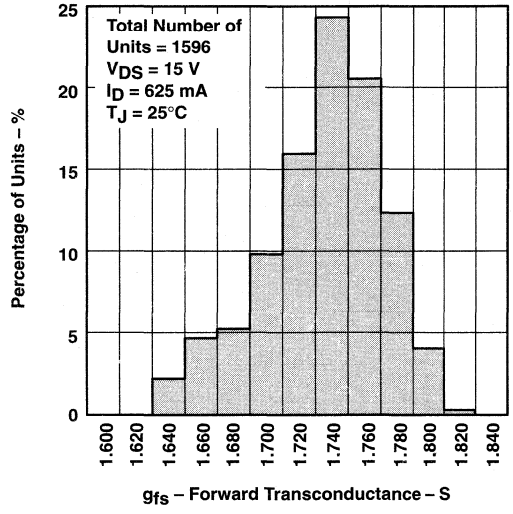


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

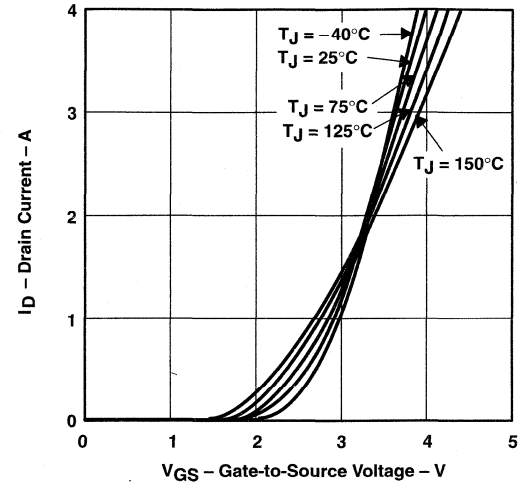


Figure 10

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

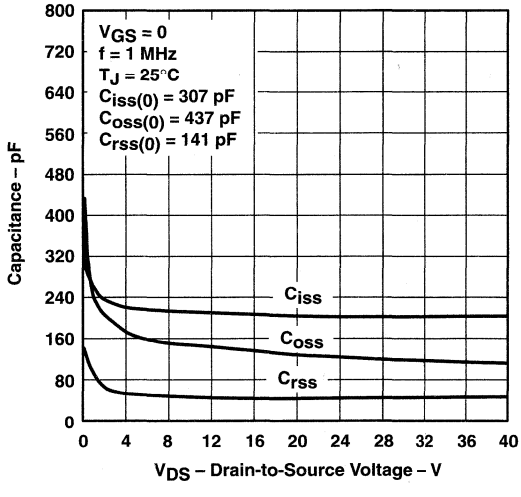


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

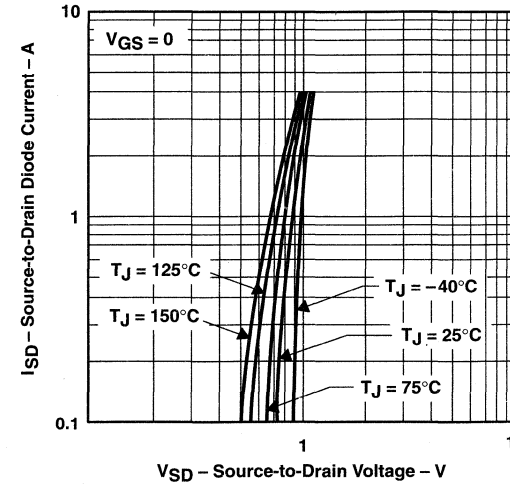


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

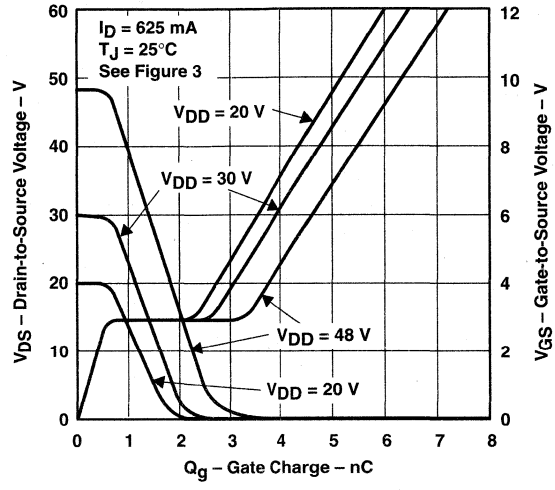


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

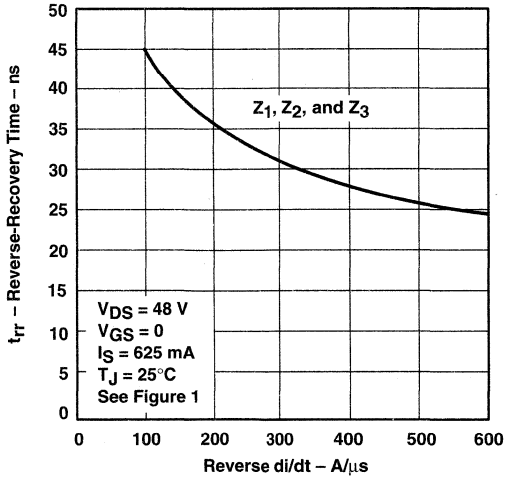
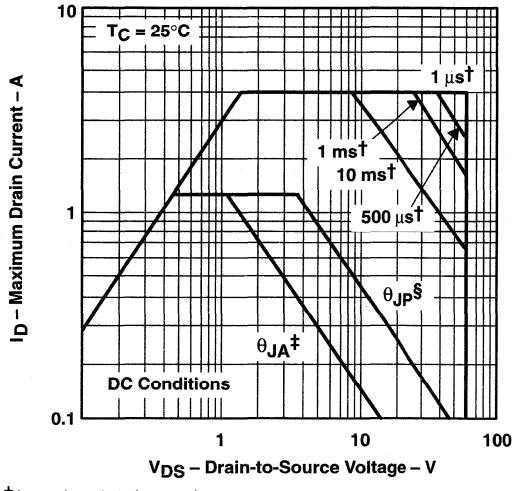


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
§ Device mounted in intimate contact with infinite heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

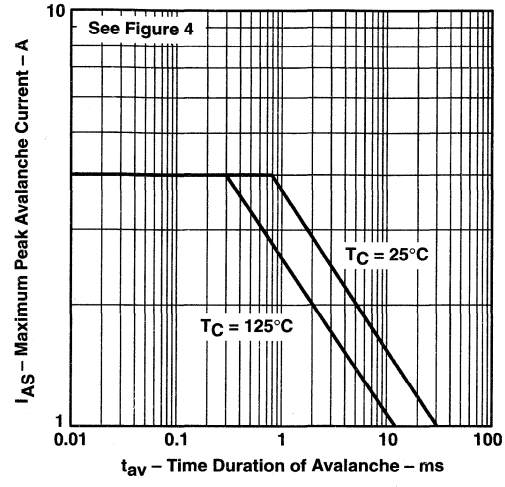
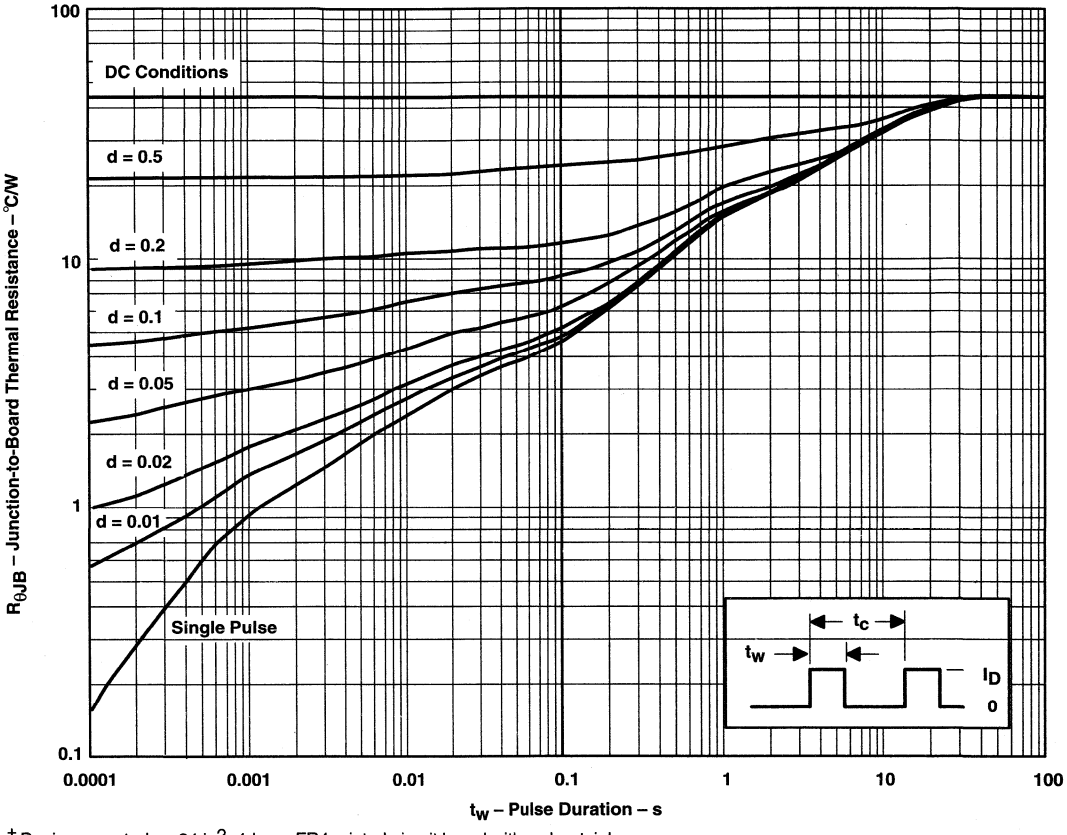


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



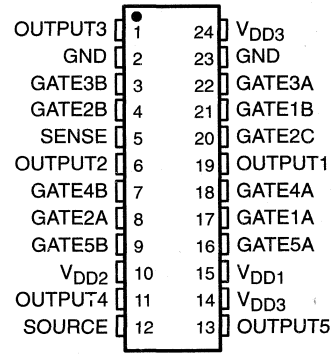
† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 17

- Low $r_{DS(on)}$:
  100 mΩ Typ (Full H-Bridge)
  400 mΩ Typ (Triple Half H-Bridge)
- Pulsed Current:
  12 A (Full H-Bridge)
  6 A (Triple Half H-Bridge)
- Matched Sense Transistor for Class A-B Linear Operation
- Fast Commutation Speed

DW PACKAGE
(TOP VIEW)

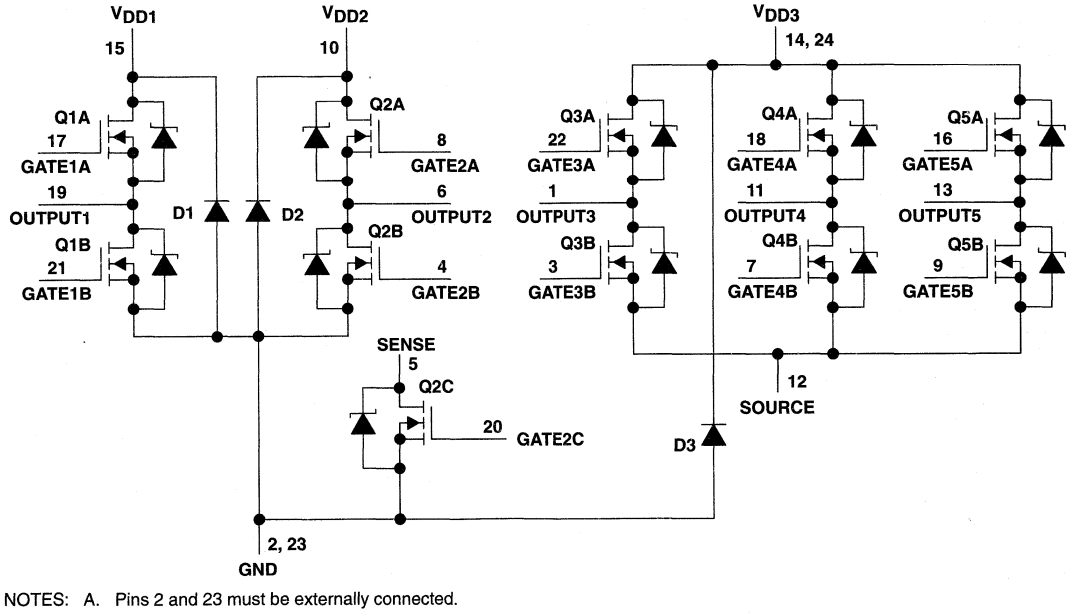


description

The TPIC1501 is a monolithic power DMOS array that consists of ten electrically isolated N-channel enhancement-mode power DMOS transistors, four of which are configured as a full H-bridge and six as a triple half H-bridge. The lower stage of the full H-bridge is provided with an integrated sense-FET to allow biasing of the bridge in class A-B operation.

The TPIC1501 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTES: A. Pins 2 and 23 must be externally connected.
B. Pins 14 and 24 must be externally connected.
C. No terminal may be taken greater than 0.5 V below GND.

PRODUCT PREVIEW

absolute maximum ratings, T_C = 25°C (unless otherwise noted)†

Supply-to-GND voltage	20 V
Source-to-GND voltage (Q3A, Q4A, Q5A)	20 V
Output-to-GND voltage	20 V
Sense-to-GND voltage	20 V
Gate-to-source voltage range, V_{GS} (Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	±20 V
Gate-to-source voltage range, V_{GS} (Q2C)	−0.7 V to 6 V
Continuous drain current, each output (Q1A, Q1B, Q2A, Q2B)	3 A
Continuous drain current, each output (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1.5 A
Continuous drain current (Q2C)	15 mA
Continuous source-to-drain diode current (Q1A, Q1B, Q2A, Q2B)	3 A
Continuous source-to-drain diode current (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1.5 A
Continuous source-to-drain diode current (Q2C)	15 mA
Pulsed drain current, each output, I_{max} (Q1A, Q1B, Q2A, Q2B) (see Note 1 and Figure 24)	12 A
Pulsed drain current, each output, I_{max} (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) (see Note 1 and Figure 25)	6 A
Pulsed drain current, I_{max} (Q2C) (see Note 1)	60 mA
Continuous total dissipation, T_C = 70°C (see Note 2 and Figures 24 and 25)	2.86 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Pulse duration = 10 ms, duty cycle = 2%
2. Package mounted in intimate contact with infinite heatsink.

PRODUCT PREVIEW

electrical characteristics (Q1A, Q1B, Q2A, Q2B), T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA,	V_{GS} = 0	20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.4	1.7	2.1	V
		I_D = 5 mA,	V_{DS} = V_{GS}	1.65	1.95	2.35	
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	I_D = 5 mA,	V_{DS} = V_{GS}			40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA (D1, D2)		20			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, See Notes 3 and 4	V_{GS} = 10 V,			0.24	V
V_F	Forward on-state voltage, GND-to-V_{DD1}, GND-to-V_{DD2}	I_D = 3 A (D1, D2) See Notes 3 and 4			1.8		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, See Notes 3 and 4 and Figure 19	V_{GS} = 0,		0.85	1.05	V
		I_S = 3 A, See Notes 3 and 4 and Figure 19	V_{GS} = 0,		0.9	1.1	
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 16 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, V_{DD1}-to-GND, V_{DD2}-to-GND, gate shorted to source	V_{DGND} = 16 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 3 and 4 and Figure 9	T_C = 25°C		0.1	0.12	Ω
			T_C = 125°C		0.14	0.18	
		V_{GS} = 10 V, I_D = 3 A, See Notes 3 and 4 and Figures 7 and 9	T_C = 25°C		0.1	0.12	
			T_C = 125°C		0.14	0.18	
g_{fs}	Forward transconductance	V_{DS} = 10 V, See Notes 3 and 4	I_D = 1 A,	1.5	2.5		S
		V_{DS} = 10 V, See Notes 3 and 4 and Figure 13	I_D = 1.5 A,	2	3		
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 10 V, f = 1 MHz,	V_{GS} = 0, See Figure 17		300		pF
C_{oss}	Short-circuit output capacitance, common source				225		
C_{rss}	Short-circuit reverse transfer capacitance, common source				160		
α_s	Sense-FET drain current ratio	V_{DS} = 6 V,	$I_{D(Q2B)}$ = 5 mA	100	150	200	

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

PRODUCT PREVIEW

source-to-drain diode characteristics (Q1A, Q2A), T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1.5 A,	V_{GS} = 0,			70		ns
Q_{RR}	Total diode charge	V_{DS} = 16 V, See Figures 1 and 23	di/dt = 100 A/µs,			90		nC
t_{rr}	Reverse-recovery time	I_S = 2 A,	V_{GS} = 0,			75		ns
Q_{RR}	Total diode charge	V_{DS} = 16 V,	di/dt = 100 A/µs,			110		nC

resistive-load switching characteristics (Q1A, Q1B, Q2A, Q2B), T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 16 V,	R_L = 16 Ω,	t_{en} = 10 ns,		20		ns
$t_{d(off)}$	Turn-off delay time	t_{dis} = 10 ns,	See Figure 3			30		
t_r	Rise time					15		
t_f	Fall time					25		
Q_g	Total gate charge	V_{DS} = 16 V, See Figure 4	I_D = 1.5 A,	V_{GS} = 10 V,		5.6	7	nC
$Q_{gs(th)}$	Threshold gate-to-source charge					0.8	1,	
Q_{gd}	Gate-to-drain charge					1.2	1.5	
L_D	Internal drain inductance					5		nH
L_S	Internal source inductance					5		
R_g	Internal gate resistance					0.25		Ω

PRODUCT PREVIEW

electrical characteristics (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B), T_C = 25°C (unless otherwise noted)

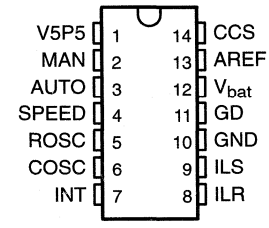
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 6	V_{DS} = V_{GS},	1.4	1.7	2.1	V
		I_D = 5 mA,	V_{DS} = V_{GS}	1.65	1.95	2.35	
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	I_D = 5 mA,	V_{DS} = V_{GS}			40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA (D3)		20			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.5 A, See Notes 3 and 4	V_{GS} = 10 V,			0.675	V
V_F	Forward on-state voltage, GND-to-V_{DD3}	I_D = 1.5 A (D3) See Notes 3 and 4			1.7		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.5 A, See Notes 3 and 4 and Figure 20	V_{GS} = 0		1	1.2	V
		I_S = 2 A, See Notes 3 and 4 and Figure 20	V_{GS} = 0		1.1	1.3	
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 16 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, V_{DD3}-to-GND, gate shorted to source	V_{DGND} = 16 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 0.3 A, See Notes 3 and 4 and Figures 8 and 10	T_C = 25°C		0.35	0.39	Ω
			T_C = 90°C		0.45	0.5	
			T_C = 125°C		0.50	0.56	
		V_{GS} = 10 V, I_D = 1.5 A, See Notes 3 and 4 and Figure 10	T_C = 25°C		0.4	0.45	
			T_C = 125°C		0.56	0.65	
g_{fs}	Forward transconductance	V_{DS} = 10 V, See Notes 3 and 4 and Figure 14	I_D = 500 mA,	0.3	0.8		S
		V_{DS} = 10 V, See Notes 3 and 4	I_D = 750 mA,	0.4	0.9		
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 10 V, f = 1 MHz,	V_{GS} = 0, See Figure 18		98		pF
C_{oss}	Short-circuit output capacitance, common source				98		
C_{rss}	Short-circuit reverse transfer capacitance, common source				65		

NOTES: 3: Technique should limit $T_J - T_C$ to 10°C maximum.
4: These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

PRODUCT PREVIEW

- **0 V to 16 V, 50 mA Max PWM Gate Drive Output**
- **Dual Speed Command Input Capability**
- **Effective Motor Voltage Adjustment**
- **100% Duty Cycle Capability**
- **Low Current (<200 μA) Sleep State**
- **Built-in Soft Start**
- **Over/Under Voltage Protection**
- **Over Current Protection of External FET/IGBT**

D or N PACKAGE
(TOP VIEW)



description

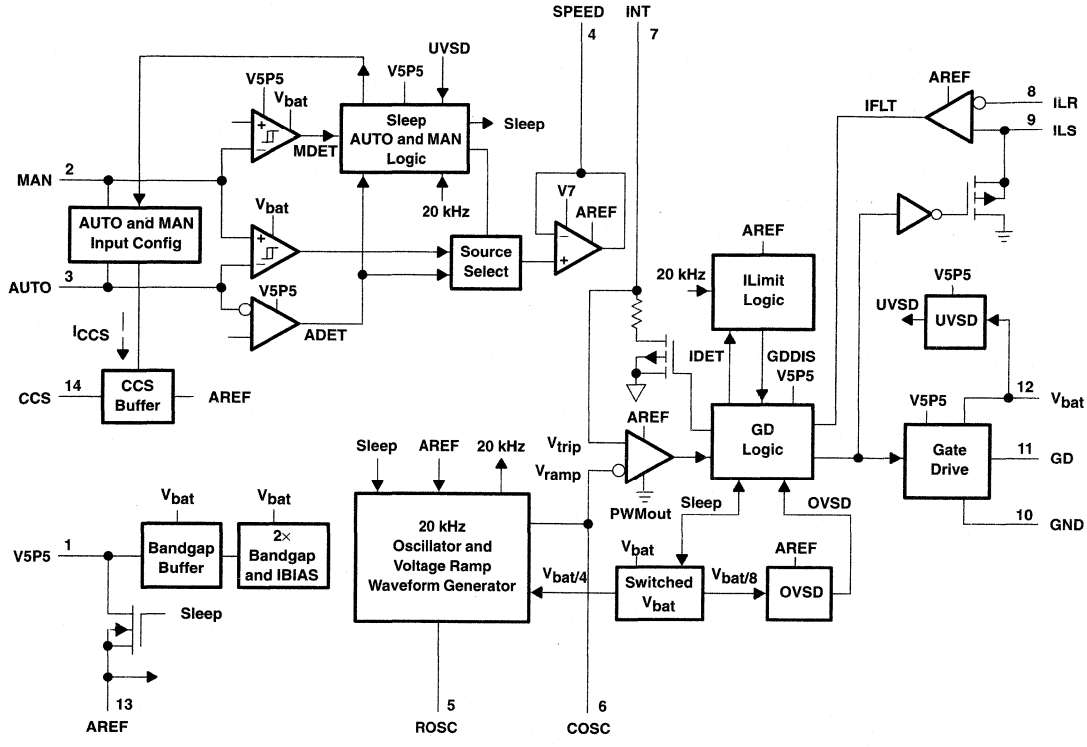
The TPIC2101 is a monolithic integrated control circuit designed for direct current (dc) brush motor control that generates a user-adjustable, fixed-frequency, variable duty cycle, pulse width modulated (PWM) signal primarily to control rotor speed of a permanent magnet dc motor. The TPIC2101 can also be used to control power to other loads such as solenoids and incandescent bulbs. This device drives the gate of an external, low side NMOS power transistor to provide PWM controlled power to a motor or other loads. Inductive current from motor or solenoid loads during PWM off-time is recirculated through an external diode.

The TPIC2101 accepts a 0% to 100% PWM signal (auto mode) or a 0 V to 2.2 V differential voltage (manual mode), and internally engages the correct operating mode to accept the input type.

The device operates in a sleep state, a run state, or a fault state. In the sleep state the gate-drive (GD) terminal is held low and the overall current draw is less than 200 μA. The normal operating mode of the device is in the run state and is initiated by any speed command. When the device detects an overvoltage or current fault, it enters the fault state.

The TPIC2101 is offered in a 14-terminal plastic DIP (N) package, and a SOIC (D) package, and is characterized for operation over the operating free-air temperature range of –40°C to 105°C.

functional block diagram



NOTE A. For correct operation, no terminal may be taken below GND.

TEXAS INSTRUMENTS
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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
V5P5	1	O	5.5 V supply voltage. V5P5 is a regulated voltage supply from V_{bat}, internally switched to AREF during the run state. This requires a 4.7 µF tantalum capacitor from V5P5 to GND for stability.
MAN	2	I	Manual control input. MAN is an active high (greater than 5.5 V asserts the manual mode) input that serves as a positive differential input (0-2.3 V full range) for the manual mode. In man mode, I_{man} is approx. 20×I_{CCS}.
AUTO	3	I	PWM control input. AUTO is an active low input that remains active if pulsed every 2048 counts of the oscillator frequency. It also serves as a negative differential input for the manual mode. In auto mode, I_{auto} is approx. 13×Iccs pullup, I_{auto} is approx. 20×I_{CCS} pulldown in man mode.
SPEED	4	O	Integrator output. SPEED is an integrator output with a required minimum resistance between SPEED and INT terminals of 20 kΩ (typically 1 second RC time constant, or as required for soft start).
ROSC	5	O	Oscillator resistor output. ROSC has an external resistor connected to ground which determines the constant charging current of COSC. The IC forces a voltage of V_{bat}/4 in run state.
COSC	6	O	Oscillator capacitor output. COSC has an external capacitor connected to ground which determines (with ROSC) switching frequency. f(osc) = 2/(ROSC×COSC)
INT	7	I	Integrator input. INT is an input from an integrator that requires a 4.7 µF capacitor and a 20 k minimum resistance between the SPEED and INT terminals.
ILR	8	I	Current limit reference. ILR is an input from a resistor divider off AREF.
ILS	9	I	Current limit sense. ILS senses drain voltage of external FET. ILS trips within ±10 mV of ILR.
GND	10		Ground terminal
GD	11	O	Gate drive output. GD, PWM output, 0-V_{bat} voltage, provides a 0-V_{bat} PWM output pre-drive for an external FET.
V_{bat}	12	I	Positive power input.
AREF	13	O	5.5 V reference voltage. AREF is a 5.5 V reference voltage switched from V5P5 during the run state. AREF is used as a reference for ILR in current limit detection and is capable of sourcing 2 mA of current.
CCS	14		Constant current sink. I_{CCS} equals AREF/(2×R_{ccs}). Requires an external resistor.

recommended external components for auto and manual modes (see Figures 2 and 4)

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
V5P5	1	Capacitor – 4.7 µF tantalum
MAN	2	Capacitor – 0.1 µF
MAN	2	Resistor – 499 Ω, 1%, 100 ppm
AUTO	3	Capacitor – 0.47 µF
AUTO	3	Resistor – 499 Ω, 1%, 100 ppm
SPEED	4	Resistor – 100 kΩ, 1%, 100 ppm to INT terminal, (minimum 20 kΩ)
ROSC	5	Resistor – 45.3 kΩ
COSC	6	Capacitor – 2200 pF
INT	7	Capacitor – 4.7 µF
CCS	14	Resistor – 27.4 kΩ, 1%, 100 ppm

detailed description

The TPIC2101 is an integrated circuit that generates a fixed frequency, variable duty cycle PWM signal to control the rotor speed of a permanent-magnet dc motor. This section provides a functional description of the device.

dual command speed input capability

The TPIC2101 is user configurable to either auto or manual mode, and can sense either configuration internal to the IC. In automatic mode, the speed-command-signal is an open-collector PWM signal on the AUTO terminal, and the MAN terminal is floating. In manual mode, the speed-command-signal is a variable resistance across the AUTO and MAN terminals with the MAN terminal connected to V_{bat}.

sleep, run, and fault states

The TPIC2101 operates in a sleep state, a run state, or a fault state. In the auto mode, a zero-speed input initiates the sleep state. In the manual mode, an open-circuit at the AUTO and MAN terminals initiates the sleep state. The device will also be in the sleep state during fault conditions. In the sleep state, the gate drive terminal (GD) is held low and the overall current draw is less than 200 μA. Any speed command initiates the run state, which is the normal operating state of the device. The fault state is entered only when the device detects an overvoltage or current fault. Fault state is exited either by removal of the overvoltage condition (exiting to run state) or by resetting a current fault by entering the sleep state.

speed command adjustment

The device adjusts the GD terminal PWM signal with changes in V_{bat} to keep the effective motor voltage constant. The effective motor voltage is defined to be the product of the GD terminal PWM rate and the voltage of V_{bat}. Figure 1 shows motor voltage as a function of input speed command in the automatic mode for various battery voltages. PWM_{in} is described as the duty cycle of the PWM signal at the AUTO terminal.

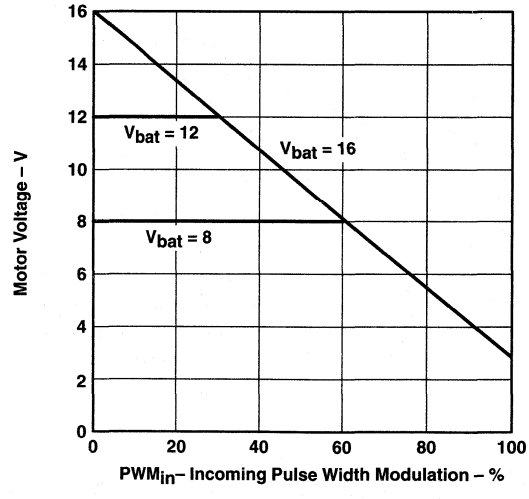


Figure 1. Motor Voltage vs. Incoming PWM for Various Battery Voltages

over/under voltage protection

The IC enters the fault state if V_{bat} rises above over-voltage shutdown (V_{OV} typically equals 18.5 V). If V_{bat} falls below the under-voltage shutdown (V_{UV} typically equals 7.5 volts) the IC enters sleep state. Hysteresis assures that the device will not toggle into and out of sleep state or fault condition.

current limit protection

Current through the motor is limited by lowering the GD terminal PWM when a high current situation occurs. If the condition persists, the device shuts off the gate drive (GD terminal) until the circuit is reset externally by entering the sleep state.

theory of operation

This section explains the normal circuit operation for the automatic and manual states.

power supply and oscillator

Positive voltage is supplied to the integrated circuit on the V_{bat} terminal, ground is the GND terminal. The IC steps down the V_{bat} supply to the regulated 5.5 V supply at the V5P5 terminal. AREF is shorted to V5P5 in run state and disconnected when the IC is in sleep state. Two terminal connections (COSC and ROSC) are provided to control an internal oscillator. The oscillator freq, $f_{(osc)}$, is defined by the following equation:

$$f_{(osc)} = \frac{2}{ROSC \times COSC}$$

Nominal oscillator frequency is 20-kHz based on the recommended components.

automatic mode signal decoding

In automatic state, a high-to-low signal transition on the AUTO terminal (open collector) will wake the device from the sleep state into the run state. The speed command information is contained in the duty cycle of a 100 Hz PWM signal on the same terminal. The speed information is inverted, i.e. a signal that is 10% high commands a faster speed than a 20% high signal. In automatic mode the MAN terminal is floating. The device is capable of rejecting ± 2 V of ground offset V_{IO} between the open-collector switching transistor and the GND terminal without affecting the output duty cycle. Two terminals are provided for an RC integrator (SPEED and INT) to average the incoming PWM signal for use as a PWM comparator input. Figure 2 illustrates the automatic state connections.

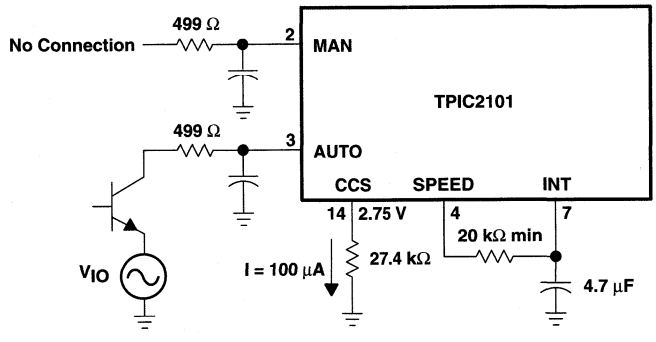


Figure 2. Automatic Mode Connections

automatic mode signal decoding (continued)

The device enters the sleep state if the PWM signal on the AUTO terminal is absent (the AUTO terminal remains high or low) for 2048 clock cycles of the 20 KHz oscillator. An internal 1 mA pull-up resistor is provided for the AUTO terminal when in the auto mode. This pull-up resistor is not present in the manual mode or during sleep state.

The device adjusts the output PWM duty cycle to keep the effective motor voltage constant with changing battery voltages (V_{bat}) as per the equation:

$$PWM_{out} = \frac{(2.88 + 13.12(1 - \text{Input Duty Cycle}))}{V_{bat}} \times 100\%$$

Figure 3 illustrates this transfer curve with various battery voltages.

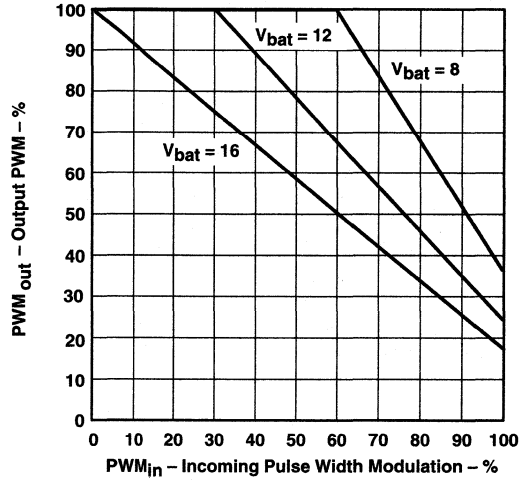


Figure 3. Output PWM vs. Incoming PWM for Various Battery Voltages

The allowable automatic mode PWM_{out} variation is ± 7% over all operating conditions as indicated in the AC characteristics Table.

manual mode speed signal decoding

In manual mode, a high input (>5.5V) on the MAN terminal changes the state of the device from sleep to run. While in the run state the device senses the resistance between the MAN and AUTO terminals by turning on a 2 mA current sink to each terminal. The MAN and AUTO current sinks are multiplied 20 X from the CCS current. This 2 mA current sink creates a 1 V drop across each 0.5 kΩ resistor and a 0 to 2.2 V differential across the 0 to 1 kΩ potentiometer (and thus across the 2 terminals). The SPEED and INT terminals should be utilized as in the proceeding section as a low-pass filter. When the connection to the MAN terminal is opened, the device enters the sleep state. In addition, the device is capable of rejecting up to 2.2 V of source voltage offset (V_{IO}), as indicated in Figure 4.

manual mode speed signal decoding (continued)

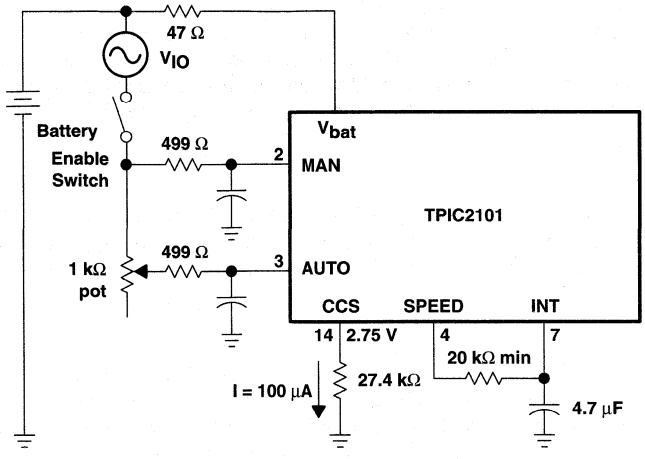


Figure 4. Manual Mode Connections

As in the automatic mode, the device will adjust the GD terminal PWM duty cycle to keep the effective motor voltage constant with changing battery voltages (V_{bat}). The transfer equation for the manual mode is:

$$PWM_{out} = \frac{(2.88 + 6.56(V_{MAN} - V_{AUTO}))}{V_{bat}} \times 100\%$$

Figure 5 shows the output characteristic for various source voltages.

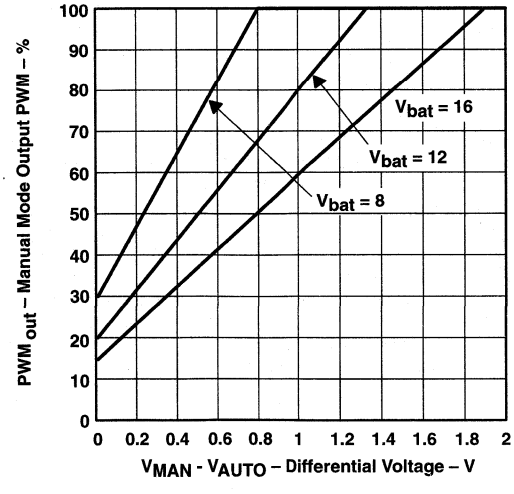


Figure 5. Manual Mode Input Signal vs. Output PWM

The allowable manual mode PWM_{out} variation is ±7% over all operating conditions as indicated in the AC characteristics table.

over/under voltage operating

The TPIC2101 detects an over or under voltage condition (on the V_{bat} terminal) and turns off the gate drive circuit. The device remains in this condition until the supply voltage returns to normal operating voltage. Hysteresis assures that the over/under voltage condition does not toggle off and on near the threshold. The INT terminal pulls toward GND through an internal impedance of less than 500 Ω during the over-voltage condition or during sleep state. This ensures a slow ramp up of the GD terminal PWM when the V_{bat} voltage returns to the operating range.

current limit operation

An over-current condition is detected if the ILS terminal is higher than the ILR terminal while the gate drive (GD terminal) is high. This condition activates a closed-loop control, causing the INT terminal to be pulled low (through an internal resistance less than 500 Ω) lowering the commanded duty cycle to close the loop.

current fault operation

During a window of 8192 clock cycles, a latch is set if at least once during the window, a current limit condition is detected. If a current limit condition is set for eight consecutive 8192 clock cycle windows, the gate drive (GD terminal) will be shut off for a disable period of 65536 clock cycles. During the disable period, the INT terminal is pulled to GND through an internal resistance of less than 500 Ω. After the disable period is completed, an internal restart is attempted. If the current limit is present again, as described above, for 8 consecutive windows, the GD and INT terminals are again pulled to GND and the device remains in this current fault state until the device is cycled through a sleep state to run state. However, if the current limit condition is not present during any of the eight 8192 clock cycle windows, the latches for the 8 count window timer and the two cycle shutdown/restart are reset. See timing diagrams, Figures 6, 7, and 8.

absolute maximum ratings over the operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{bat}‡	−0.3 V to 40 V
Input voltage range, MAN, AUTO	−0.3 V to 40 V
Input voltage range, INT CCS, ILR	−0.3 V to 7 V
Continuous gate drive output current, I_{GD}	±50 mA
Continuous speed output current, $I_{O(SPEED)}$	±1 mA
Continuous output current, $I_{O(V5P5)}$, $I_{O(AREF)}$	20 mA
Continuous ROSC output Current, $I_{O(ROSC)}$	1 mA
Continuous output current, $I_{O(CCS)}$	500 µA
Thermal Resistance, junction to ambient, $R_{\Theta JA}$: D package	131°C/W
N package	78°C/W
Operating free-air termperature range, T_A	−40°C to 105°C
Maximum junction temperature, T_{JM}	150°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Under load dump conditions, the voltage on V_{bat} can reach 40 V within 1 ms.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{bat}	8	12	16	V
AREF Input current $I_{(AREF)}$	0		2	mA
Input voltage, $V_{I(MAN)}$, $V_{I(AUTO)}$ (manual mode)	6		16	V
Differential voltage, $V_{I(MAN)} - V_{I(AUTO)}$	0		2.2	V
Input voltage, $V_{I(AUTO)}$ (auto mode)	0		5.5	V
V_I, ILR, ILS	0.5		2.75	V
Output resistance, input resistance, $R_{(CCS)}$	27.2	27.5	27.8	kΩ
Output Resistance, ROSC, r_o	20		100	kΩ
Output Capacitance, COSC, C_O	1		5	nF
Gate drive frequency f = 2/(ROSC × COSC), $f_{(GD)}$		20		kHz
Gate drive output capacitance, $C_{O(GD)}$			3300	pF
Operating free-air temperature, T_A	–40		105	°C

electrical characteristics, V_{bat} = 8 V to 16 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{bat}	Supply current (average), V_{bat}	V_{bat} = 16 V, GD open, f(osc) = 20 kHz, MAN = AUTO = V_{bat}		4	10	mA
		V_{bat} = 16 V, GD open, f(osc) = 20 kHz, MAN open, Auto mode, AUTO – 99% PWM_{in}		2	10	mA
$I_{bat(Q)}$	Quiescent current (sleep state), V_{bat}	V_{bat} = 13 V, AUTO and MAN open		150	200	µA
		V_{bat} = 13 V, AUTO shorted to MAN, floating		165	200	µA
$V_{(AREF)}$	Voltage supply regulation, AREF	$I_{(AREF)}$ = 0 – 2 mA, MAN = AUTO = V_{bat}	5.225	5.5	5.775	V
V_{IO}	Input offset voltage, current limit comparator, ILS, ILR	AUTO or MAN mode, ILS, ILR common mode, Voltage range 0.5 – 2.75 V, V_{int} = 4.5 V, Detect $I_{(int)}$ > 100 µA			10	mV
I_{IB}	Input bias current, current limit comparator, ILS, ILR†	ILS, ILR common mode, Voltage range 0.5 – 2.75 V			250	nA
I_{IO}	Input offset current, current limit comparator, ILS, ILR†	ILS, ILR common mode, Voltage range 0.5 – 2.75 V			100	nA
$I_{OL(CLS)}$	Pulldown current, ILS terminal blanking, ILS	ILS = 100 mV, GD commanded low	250	360		µA
$V_{IL(AUTO)}$	Automatic mode low level input voltage, AUTO	MAN open, AUTO mode, Lower $V_{I(AUTO)}$ until $V_{I(SPEED)}$ >2.4V	2.7	3	3.3	V
$V_{IH(AUTO)}$	Automatic mode high level input voltage, AUTO	MAN open, AUTO mode, Raise $V_{I(AUTO)}$ until $V_{I(SPEED)}$ < 2.4 V	3.6	4	4.4	V
$I_{I(AUTO)}$	Input current, automatic mode, AUTO	MAN open, Auto mode, $V_{I(AUTO)}$ = 0 V	–1		–10	mA
$I_{I(AUTOQ)}$	Input current, auto sleep mode, AUTO	MAN open, Sleep state, $V_{I(AUTO)}$ = 0 V	–40	–80		µA
$V_{IH(MAN)}$	High level input voltage, manual mode, MAN	V_{bat} = 9 V to 16 V, $V_{IH(MAN)}$ = $V_{IH(AUTO)}$, Raise $V_{(MAN)}$ until $V_{I(AREF)}$ > 2.5 V	5	5.5	6	V
$V_{IL(MAN)}$	Low level input voltage, manual mode, MAN	$V_{I(MAN)}$ = $V_{I(AUTO)}$, Lower $V_{I(MAN)}$ until $V_{I(AREF)}$ < 2.5 V	2.3	2.5	2.7	V
$V_{ID(MAN)}$	Input voltage, manual mode high differential (high speed command), MAN-AUTO	V_{bat} = 16 V, V_{bat} – 3.5 V < MAN < V_{bat}	1.7		2.3	V

† Indicates electrical parameter not tested in production.

electrical characteristics, V_{bat} = 8 V to 16 V, T_A = 25°C (continued)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$V_{ID(low)}$	Input voltage, manual mode low differential (low speed command), MAN–AUTO	V_{bat} –3.5 V < MAN < V_{bat}+ΔV where "Δ" is the lesser of 2 V and 16 V –V_{bat}, PWM_{out} @ $V_{(diff)}$ = 0.2 V ≥ PWM_{out} @ $V_{I(DIFF)}$= 0 V				0.2	V
$I_{I(MAN)}$ $I_{I(AUTO)}$	Input currents, auto and manual mode, MAN, AUTO	V_{bat} –3.5 V < MAN < V_{bat} +ΔV where "Δ" is the lesser of 2 V and 16 V –V_{bat}, MAN – AUTO = 0 V to 2 V, $R_{(css)}$ = 27.5 kΩ to GND		1.70	2	2.30	mA
$I_{I(MANRATIO)}$	Input current, manual mode matching ratio, MAN, AUTO	V_{bat} –3.5 V < MAN < V_{bat} +ΔV where "Δ" is the lesser of 2 V and 16 V –V_{bat}, MAN – AUTO = 0 V to 2 V, R_{CSS} = 27.5 kΩ to GND		–7		7	%
$I_{I(MAN(a))}$	Input current, man terminal auto mode, MAN	Auto mode,	MAN = 2.2 V	5	10	15	µA
$I_{I(MANQ)}$	Input current, man terminal sleep mode, MAN	Sleep state,	MAN = 2.2 V	5	10	15	µA
$V_{(CCS)}$	Constant current sink voltage regulation, CCS	Auto or Man mode,	$I_{(CCS)}$ = –100 µA	2.58	2.78	2.92	V
$V_{(OV)}$	Over voltage shutdown, V_{bat}	V_{bat} rising from 16 V, Detect $I_{(INT)}$ > 100 µA	INT = 1 V,	17	18.5	20	V
$V_{hys(OV)}$	Hysteresis, over voltage, V_{bat}	V_{bat} rising from 20.1 V, Detect $I_{(INT)}$ < 100 µA	INT = 1 V,	0.5	0.8	0.99	V
$V_{IT-(UVLO)}$	Under voltage shutdown negative going threshold voltage, V_{bat}	MAN = V_{bat}, Detect AREF < 2.5 V	V_{bat} falling from 9 V,	7	7.5	8	V
$V_{IT+(UVHI)}$	Under voltage shutdown positive going threshold voltage, V_{bat}	MAN = V_{bat}, Detect AREF > 2.5 V	V_{bat} rising from 6.9 V,	8	8.5	9	V
$V_{hys(UV)}$	Hysteresis, under voltage, V_{bat}	$V_{(UVHI)}$ – $V_{(UVLO)}$		0.5	1		V
$V_{OH(GD)}$	High level output voltage, gate drive, GD	I_{GD} = –50 mA, Run state	INT = 4.5 V,	V_{bat} –3		V_{bat}	V
		I_{GD} = –2 mA, Run state	INT = 4.5 V,	V_{bat} –0.2		V_{bat}	V
$V_{OL(GD)}$	Low level output voltage, gate drive, GD	Run state, $V_{I(INT)}$ = 0 V,	I_{GR} = 50 mA, V_{COSC} = 1 V			3.5	V
		Run state, INT = 0 V,	I_{GD} = 2 mA, V_{COSC} = 1 V			0.75	V
$V_{GD(SL)}$	Gate voltage, sleep-state, GD	Sleep state,	I_{GD} = 2 mA		0.03	0.75	V
$I_{(GDP)}$	Pulldown current, gate drive passive, GD	V_{bat} open,	V_{GD} = 0.75 V	7.5	20		µA
$I_{(INT)}$	Pulldown current, INT	Run state, $V_{I(INT)}$ = 1 V	V_{ILS} > V_{ILR},	2	3		mA

switching characteristics, V_{bat} = 8 V to 16 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{bat} = 16 V, Load = 3300 pF, ROSC = 45.3 kΩ, COSC = 2200 pF			1	µs
t_f	Fall time	V_{bat} = 16 V, Load = 3300 pF, ROSC = 45.3 kΩ, COSC = 2200 pF			0.8	µs
	Output PWM absolute accuracy to spec equation	16 > V_{bat} > 9 Manual and automatic modes GD open, Measure at GD = 0.5 × V_{bat} @ 20 kHz	–7%		7%	
$f_{(osc)}$	Oscillator frequency	ROSC = 45.3 kΩ, COSC = 2200 pF	19	20	21	kHz
	Minimum speed pedestal	MAN = AUTO=V_{bat} = 16	15		21	%DC
		V_{bat} = 16, MAN floating, AUTO @ 99% duty cycle	15		21	%DC

PARAMETER MEASUREMENT INFORMATION

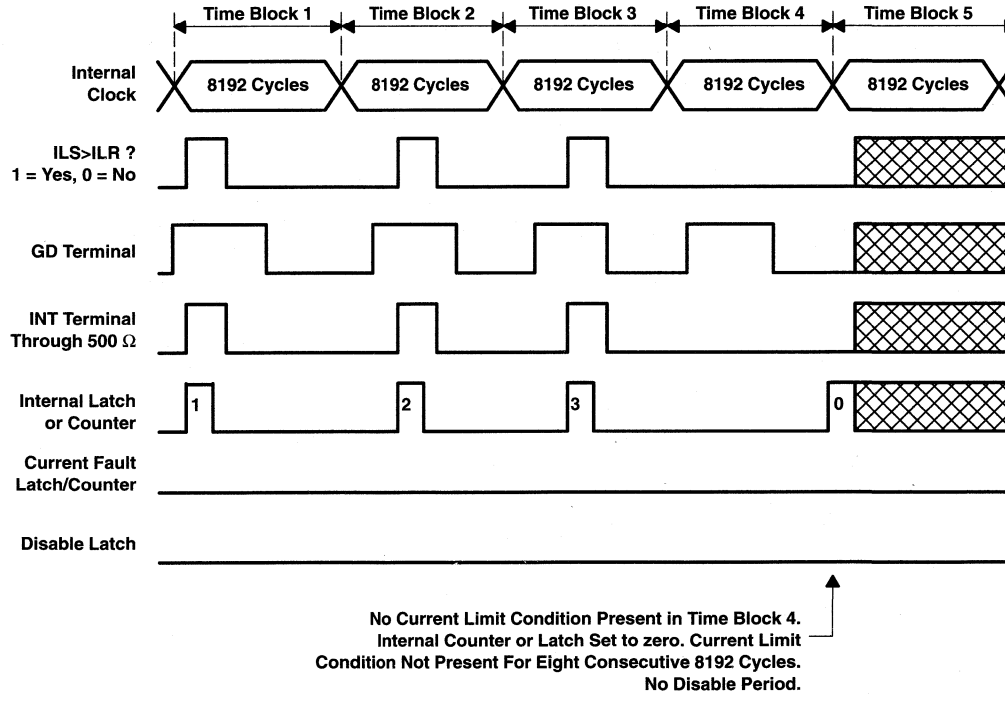


Figure 6. Current Fault Timing Diagram, Normal State

PARAMETER MEASUREMENT INFORMATION

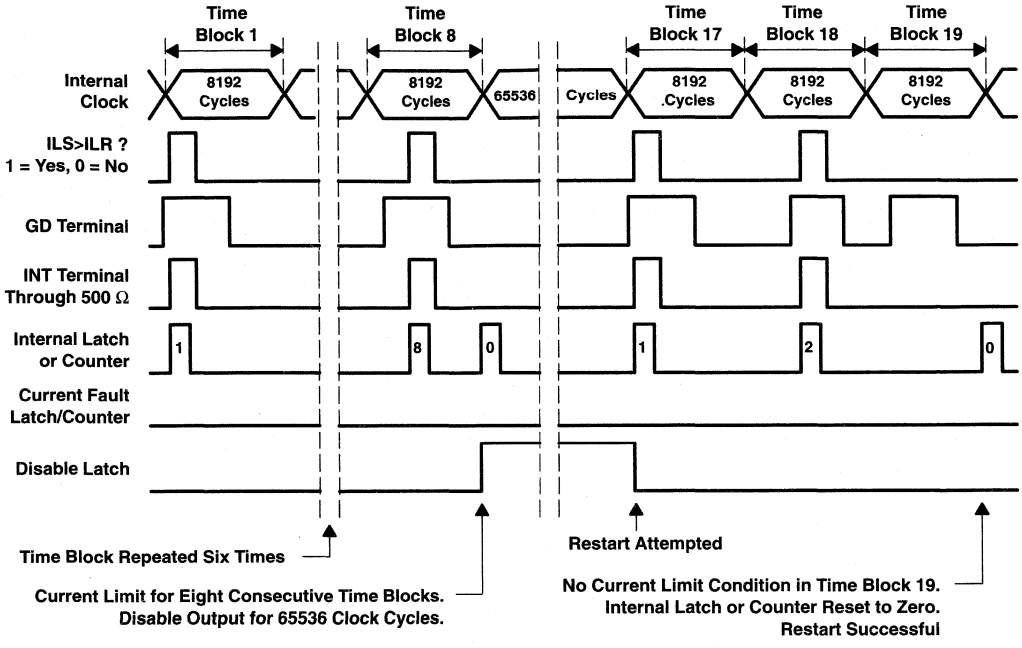
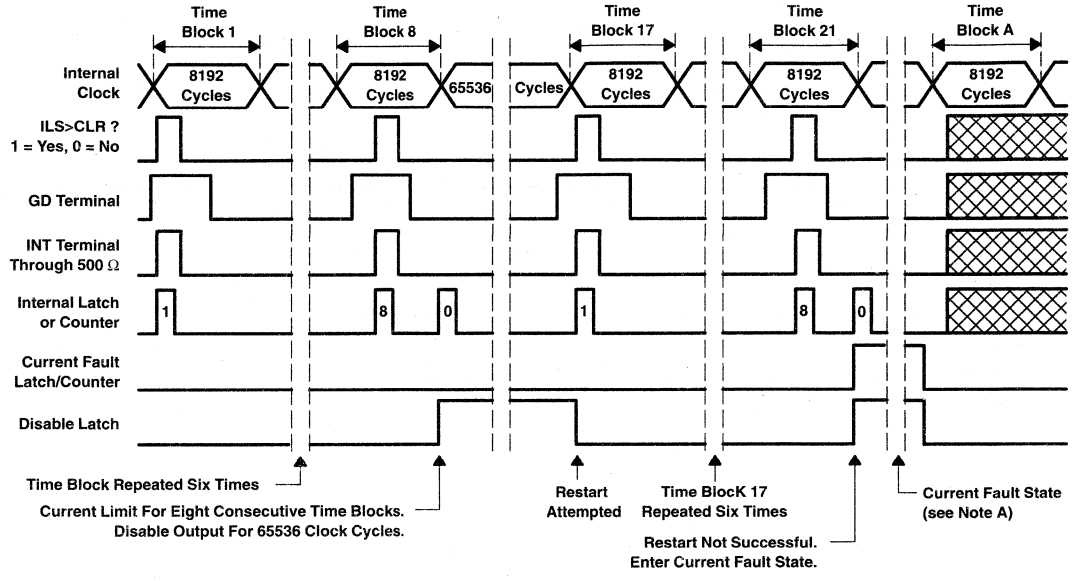


Figure 7. Current Fault Timing Diagram, Over-Current Limit Condition

PARAMETER MEASUREMENT INFORMATION



NOTE A. The integrated circuit remains in this state until cycled through the sleep state into the run state. Timing resumes as shown in time block A at right.

Figure 8. Over-Current Fault State Timing Diagram 3

TYPICAL CHARACTERISTICS

MANUAL/AUTO CURRENT
vs
CCS CURRENT (MANUAL MODE)

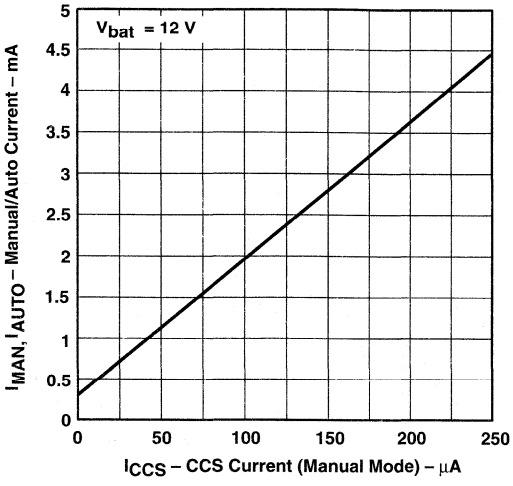


Figure 9

AUTO CURRENT
vs
CCS CURRENT (AUTO MODE)

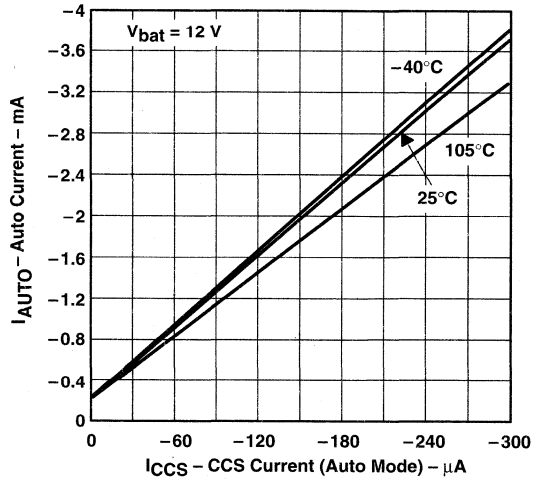


Figure 10

INTEGRATOR PULLDOWN CURRENT
vs
INTEGRATOR INPUT VOLTAGE

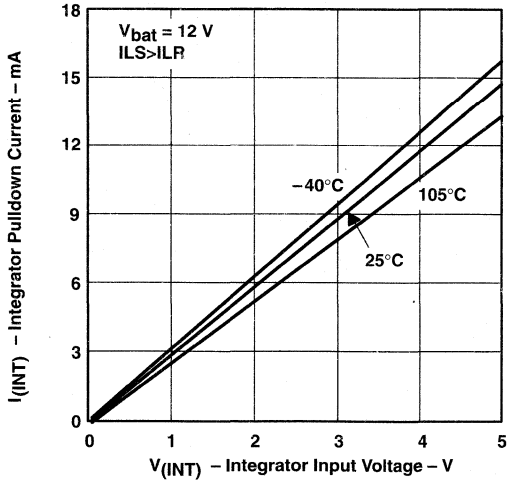


Figure 11

OSCILLATOR CAPACITOR CURRENT
vs
OSCILLATOR RESISTOR CURRENT

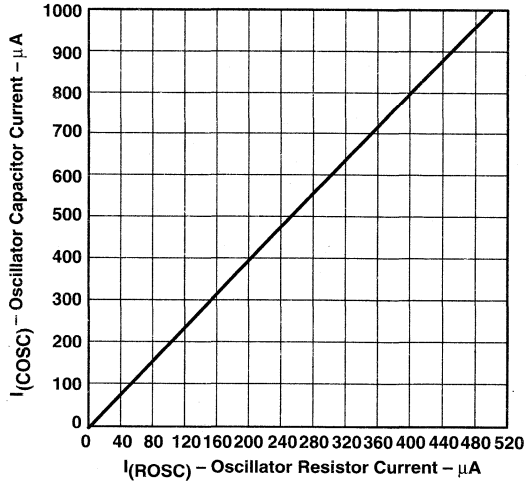


Figure 12

TYPICAL CHARACTERISTICS

GATE DRIVE LOW SIDE
vs
GATE DRIVE CURRENT

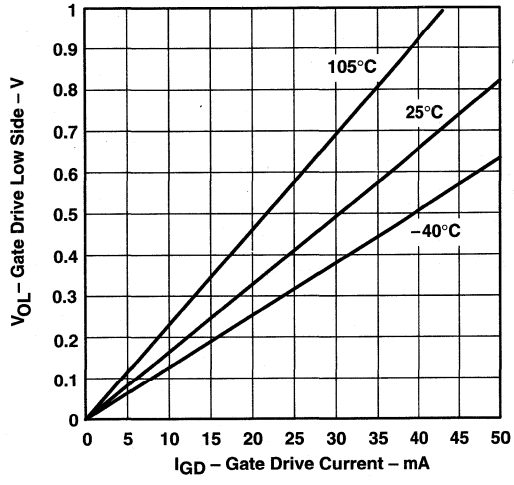


Figure 13

GATE DRIVE HIGH SIDE
vs
GATE DRIVE CURRENT

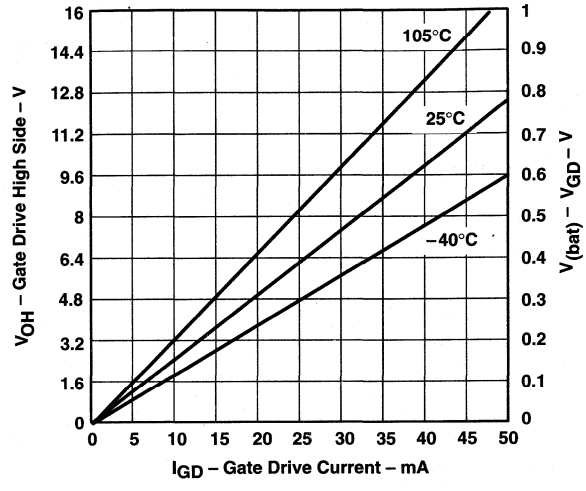


Figure 14

EFFECTIVE MOTOR VOLTAGE
vs
INCOMING PULSE WIDTH MODULATION

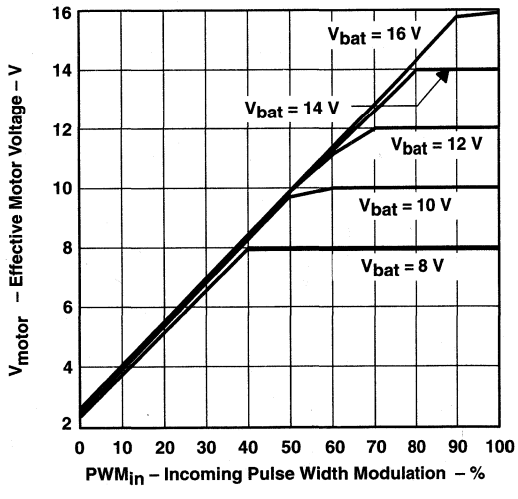


Figure 15

MOTOR RPM
vs
INCOMING PULSE WIDTH MODULATION

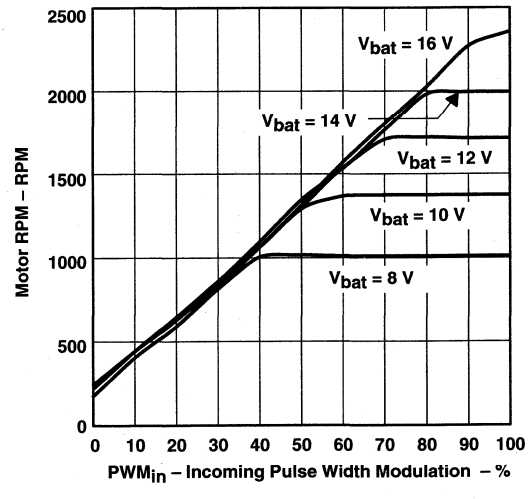


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE V5P5
vs
INPUT VOLTAGE AT V_{bat}

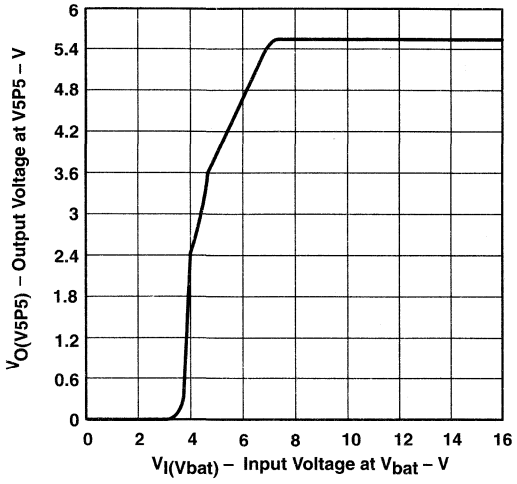


Figure 17

OUTPUT VOLTAGE AT V5P5
vs
AMBIENT TEMPERATURE

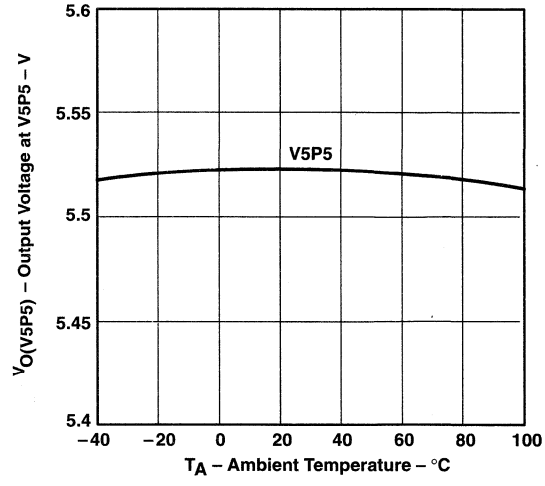


Figure 18

OUTPUT VOLTAGE AT V5P5
vs
V5P5 OUTPUT CURRENT

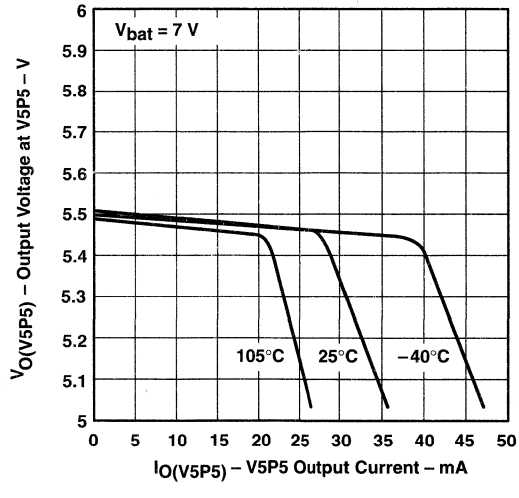
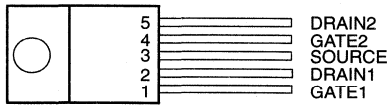


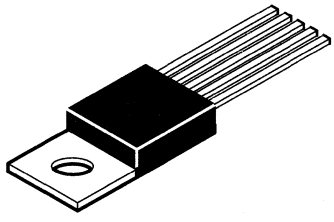
Figure 19

- **Two 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KC PACKAGE
(TOP VIEW)



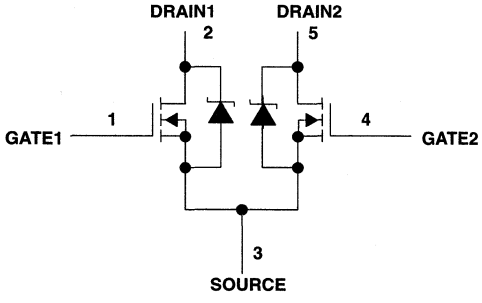
The tab is electrically connected to SOURCE.



description

The TPIC2202 is a monolithic power DMOS array that consists of two independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0			60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}			1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4				0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C			0.07	1	µA
			T_C = 125°C			1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0				10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0				10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C			0.09	0.125	Ω
			T_C = 125°C			0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4			2.5	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz				490		pF
C_{oss}	Short-circuit output capacitance, common source					285		
C_{rss}	Short-circuit reverse transfer capacitance, common source					90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{GS} = 0, di/dt = 100 A/µs, V_{DS} = 48 V, See Figure 1		0.8	1.3	V
t_{rr}	Reverse recovery time			200		ns
Q_{RR}	Total source-drain diode charge			1.5		µC

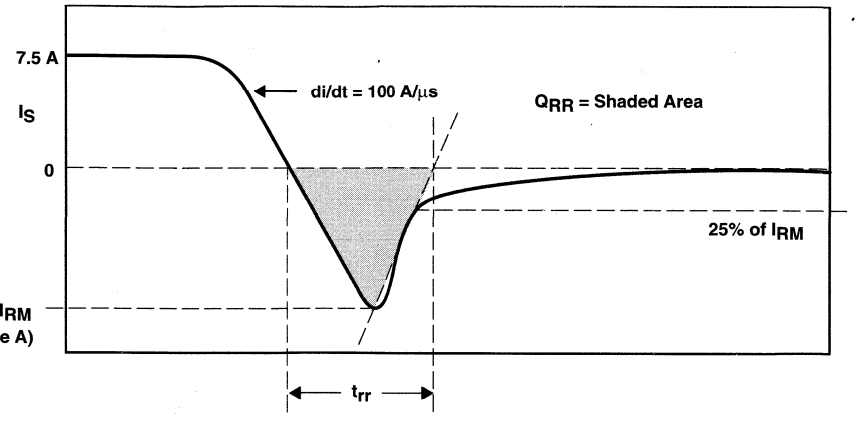
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 6.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		12		ns
$t_{d(off)}$	Turn-off delay time			100		
t_r	Rise time			43		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 2.5 A, V_{GS} = 10 V, See Figure 3		13.6	18	nC
Q_{gs}	Gate-source charge			8.3	11	
Q_{gd}	Gate-drain charge			5.3	7	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

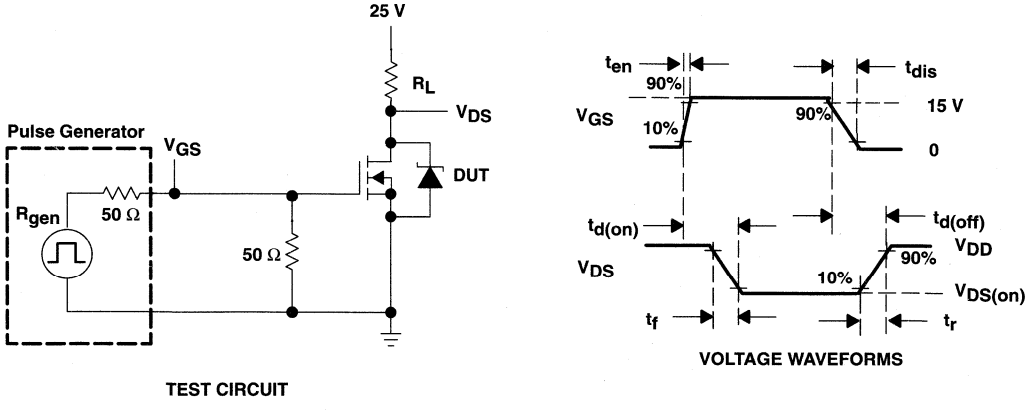


Figure 2. Test Circuit and Voltage Waveforms, Resistive Switching

PARAMETER MEASUREMENT INFORMATION

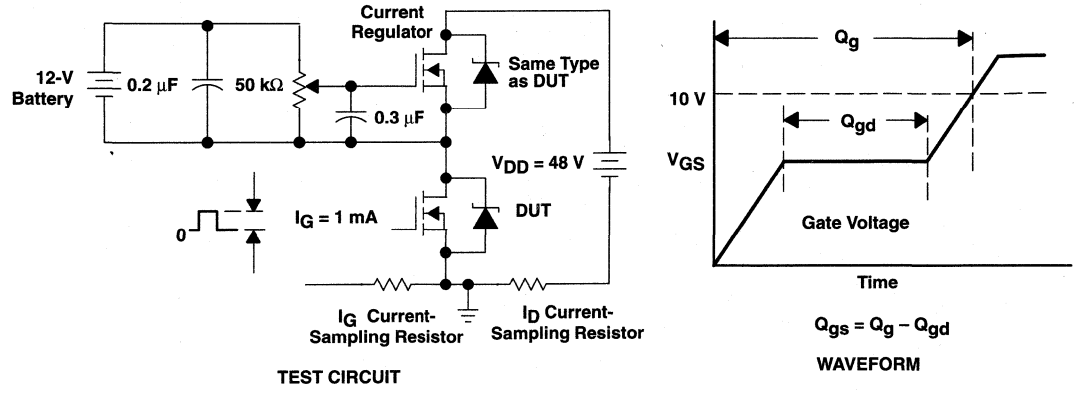
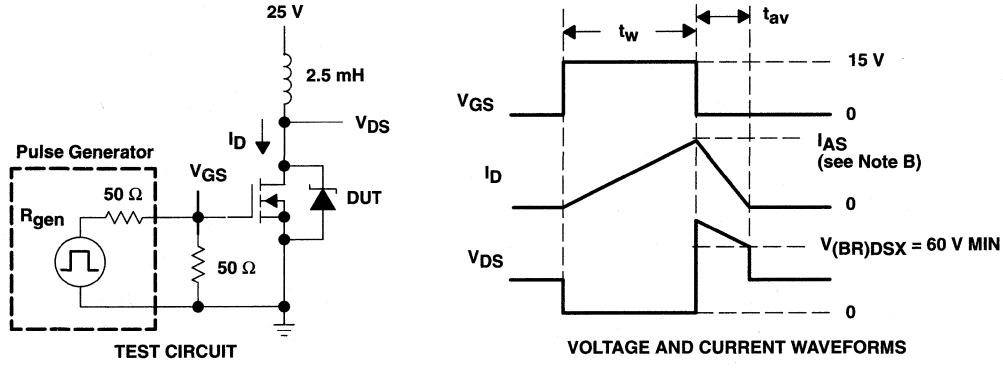


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

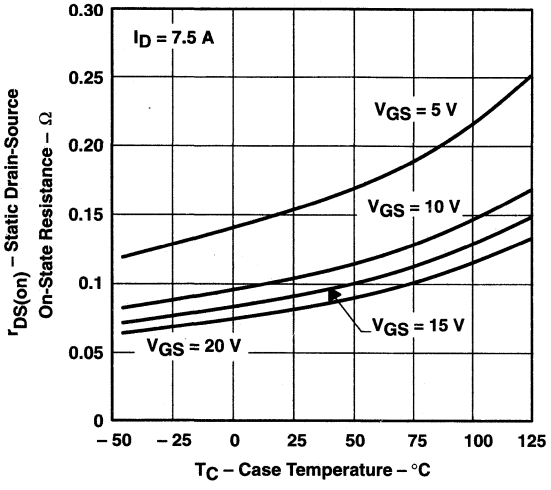


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

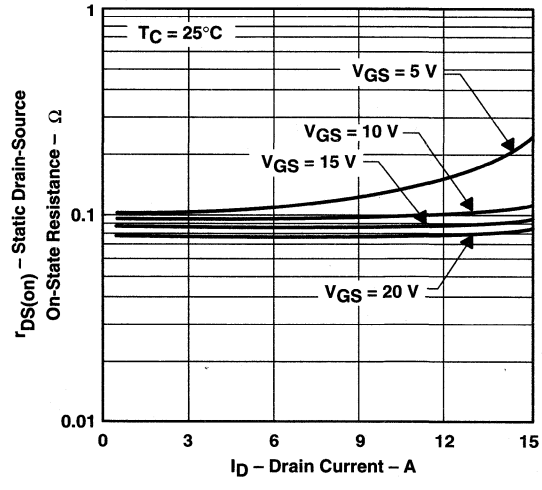


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

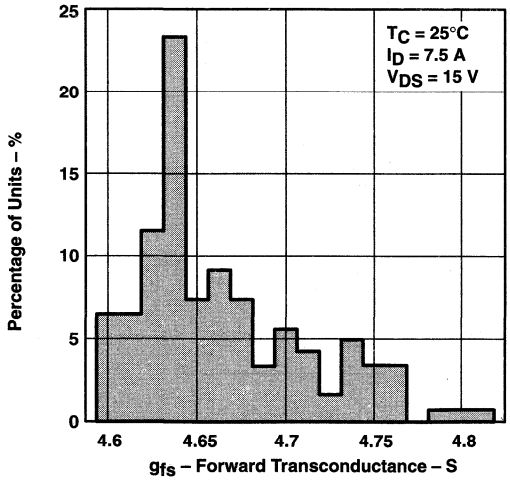


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

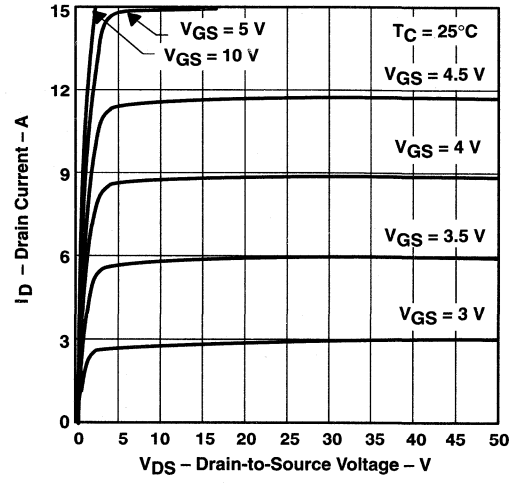


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
CASE TEMPERATURE

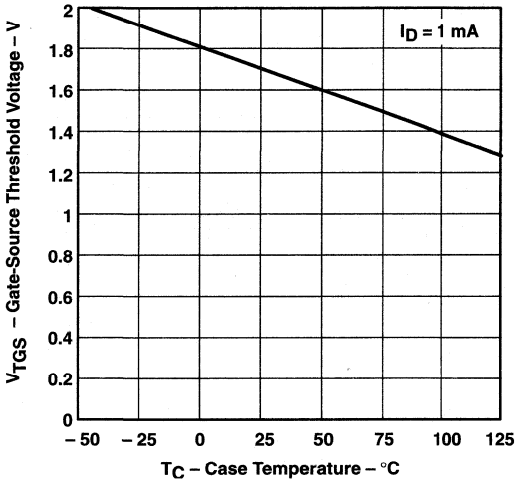


Figure 9

SOURCE-DRAIN DIODE CURRENT
vs
SOURCE-DRAIN VOLTAGE

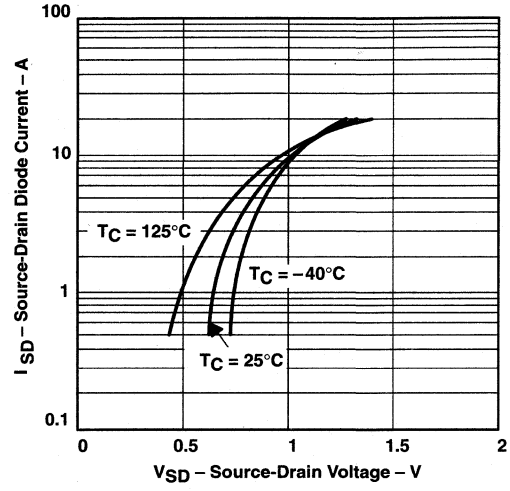


Figure 10

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

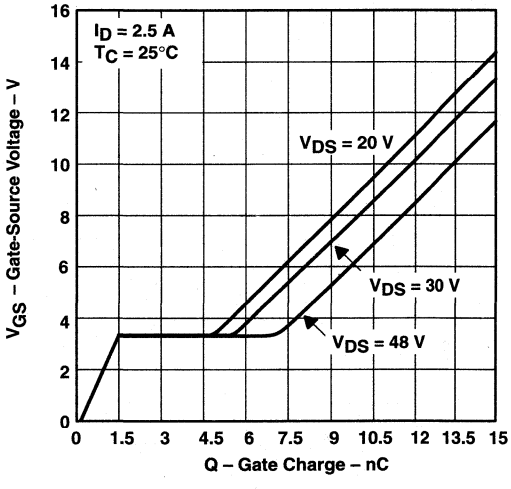


Figure 11

REVERSE RECOVERY TIME
vs
REVERSE di/dt

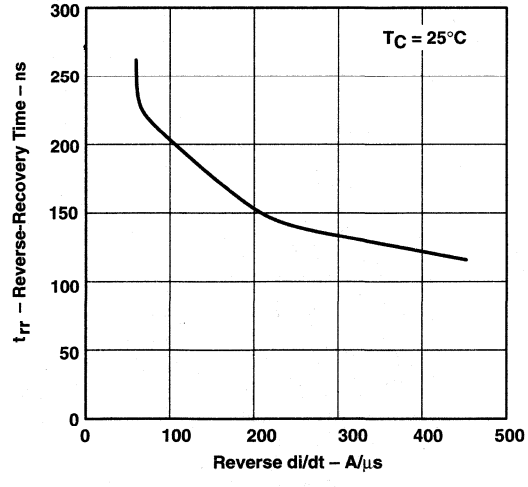


Figure 12

TYPICAL CHARACTERISTICS

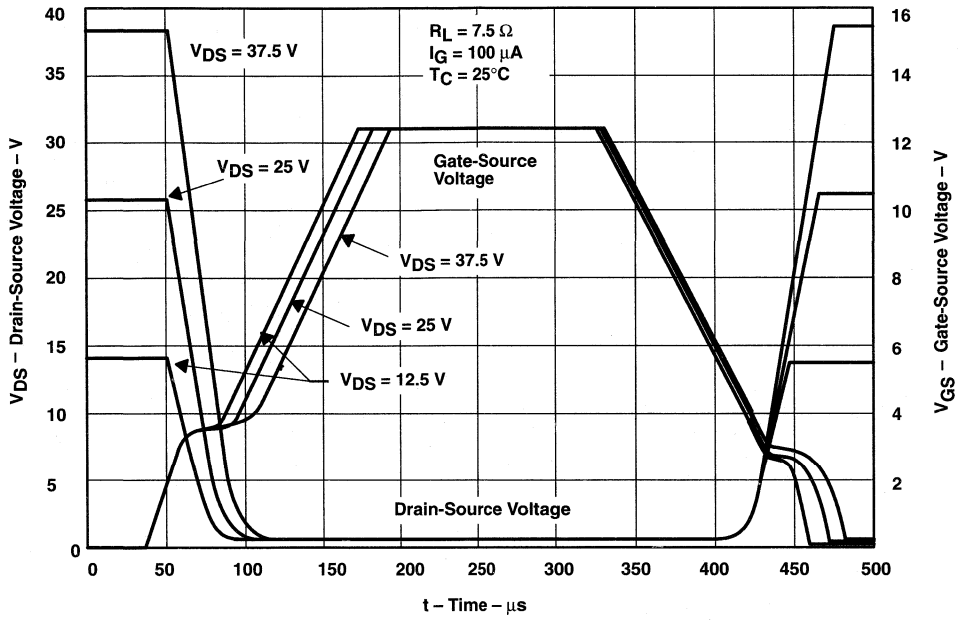


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-SOURCE VOLTAGE

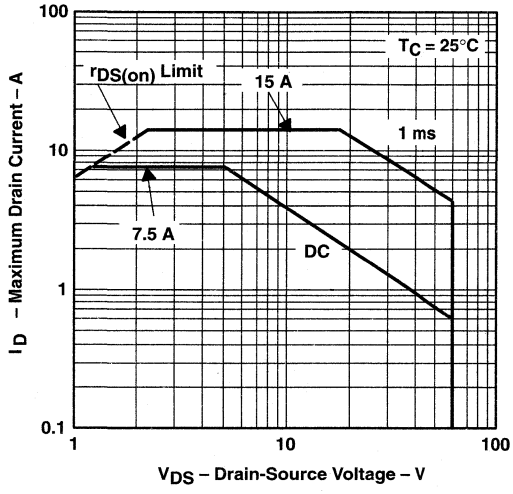


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

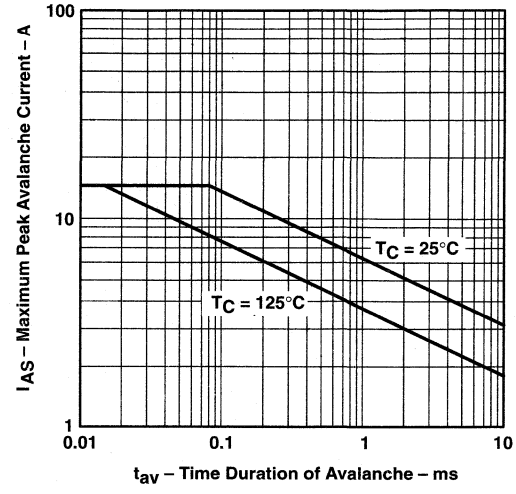
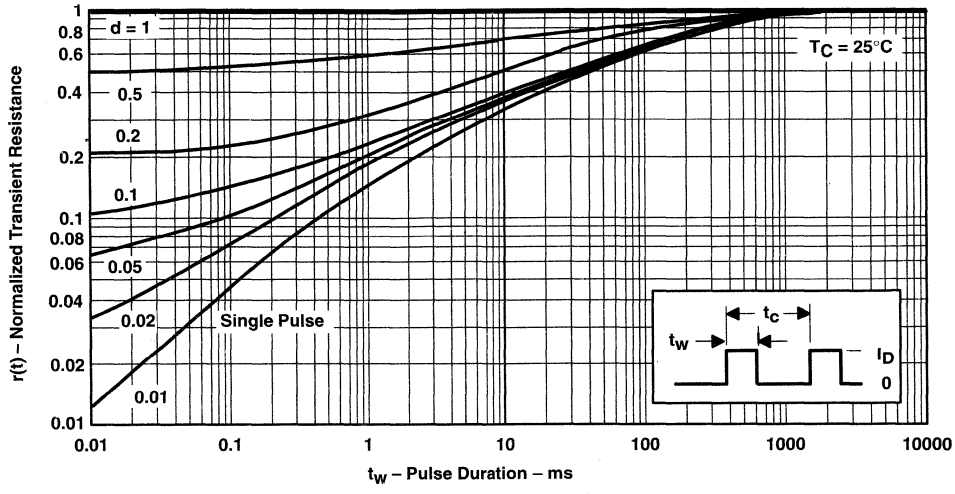


Figure 15

THERMAL INFORMATION

NORMALIZED TRANSIENT THERMAL IMPEDANCE vs SQUARE-WAVE PULSE DURATION

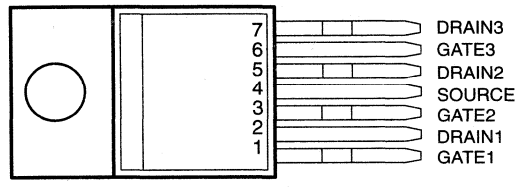


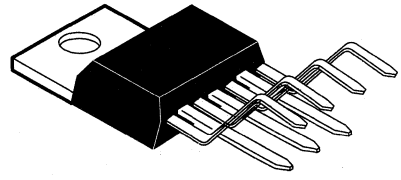
NOTES: $Z_{\theta JC}(t) = r(t)\, R_{\theta JC}$
t_W = pulse duration
t_C = period
d = duty cycle = t_W/t_C

Figure 16

- **Three 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)



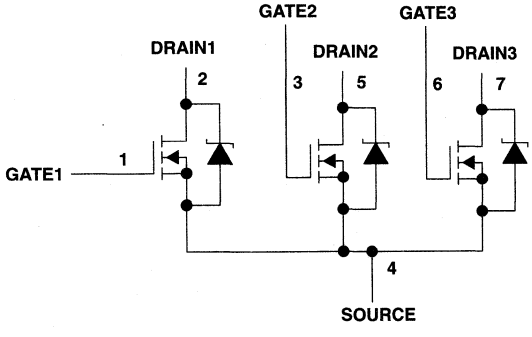


The tab is electrically connected to SOURCE.

description

The TPIC2301 is a monolithic power DMOS array that consists of three independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	50 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.66 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0			60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}			1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4				0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C			0.07	1	µA
			T_C = 125°C			1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0				10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0				10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C			0.09	0.125	Ω
			T_C = 125°C			0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4			3.3	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz				490		pF
C_{oss}	Short-circuit output capacitance, common source					285		
C_{rss}	Short-circuit reverse transfer capacitance, common source					90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{GS} = 0, di/dt = 100 A/µs, V_{DS} = 48 V, See Figure 1		0.8	1.3	V
t_{rr}	Reverse recovery time			200		ns
Q_{RR}	Total source-drain diode charge			1.5		µC

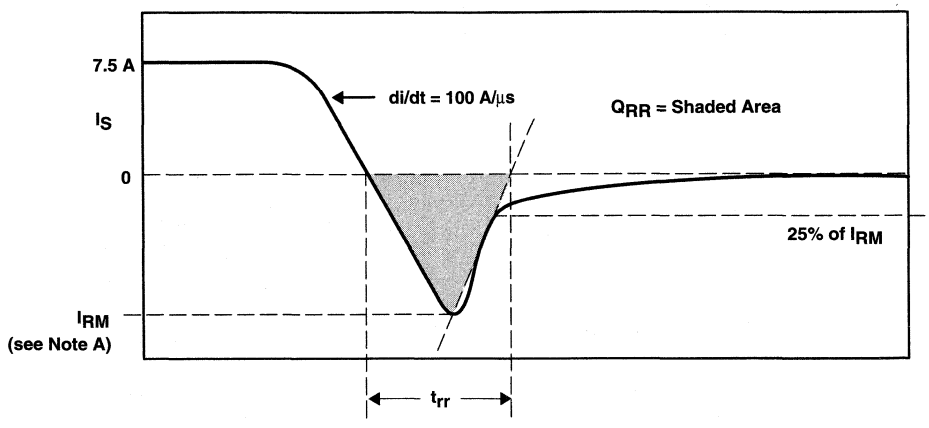
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 6.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		12		ns
$t_{d(off)}$	Turn-off delay time			100		
t_r	Rise time			43		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 2.5 A, V_{GS} = 10 V, See Figure 3		13.6	18	nC
Q_{gs}	Gate-source charge			8.3	11	
Q_{gd}	Gate-drain charge			5.3	7	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			1.5	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

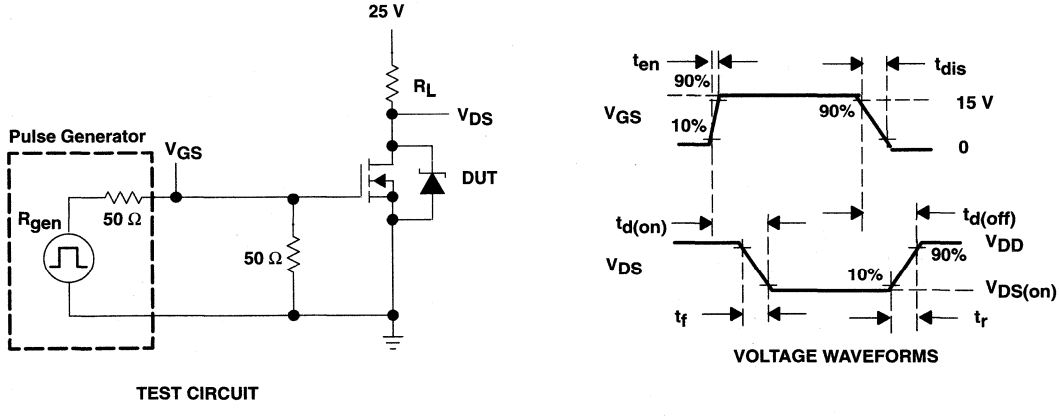


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

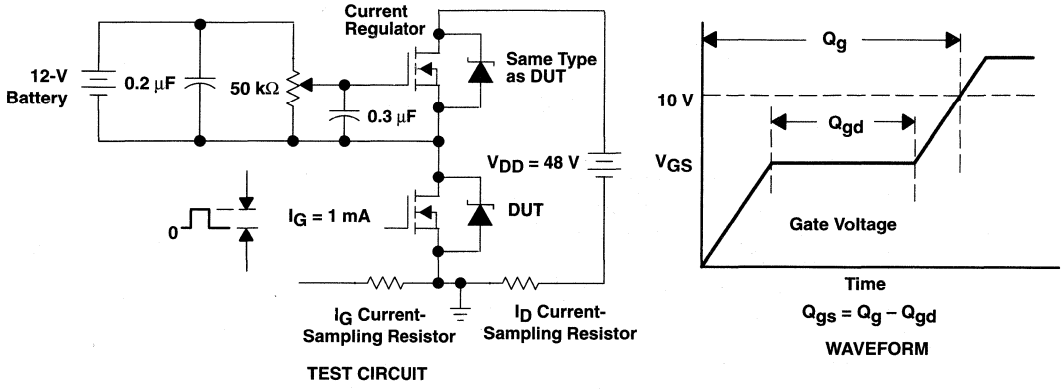
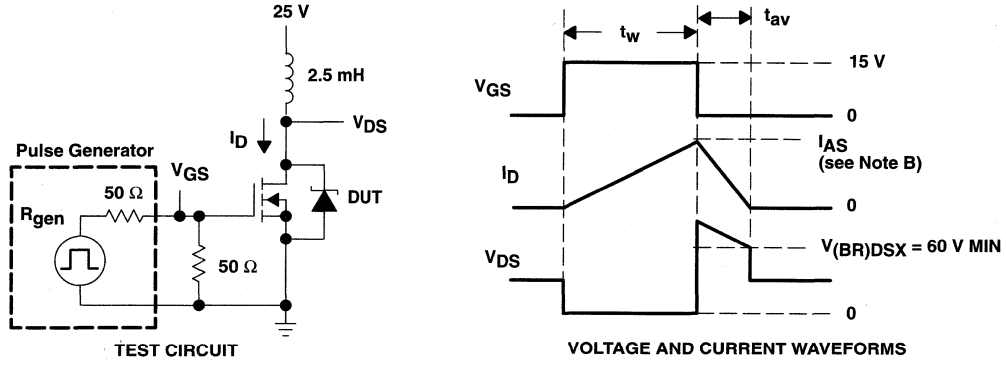


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

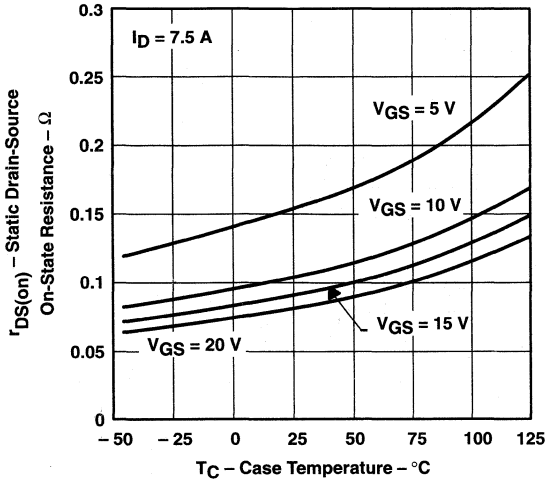


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

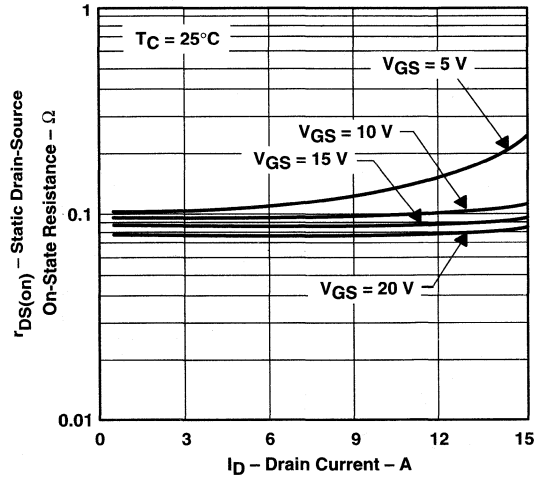


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

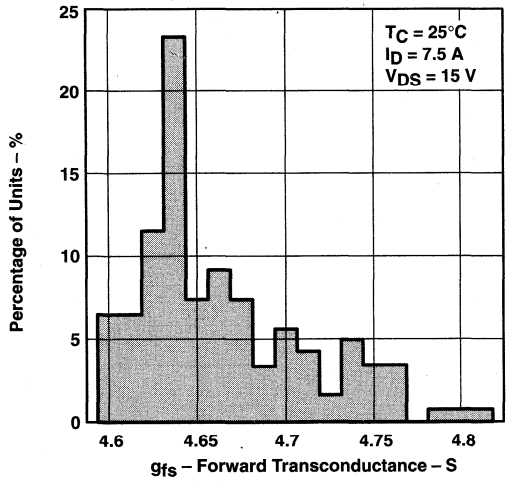


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

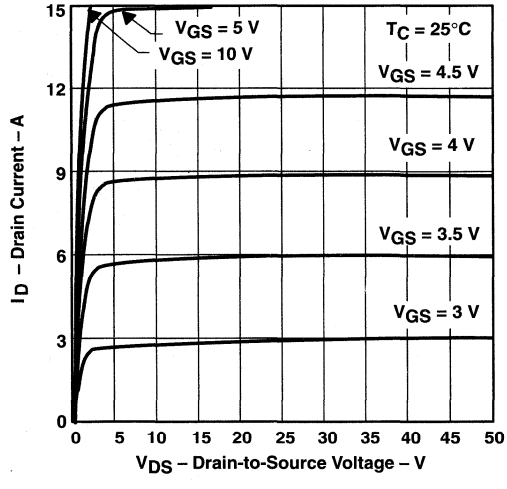


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
CASE TEMPERATURE

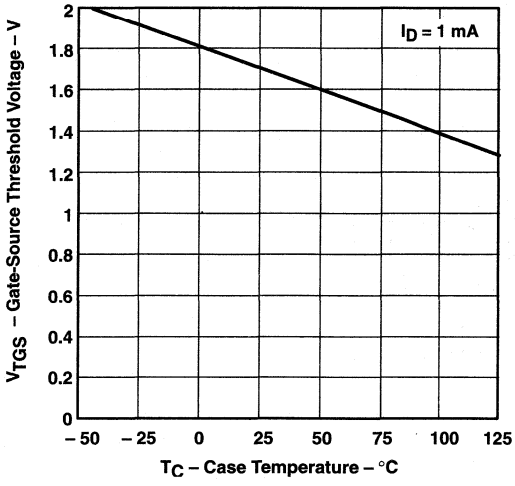


Figure 9

SOURCE-DRAIN DIODE CURRENT
vs
SOURCE-DRAIN VOLTAGE

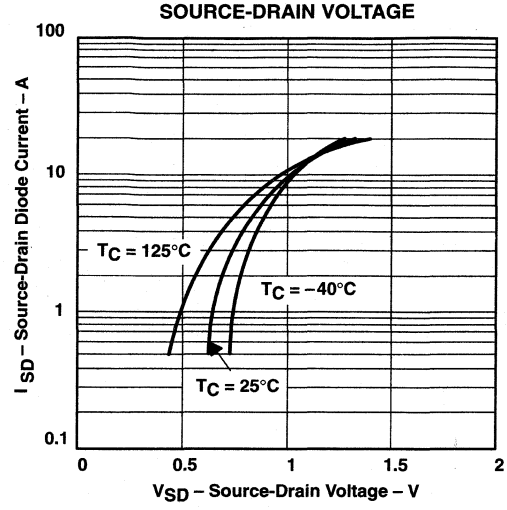


Figure 10

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

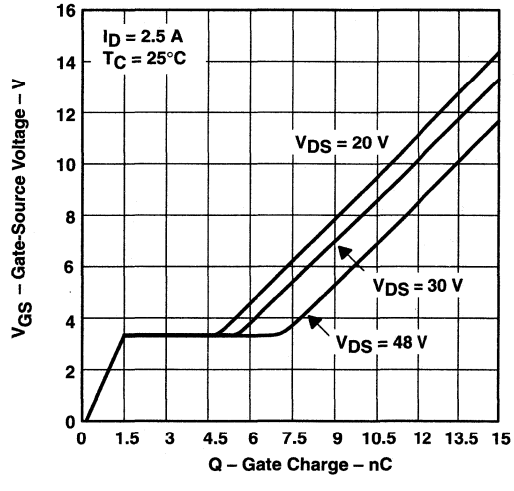


Figure 11

REVERSE RECOVERY TIME
vs
REVERSE di/dt

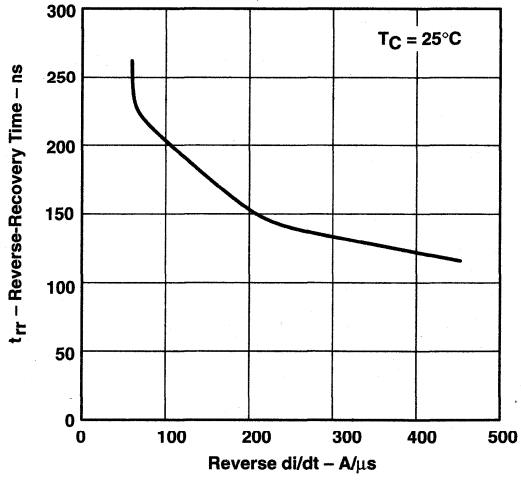


Figure 12

TYPICAL CHARACTERISTICS

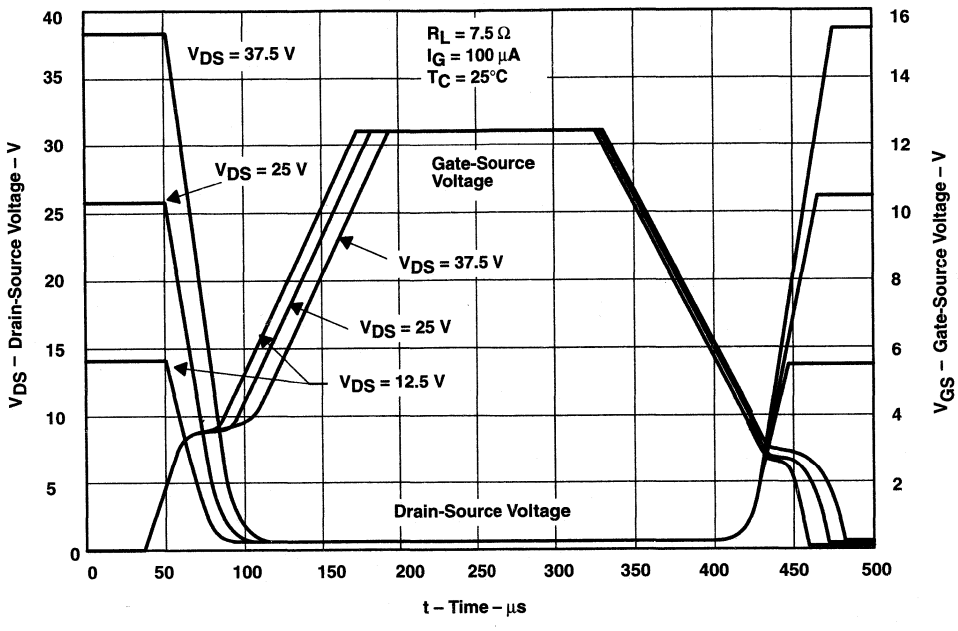


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-SOURCE VOLTAGE

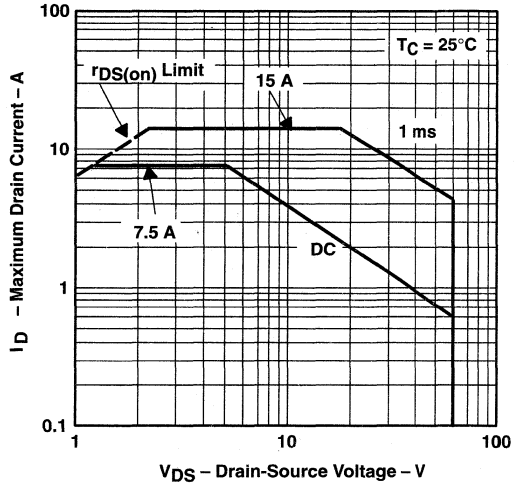


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

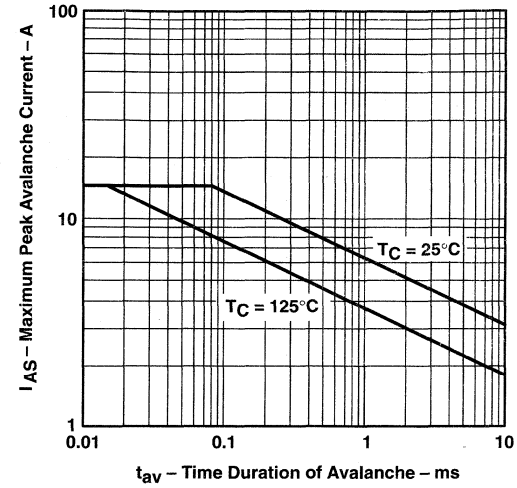
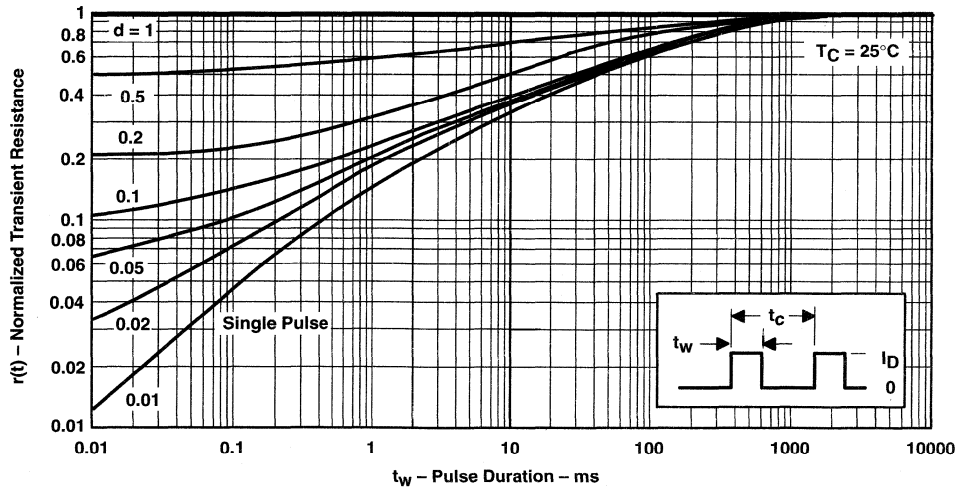


Figure 15

NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE DURATION

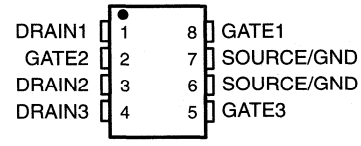


NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

Figure 16

- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 5 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)

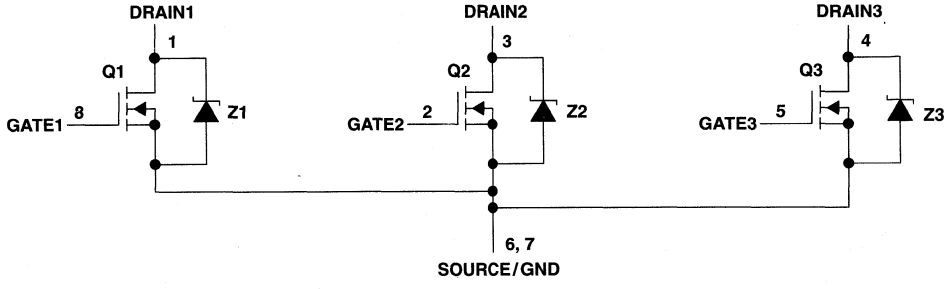


description

The TPIC2302 is a monolithic power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains. The TPIC2302 is offered in a standard 8-pin small-outline surface-mount (D) package.

The TPIC2302 is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 6)	5 A
Single-pulse avalanche energy, T_C = 25°C, E_{AS} (see Figures 4 and 16)	9 mJ
Continuous total power dissipation at (or below) T_C = 25°C	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 10 V, See Notes 2 and 3			0.4	0.475	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3), See Notes 2 and 3			0.9	1.1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.475	Ω
			T_C = 125°C		0.63	0.7	
g_{fs}	Forward transconductance	V_{DS} = 10 V, See Notes 2 and 3	I_D = 0.5 A,	0.85	1.02		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz			115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤ 5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		65		ns
Q_{RR}	Total diode charge			0.03		µC

resistive-load switching characteristics, T_C = 25°C

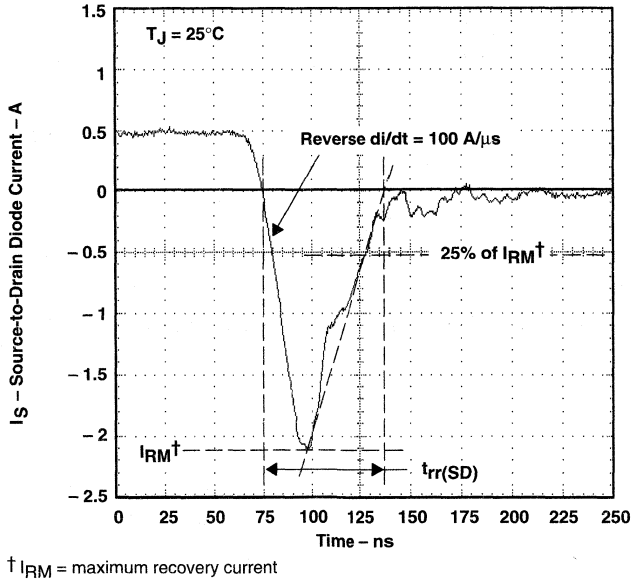
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		21	42	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_{r2}	Rise time			5	10	
t_{f2}	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 10 V, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.3	1.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

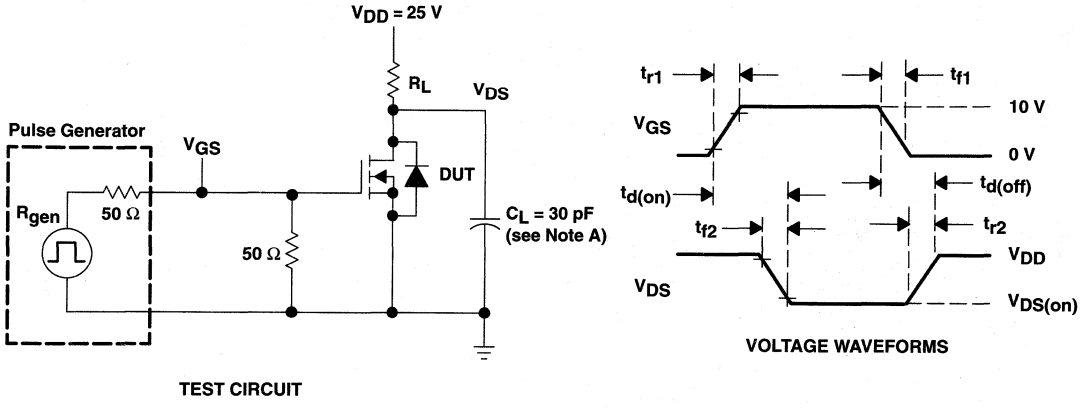
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

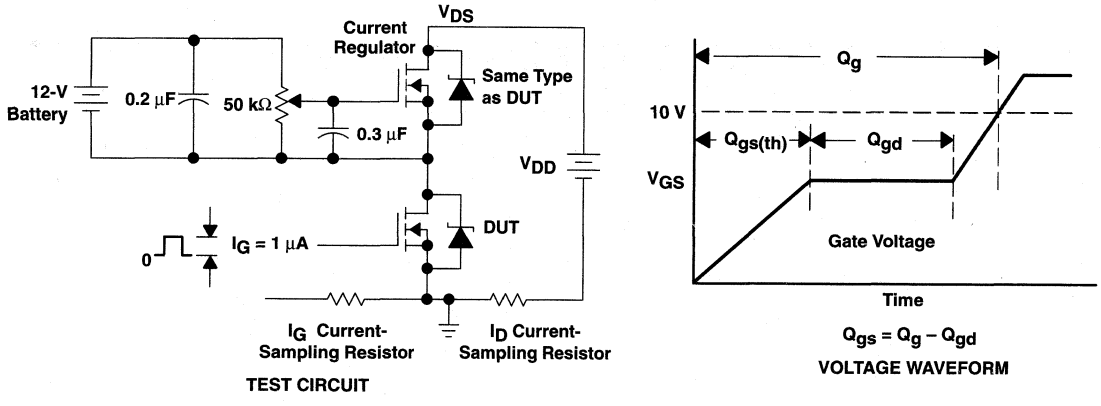


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

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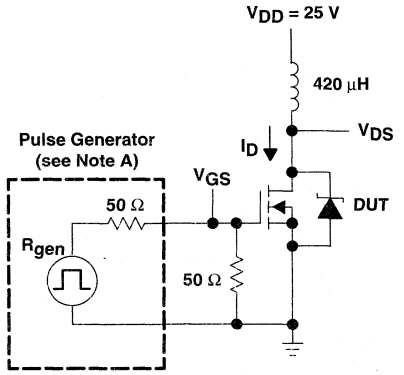
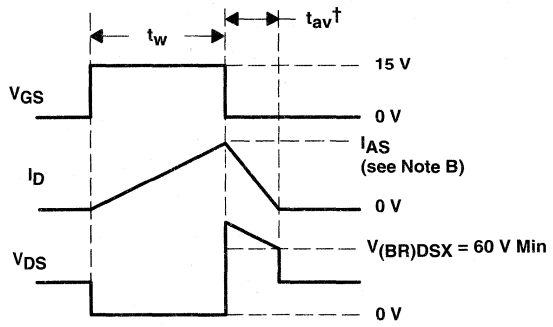
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 9$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

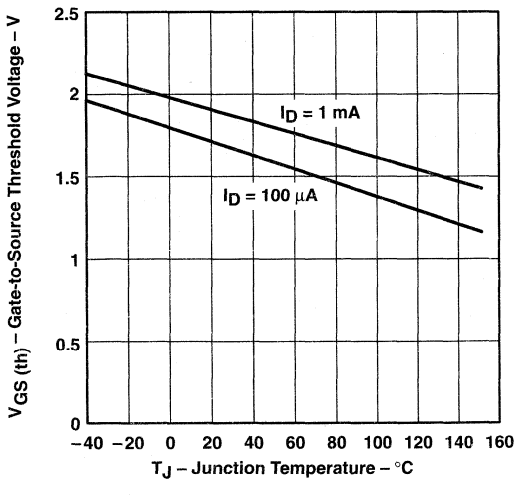


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

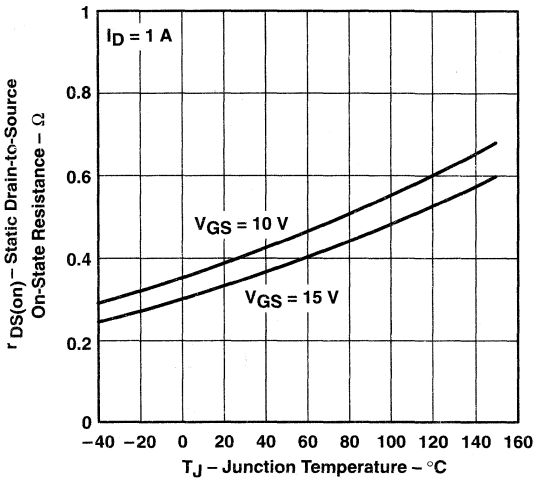


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

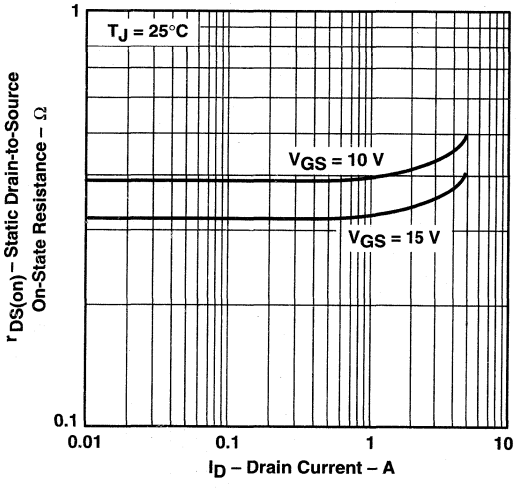


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

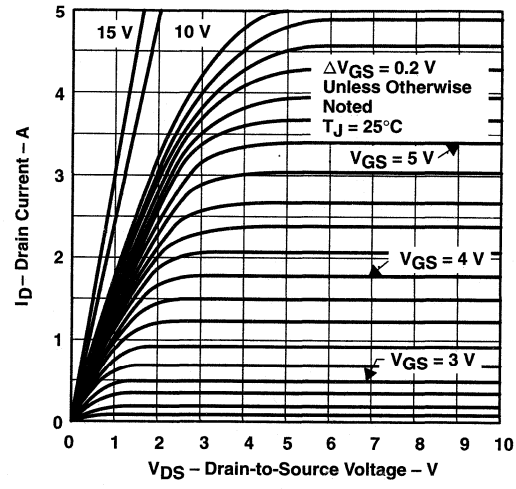


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

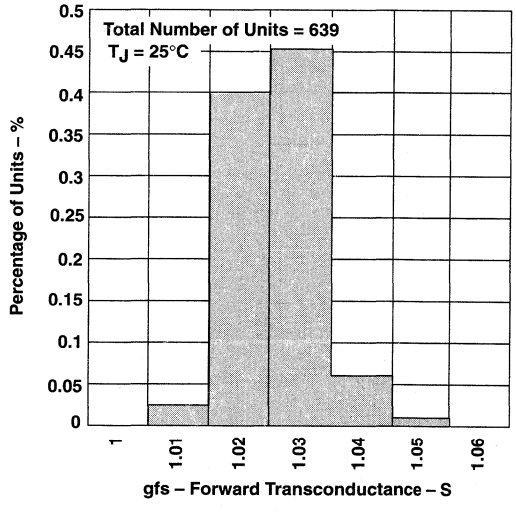


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

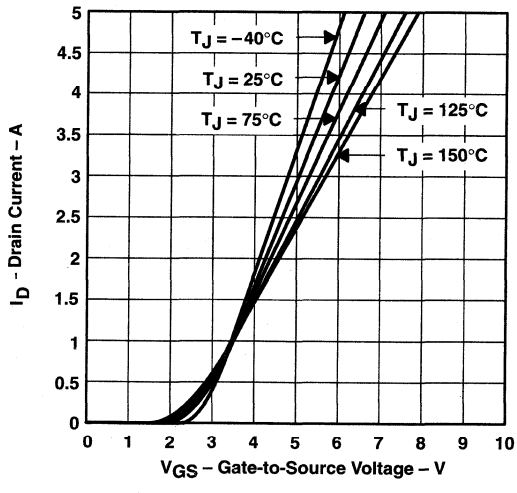


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

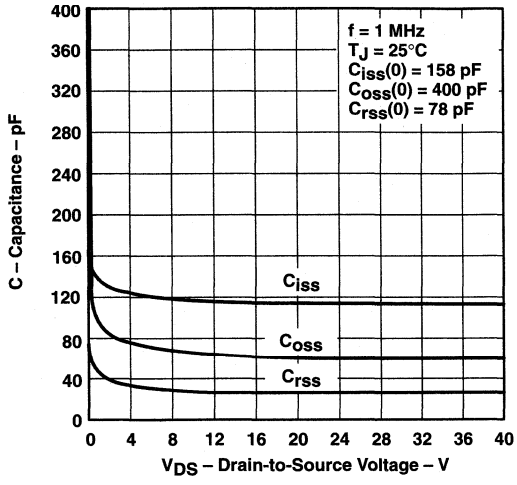


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

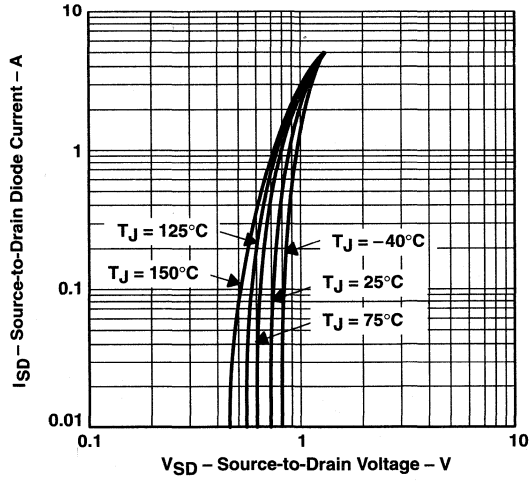


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

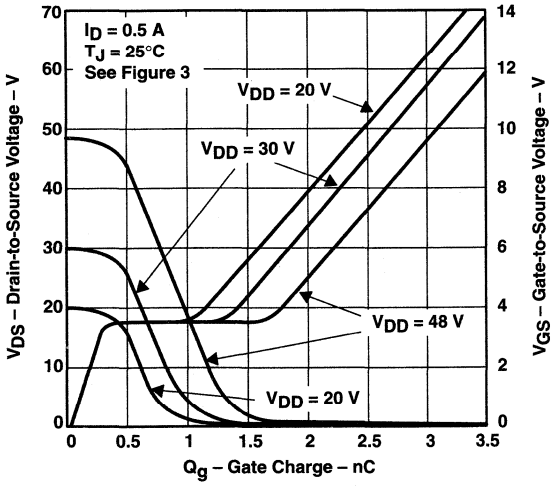


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

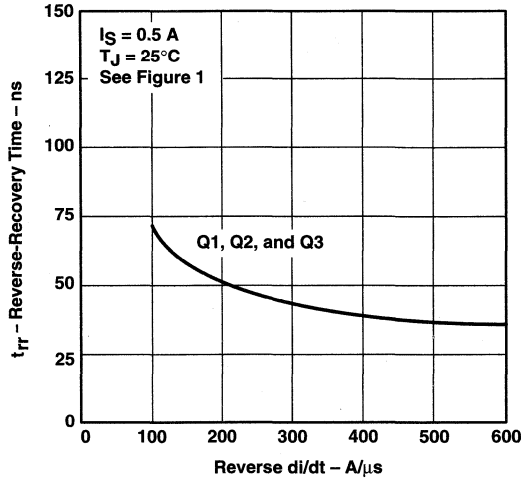
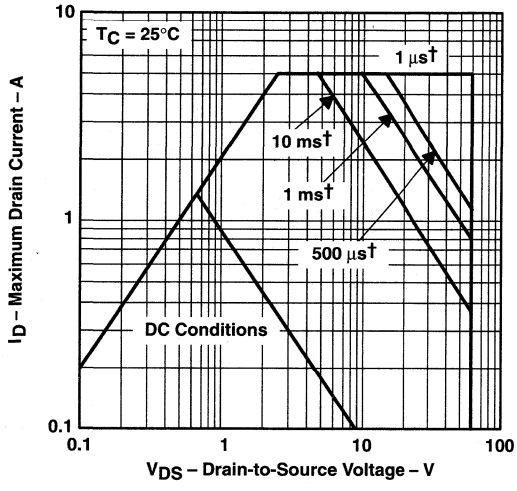


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

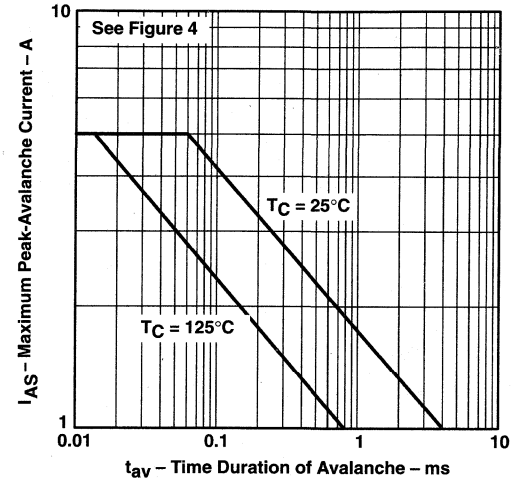
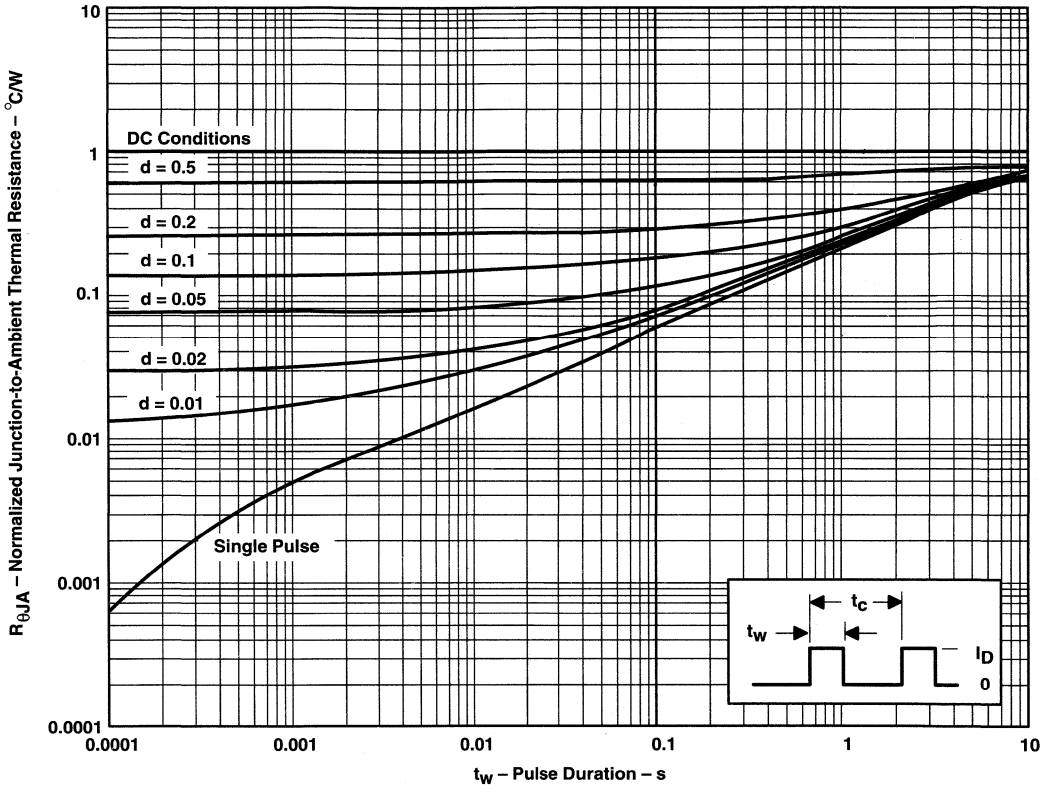


Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

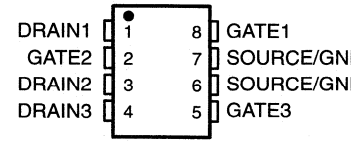
Figure 17

3-CHANNEL COMMON-SOURCE LOGIC-LEVEL POWER DMOS ARRAY

SLIS036A – JUNE 1994 – REVISED OCTOBER 1994

- **Low $r_{DS(on)}$ . . . 0.6 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 2.25 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)

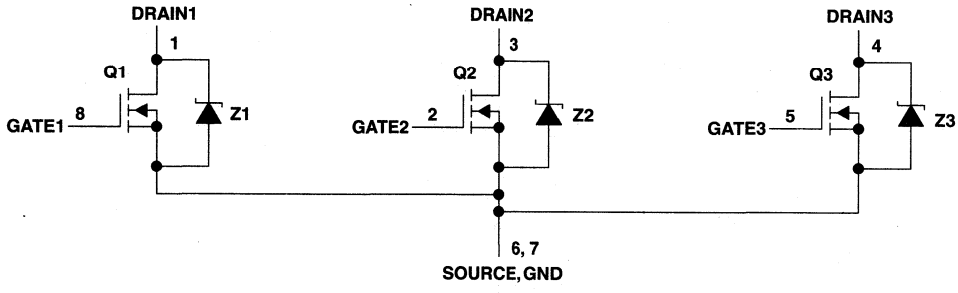


description

The TPIC2322L is a monolithic logic-level power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains.

The TPIC2322L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Gate-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	0.75 A
Continuous source-to-drain diode current, T_C = 25°C	0.75 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	30.4 mJ
Continuous total power dissipation at (or below) T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain to GND breakdown voltage	Drain to GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.75 A, See Notes 2 and 3	V_{GS} = 5 V,		0.45	0.53	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 0.75 A, See Notes 2 and 3 and Figure 12	V_{GS} = 0		0.85	1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 0.75 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.7	Ω
			T_C = 125°C		0.94	1	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 0.5 A,	0.75	0.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C (see schematic diagram)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 0.375 A, di/dt = 100 A/µs,	V_{DS} = 48 V, See Figures 1 and 14		85		ns
Q_{RR}	Total diode charge				0.19		µC

resistive-load switching characteristics, T_C = 25°C

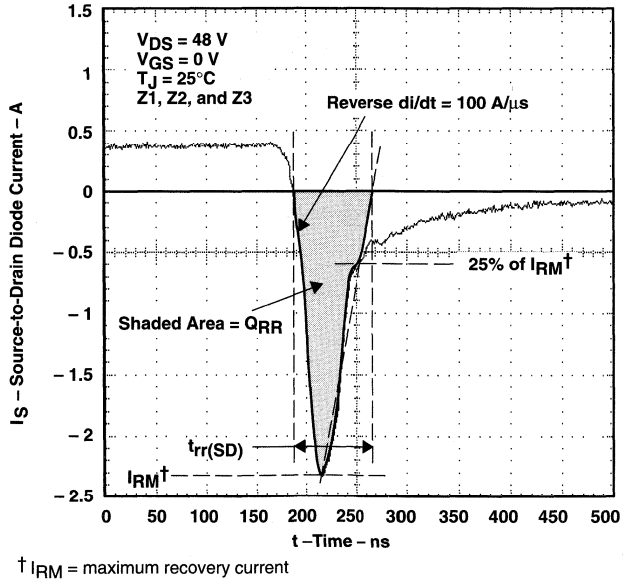
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 67 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		21	42	ns
$t_{d(off)}$	Turn-off delay time			26	52	
t_r	Rise time			14	28	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.375 A, V_{GS} = 5 V, See Figure 3		1.8	2.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.1	1.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		°C/W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

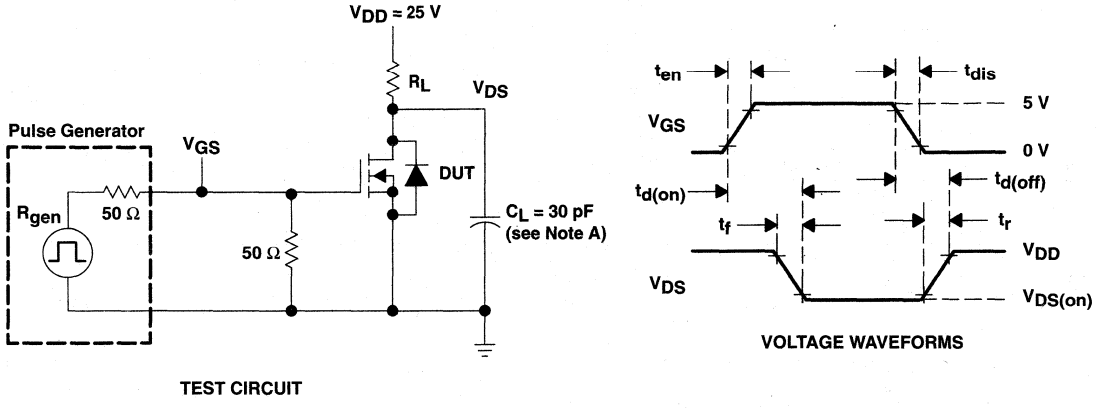
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

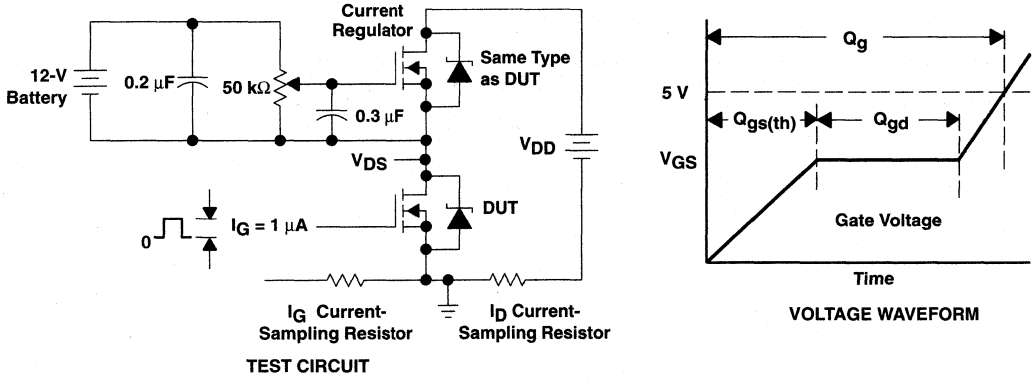
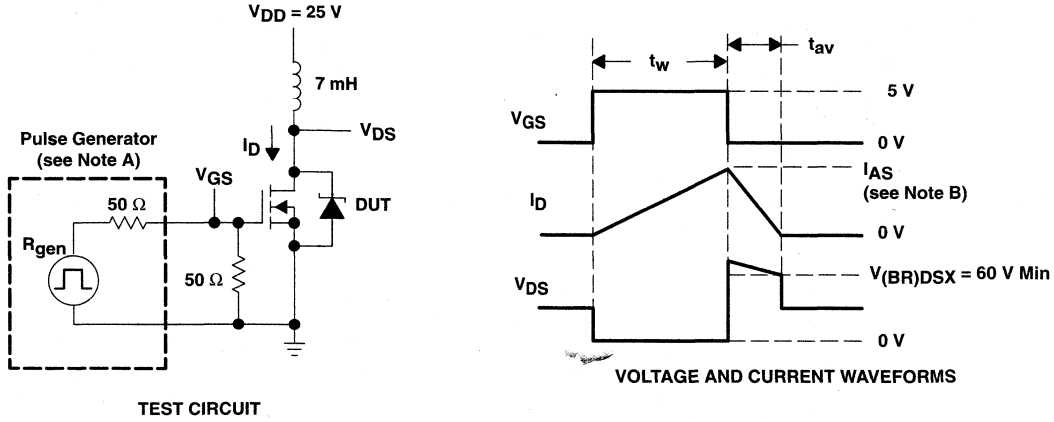


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 30.4$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

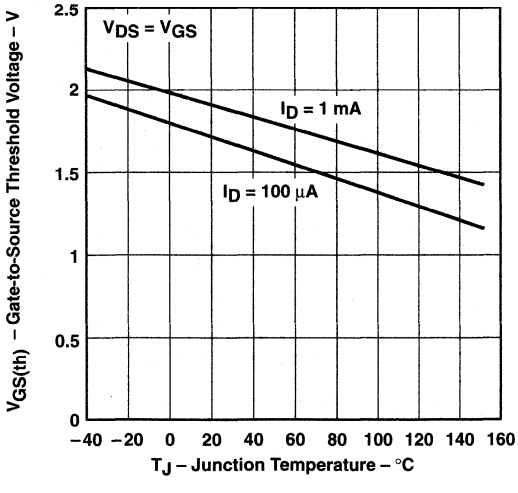


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

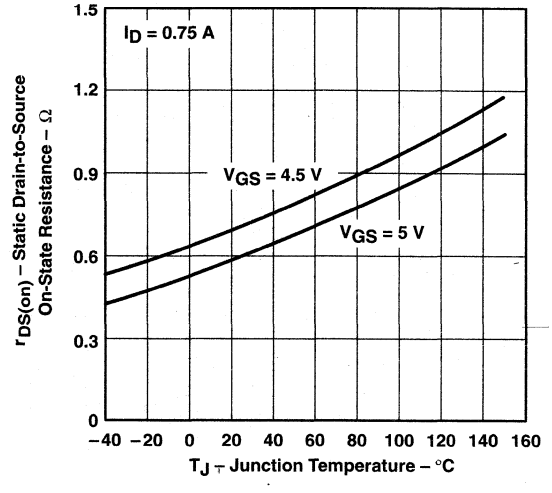


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

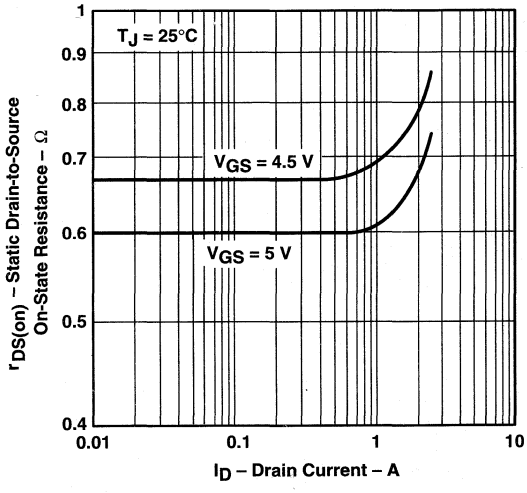


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

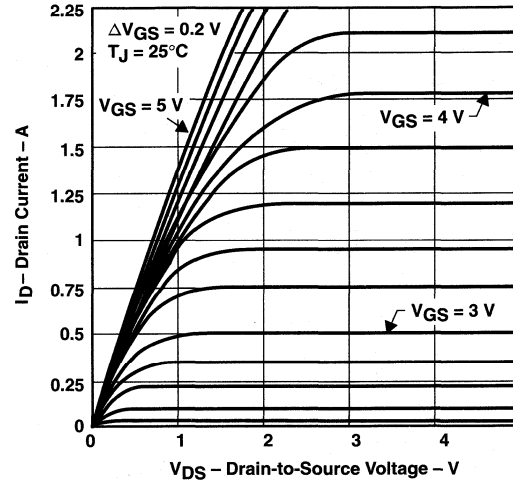


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

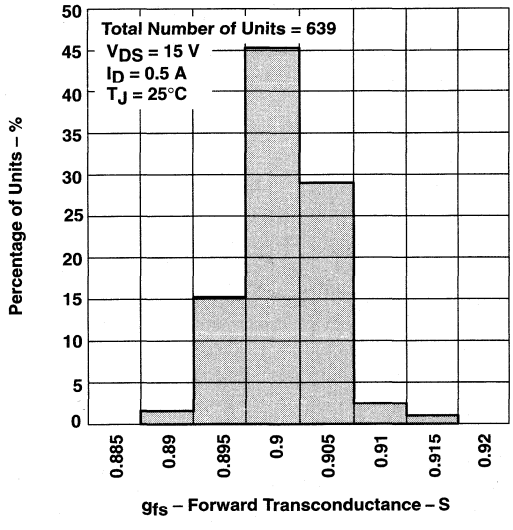


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

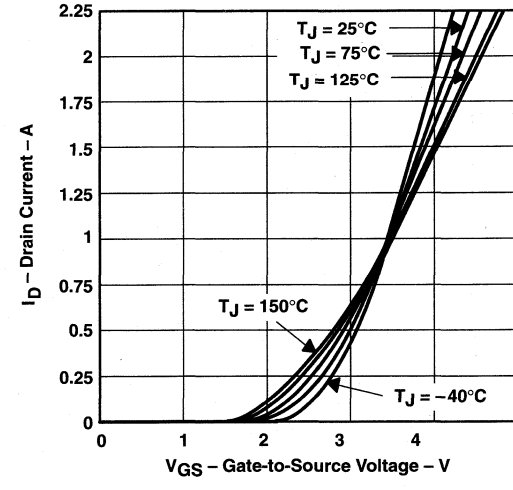


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

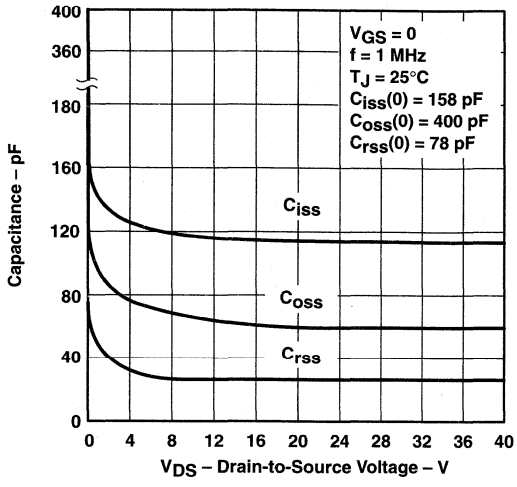


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

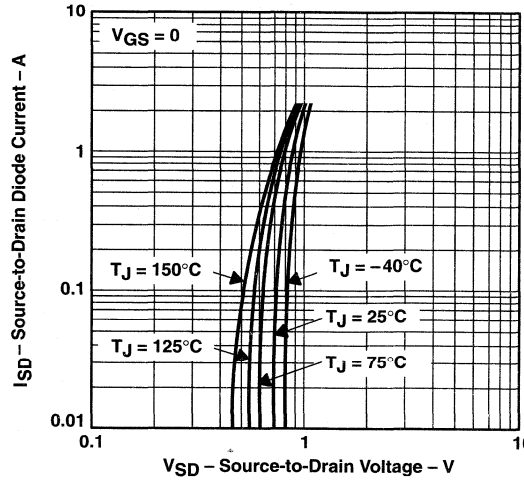


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

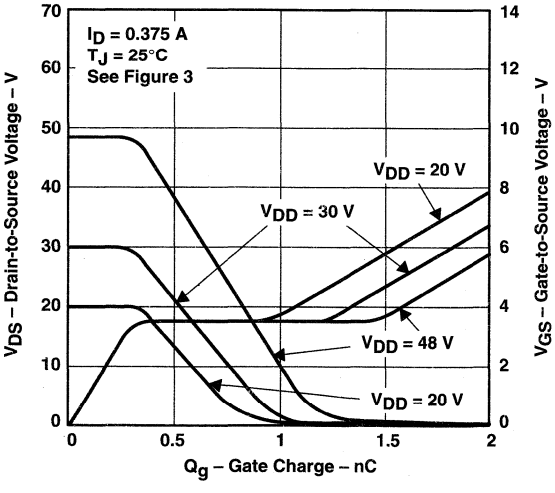


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

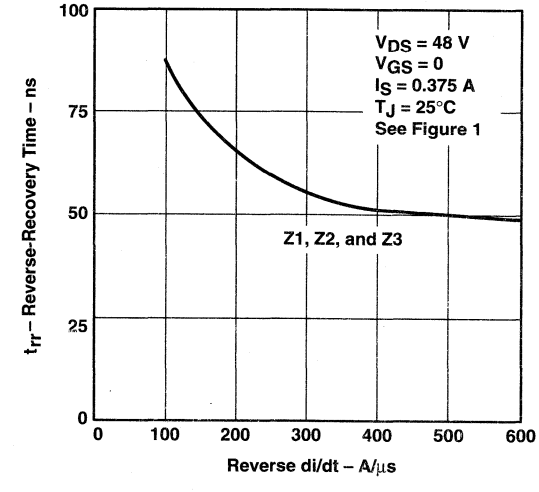
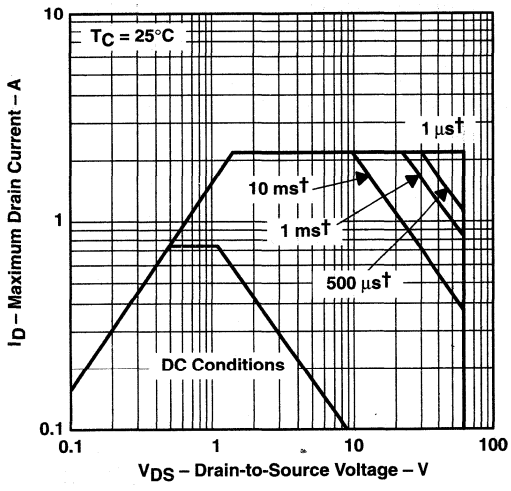


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

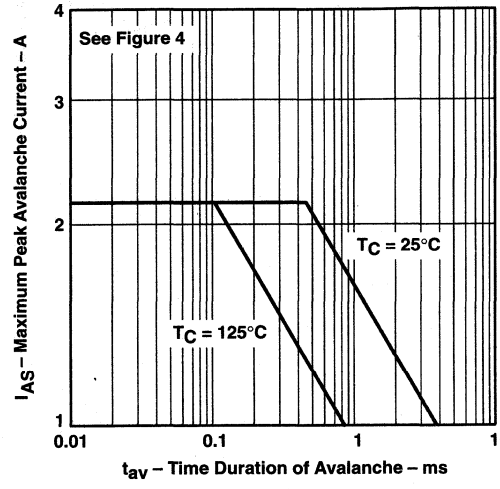
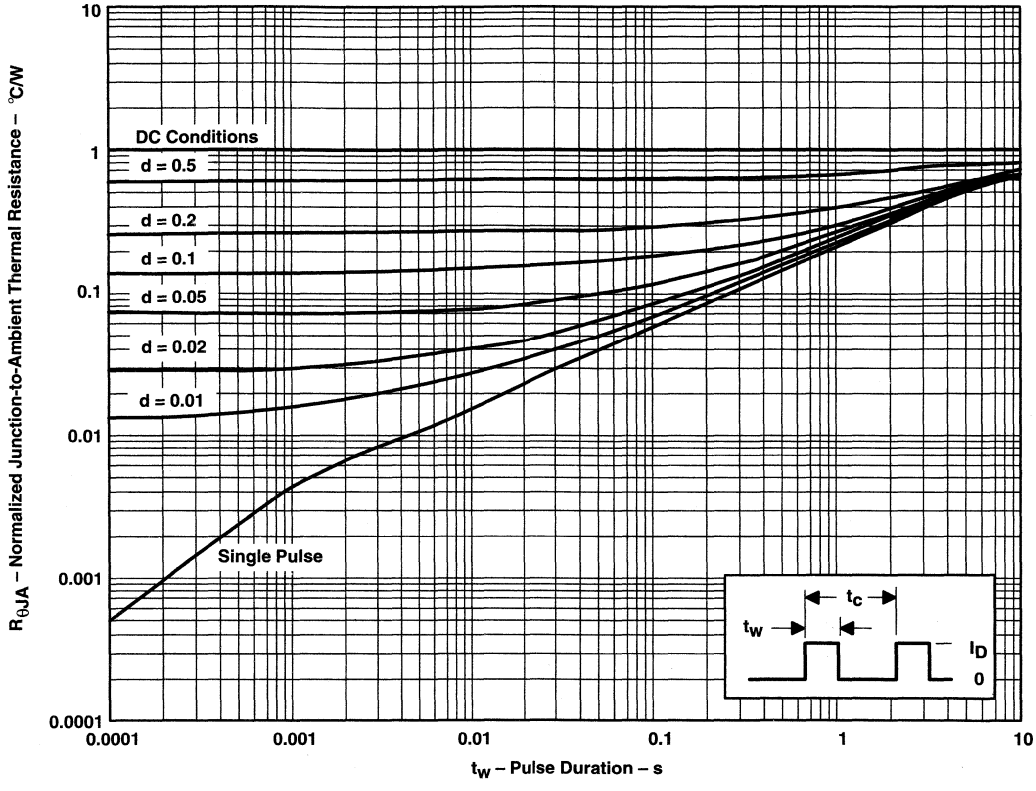


Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



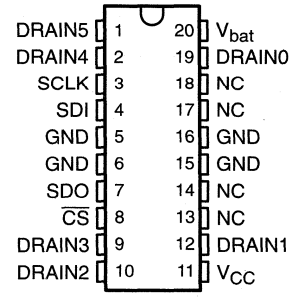
† Device mounted on FR4 printed-circuit board with no heat sink.

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

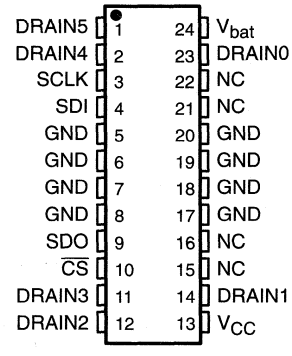
Figure 17

- **Serial Control With Diagnostics**
- **Six Power DMOS Transistor Outputs of 350 mA Continuous Current**
- **Internal 60-V Inductive Load Clamp**
- **Independent ON-State Shorted-Load/Short-to-Battery Fault Detection on All Drain Terminals**
- **Independent OFF-State Open-Load Fault Sense on All Drain Terminals**
- **Transition of Drain Outputs to Low Duty Cycle PWM Mode for Over-Current Condition**
- **Over-Battery-Voltage-Lockout Protection**
- **Over-Temperature Fault Sense and Reporting**
- **Fault Diagnostics Returned Through Serial Output Terminal**
- **Internal Power-On Reset of Registers**
- **CMOS Compatible Inputs With Hysteresis**

NE PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPIC2603 is a monolithic low-side driver which provides serial interface and diagnostics to control six on-board power DMOS switches. Each channel has independent OFF-state open-load sense, ON-state shorted-load/short-to-battery protection, over-battery-voltage protection, and over-temperature sense with fault status reported through the serial interface. The device also provides inductive voltage transient protection for each drain output. The TPIC2603 can be used to drive inductive and resistive loads such as relays, valves, and lamps.

Serial data input (SDI) is transferred through the serial register when $\overline{CS}$ is low on low-to-high transitions of the serial clock (SCLK). Each string of data must consist of 8 or 16 bits of data. A logic high input data bit will turn the respective output channel ON and a logic low data bit will turn it OFF. $\overline{CS}$ must be transitioned high after all of the serial data has been clocked into the device. A low-to-high transition of $\overline{CS}$ will transfer the last six bits of serial data to the output buffer, 3-state the serial data out (SDO) terminal, and re-enable the fault register. Fault data for the device is sent out the SDO terminal. The first bit of the shift register is exclusively OR'ed with the fault registers. When a fault exists, the SDI data is inverted as it is transferred out of SDO. Fault data consists of fault flags for over-temperature (bit 6) and shorted/open-load (bits 0-5) for each of the six output channels. Fault register bits are set or cleared asynchronously, when $\overline{CS}$ is high to reflect the current state of the hardware. The fault must be present when $\overline{CS}$ is transitioned from high to low to be captured and reported in the serial fault data. New faults cannot be captured in the serial register when $\overline{CS}$ is low.

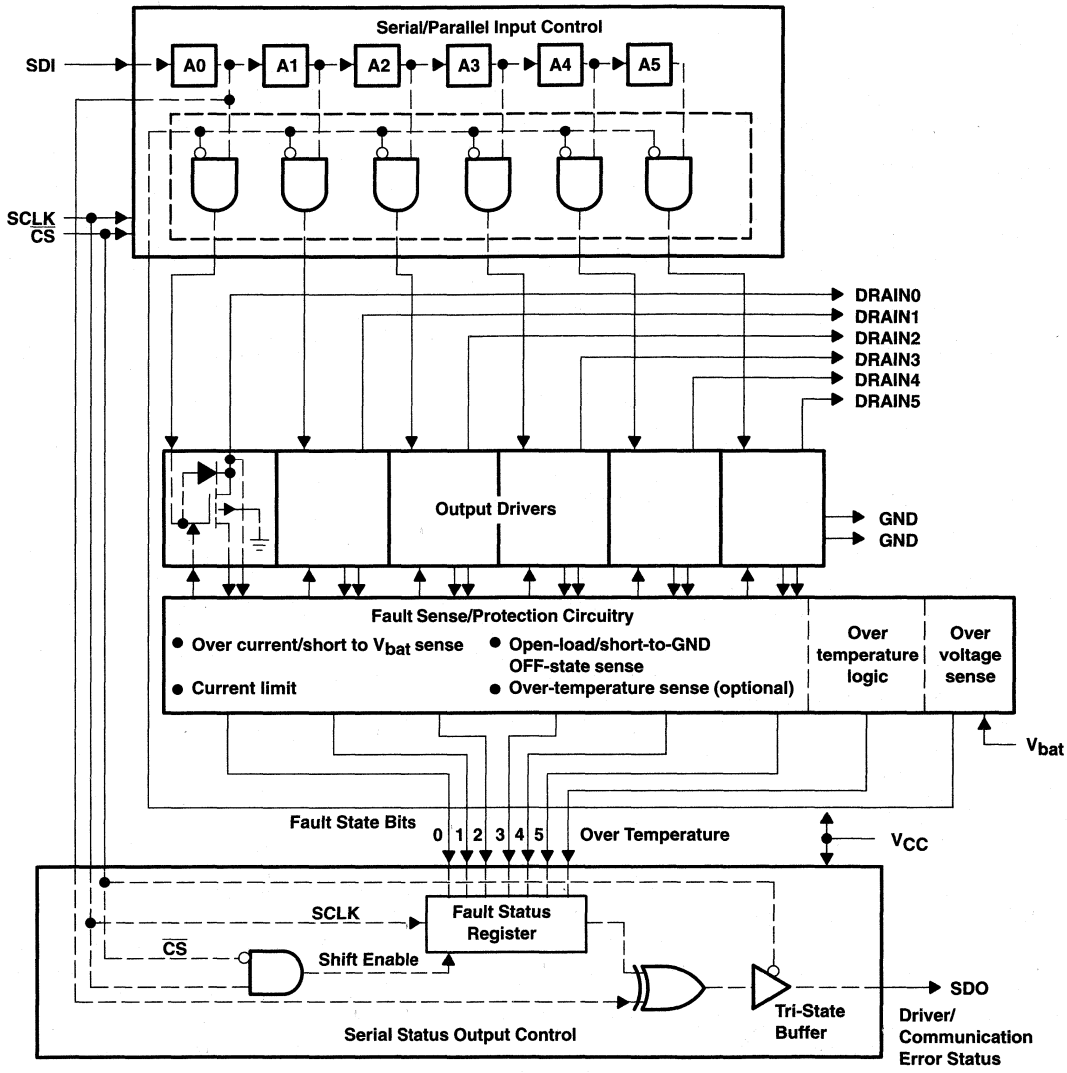
If an over-current or shorted-load fault occurs, the channel will transition into a low duty cycle pulse-width-modulated (PWM) signal as long as the fault is present. More detail on fault detection operation is presented in the device operation section of this data sheet.

The TPIC2603 provides pull-down resistors on all active-high inputs except SCLK. A pull-up resistor is used on $\overline{CS}$.

The TPIC2603 is characterized for operation over the operating case temperature of −40°C to 125°C.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
$\overline{CS}$	8 (10)	I	Chip select. $\overline{CS}$ is an active-low input. Serial communication is enabled by pulling the $\overline{CS}$ terminal low. The $\overline{CS}$ input should only be transitioned when SCLK is low. $\overline{CS}$ has an internal active pull-up and requires CMOS logic level inputs.
DRAIN0 DRAIN1 DRAIN2 DRAIN3 DRAIN4 DRAIN5	19 (23) 12 (14) 10 (12) 9 (11) 2 (2) 1 (1)	O	FET drain outputs. These terminals pull current through the low-side switched loads. They are actively clamped at the peak clamping voltage as defined in the electrical characteristics section of this data sheet.
GND	5, 6, 15, 16 (5, 6, 7, 8, 17, 18, 19, 20)		Ground. These terminals provide circuit ground for the device.
SCLK	3 (3)	I	Serial clock. SCLK clocks the shift register. Serial data is transferred into the serial data input (SDI) port and serial fault data is transferred out of the serial data output (SDO) port of the device on the rising edges of SCLK.
SDI	4 (4)	I	Serial data input. SDI receives serial data from the control device. The serial data transmitted on this terminal is an 8-bit (or 16-bit) control byte with the most significant bit (MSB) being transferred first. The input has an internal active pull-down and requires CMOS logic level inputs. See Figures 2 and 4 for input protocol.
SDO	7 (9)	O	Serial data output. This 3-state output transfers fault data to the control device. The output will remain 3-stated unless the device is selected by a low on chip select ($\overline{CS}$). See Figures 3 and 4 for fault protocol.
V_{bat}	20 (24)		Battery voltage. The output drivers will operate at the battery voltage (V_{bat}) levels as low as 5.5-V. This supply is provided for over-voltage shutdown protection and for added gate-drive capabilities.
V_{CC}	11 (13)		Supply voltage. V_{CC} is connected to the 5-V power supply voltage. The output driver will be able to turn ON at V_{CC} levels as low as 4.5 V.

† Terminal numbers listed in parenthesis are for the 24-pin DW package.

absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)‡

Logic supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Battery supply voltage range, V_{bat} ..... −1.5 V to 60 V
Logic input voltage range, V_I ..... −0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2) ..... 70 V
Continuous drain current, each output, all outputs on, I_{Dn}, T_C = 25°C ..... 350 mA
Pulsed drain current, single output, T_A = 25°C (see Note 3) ..... 2.25 A
Single-pusle avalanche energy, E_{AS} (see Figure 14) ..... 100 mJ
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seocnds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.

PRODUCT PREVIEW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5	5.5	V
Battery supply voltage, V_{bat}	5.5	12	25	V
High-level input voltage, V_{IH}	0.7 V_{CC}		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.3 V_{CC}	V
Operating case tempeature, T_C	−40		125	°C

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{bat}	Battery supply voltage	Normal operation		5.5		25	V
I_{bat}	Battery supply current	V_{CC} = 5 V				5	mA
		V_{CC} = 0 V				50	µA
V_{CC}	Logic supply voltage			4.5		5.5	V
I_{CC}	Logic supply current	All outputs off,	V_{bat} = 5.5 V			5	mA
V_{turnon}	V_{CC} turn-on voltage (logic operational)	V_{bat} = 5.5 V,	Check output functionality			4.5	V
$V_{(OV)}$	Over-battery voltage shutdown	Gate disabled		30		38	V
$V_{hys(ov)}$	Over-battery voltage reset hysteresis			0.4		2	V
$r_{DS(on)}$	Drain-to-source on-state resistance	V_{bat} = 13 V	I_O = 0.35 A, T_C = 25°C		0.7	1	Ω
		V_{bat} = 5.5 V			1.7	2.3	
		V_{bat} = 13 V	I_O = 0.35 A, T_C = 125°C		1.2		
		V_{bat} = 5.5 V			2.7		
I_L	On-state current limit			0.8		5	A
$I_{TM(ov)}$	Over-current sense			0.8		3	A
I_{CS}	Input pull-up current	GND < V_I < 0.7 V_{CC} − $\overline{CS}$		−5	−10	−50	µA
I_{IL}	Input pull-down current	0.3 V_{CC} < V_I < V_{CC},	All other inputs	2.5	10	25	µA
I_{DSX}	Off-state drain current	V_{load} = V_{bat} = 14.5 V		20	40	80	µA
$I_{O(sleep)}$	Output current, sleep-state	V_{bat} < 0.5 V,	V_{CC} < 0.5 V, Load = 14 V			50	µA
V_{OH}	High-level serial output voltage	I_O = 1 mA		0.8 V_{CC}			V
V_{OL}	Low-level serial output voltage	I_O = 1 mA			0.2	0.4	V
I_{oz}	Output current, SDO 3-state	V_{CC} = 5.5 V to 0 V		−10	1	10	µA
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	dc < 1%,	t_w = 100 µs, I_O = 20 mA	52	58	68	V
$T_{(limit)}$	Thermal flag			150	170	185	°C
$T_{(hyst)}$	Thermal flag hyteresis			5	10	15	°C
$V_{(open)}$	Open load detection voltage			0.3 V_{CC}		0.7 V_{CC}	V

PRODUCT PREVIEW

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Clock cycle period pulse duration SCLK	See Figure 1		250	555	ns
$t_{wH(SCLK)}$	Pulse duration SCLK high	See Figure 1		100	248	ns
$t_{wL(SCLK)}$	Pulse duration SCLK low	See Figure 1		100	248	ns
t_{pd1}	Propagation delay from falling edge of $\overline{CS}$ to SDO valid	$\overline{CS}$ = 0.8 V to SDO low impedance (see Figure 1)		150	300	ns
t_{pd2}	Propagation delay from rising edge of $\overline{CS}$ to SDO 3-state	$\overline{CS}$ = 2 V to SDO 3-state		150	200	ns
t_{pd3}	Propagation delay from SCLK to SDO	$\overline{CS}$ < 0.8 V		80	172	ns
$t_{r(SDO)}$	Rise time of SDO	C_{load} = 200 pF		30	50	ns
$t_{f(SDO)}$	Fall time of SDO	C_{load} = 200 pF		30	50	ns
t_{stb}	Short-to-battery/shorted-load/open-load deglitch time	See Figures 5 and 6	25	70	100	µs
$t_{d(on)}$	Turn-on delay time, rising edge of $\overline{CS}$ to drain	V_{bat} = 14 V, R_{load} = 30 Ω	0.4	5	10	µs
$t_{d(off)}$	Turn-off delay time, rising edge of $\overline{CS}$ to drain		0.4	5	15	
$t_{r(drain)}$	Rise time of drain terminal		0.4	5	10	
$t_{f(drain)}$	Fall time of drain terminal		0.4	5	10	
$f_{(SCLK)}$	Serial clock frequency		1.8	4		MHz
$t_{cyc(ref)}$	Short-to-battery sense cycle time	See Figure 5	1.6	4	6.4	ms
t_{wsense}	Short-to-battery sense pulse duration	See Figure 5	25	70	100	µs
t_{su1}	Setup to/from the fall edge of $\overline{CS}$ to the rising edge of SCLK	See Figure 1		150	200	ns
$t_{su(SDI)}$	Setup time, SDI to SCLK	See Figure 1		25	55	ns
$t_{h(SDI)}$	Hold time, SDI after SCLK	See Figure 1		10	55	ns

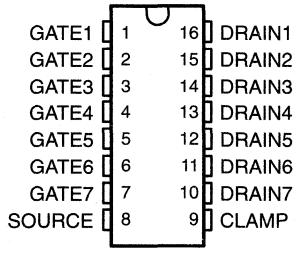
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			50	°C
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			10	°C

PRODUCT PREVIEW

- **Seven 0.5-A Independent Output Channels**
- **Integrated Clamp Diode With Each Output**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Avalanche Energy . . . 22 mJ**

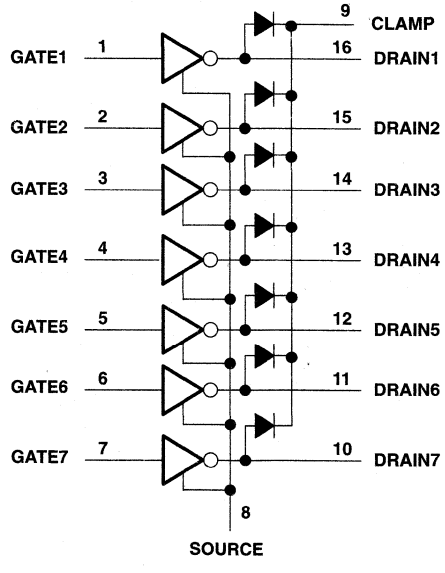
N PACKAGE
(TOP VIEW)



description

The TPIC2701 is a monolithic power DMOS transistor array that consists of seven independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains. The TPIC2701 is pin-for-pin functionally compatible with the Texas Instruments ULN2001A through ULN2004A.

logic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Clamp-drain voltage, V_{CD}	60 V
Continuous source-drain diode current	0.5 A
Pulsed drain current, each output, I_D (see Note 1 and Figure 17)	3 A
Pulsed clamp current, I_{CL} (see Note 1 and Figure 18)	3 A
Continuous drain current, each output, all outputs on	0.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	22 mJ
Continuous total dissipation at (or below) T_A = 25°C (see Note 2)	1.4 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 11 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 0.5 A, V_{GS} = 15 V, See Notes 3 and 4			0.25	0.4	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Forward drain-source on-state resistance	V_{GS} = 15 V, I_D = 0.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C		0.5	0.8	Ω
			T_C = 125°C		0.8	1.3	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 3 and 4		0.5	0.8		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			105		pF
C_{oss}	Short-circuit output capacitance, common source				65		
C_{rss}	Short-circuit reverse transfer capacitance, common source				15		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts with a single output transistor conducting.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 0.5 A, V_{GS} = 0		0.9	1.4	V
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 25 A/µs, See Figure 1		165		ns
Q_{RR}	Total source-drain diode charge			250		nC

clamp diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward on-voltage	I_F = 0.5 A		1	1.5	V
V_{BR}	Breakdown voltage	I_R = 1 µA	60			V
I_R	Reverse leakage current	V_R = 48 V		0.05	1	µA
$t_{rr(CD)}$	Reverse-recovery time	I_F = 0.1 A, di/dt = 25 A/µs, V_{CD} = 48 V, See Figure 1		90		ns
Q_{RR}	Total source-drain diode charge			100		nC

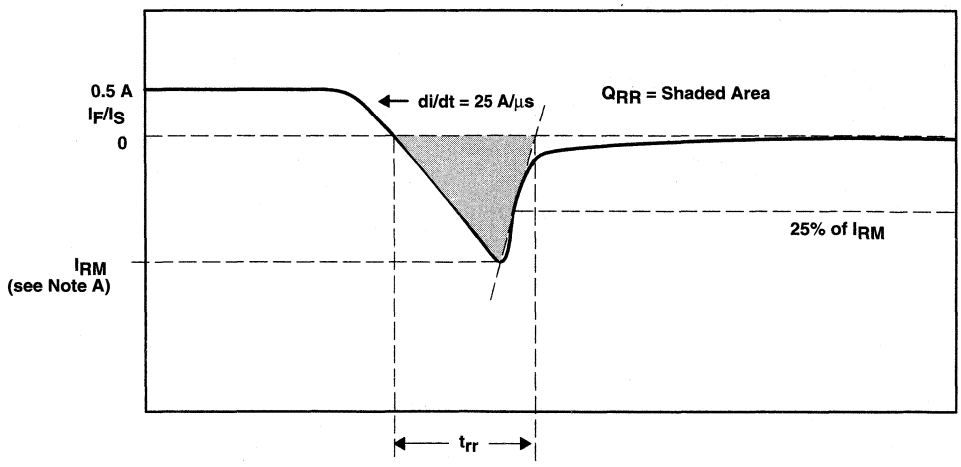
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 100 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		10		ns
$t_{d(off)}$	Turn-off delay time			30		
t_r	Rise time			15		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.25 A, V_{GS} = 10 V, See Figure 3		2.8	3.6	nC
Q_{gs}	Gate-source charge			1.6	2	
Q_{gd}	Gate-drain charge			1.2	1.6	

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			90	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain and Clamp Diodes

PARAMETER MEASUREMENT INFORMATION

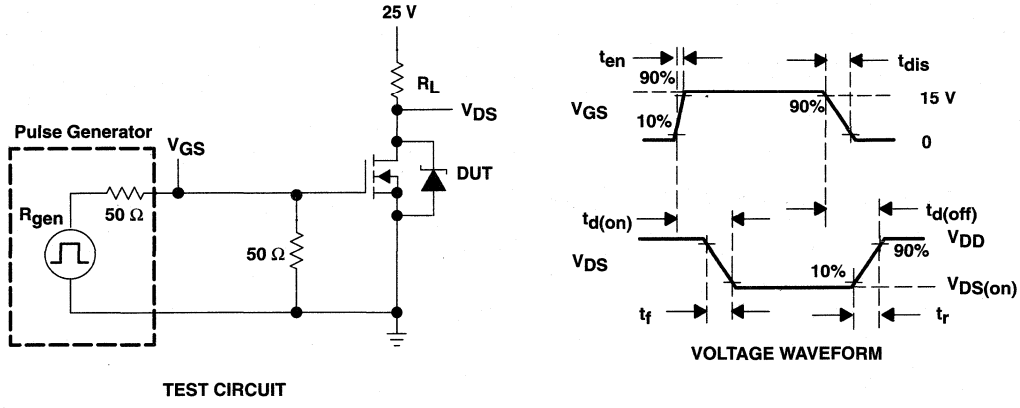


Figure 2. Resistive Switching

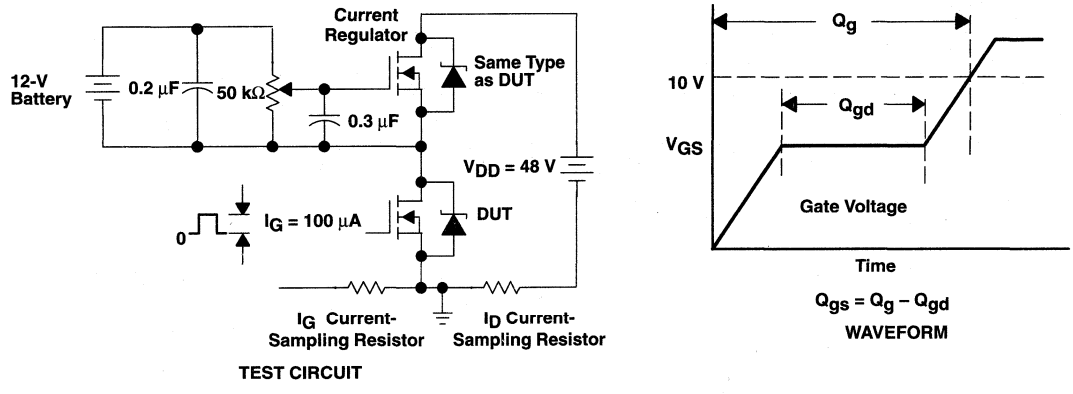
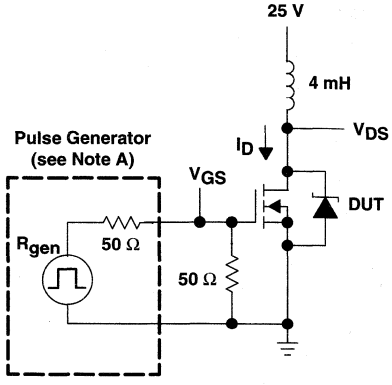
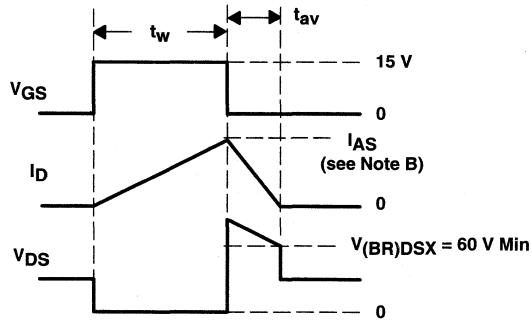


Figure 3. Gate Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

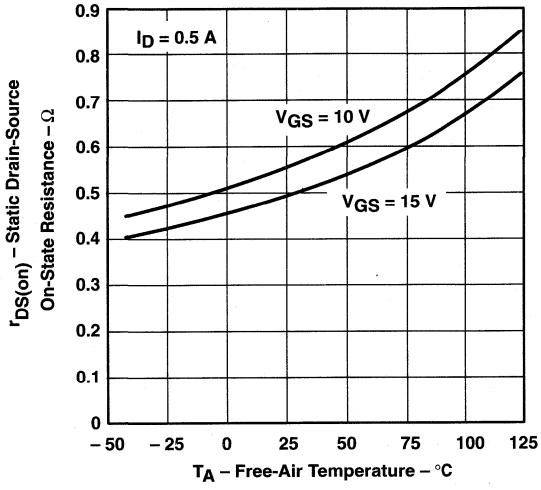


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

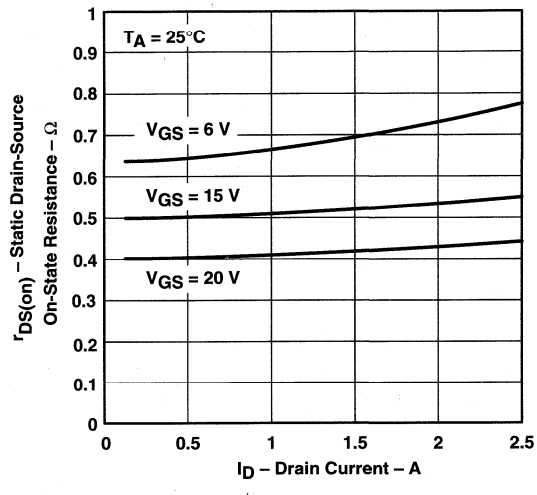


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

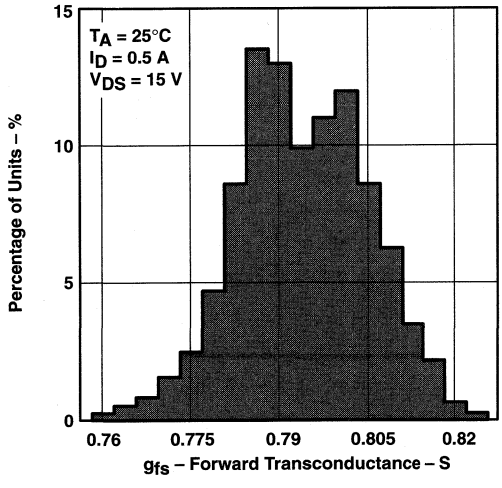


Figure 7

DRAIN-TO-SOURCE CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

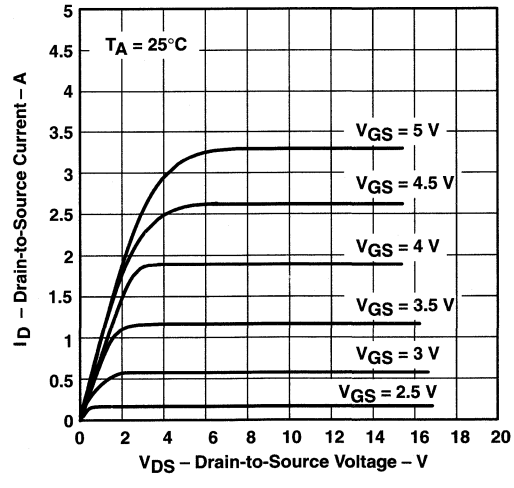


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

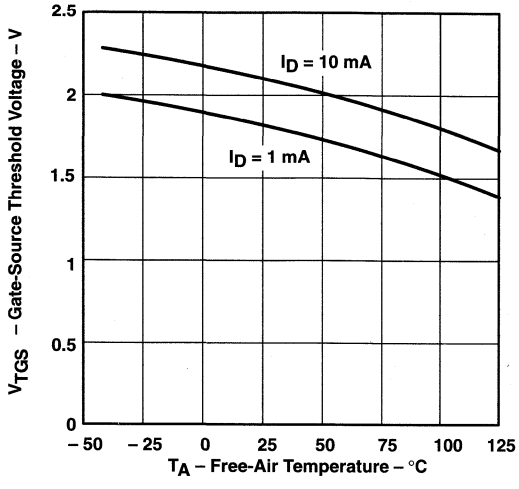


Figure 9

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

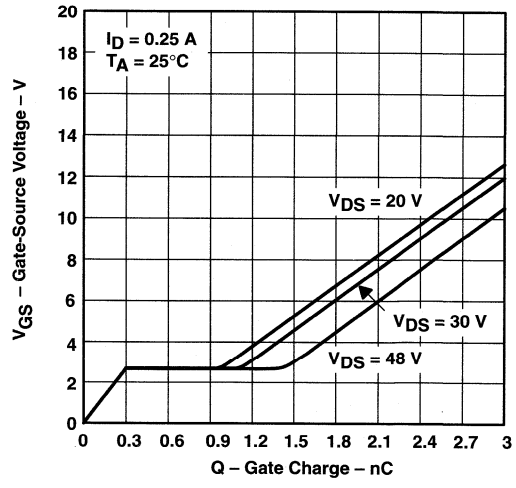


Figure 10

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN DIODE VOLTAGE

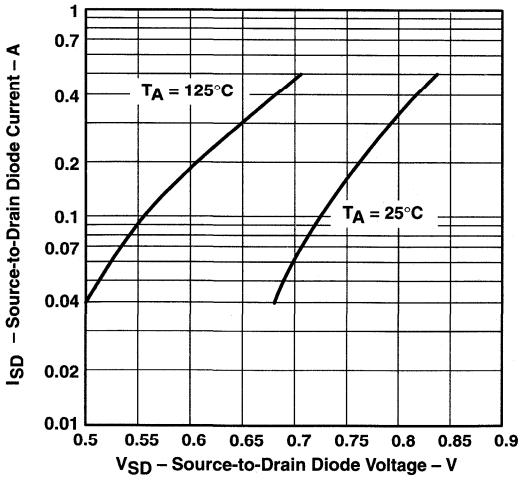


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN DIODE VOLTAGE

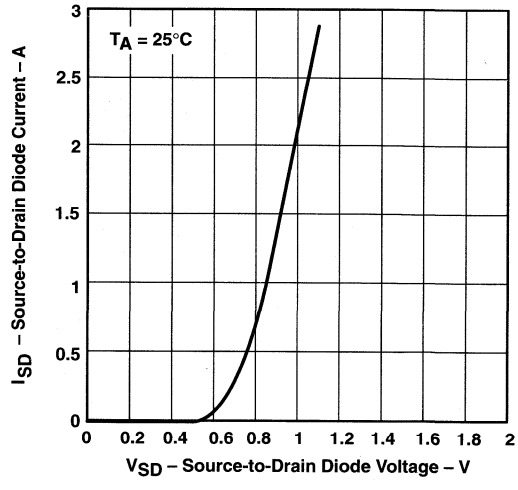


Figure 12

TYPICAL CHARACTERISTICS

CLAMP-DIODE CURRENT vs CLAMP-DIODE VOLTAGE

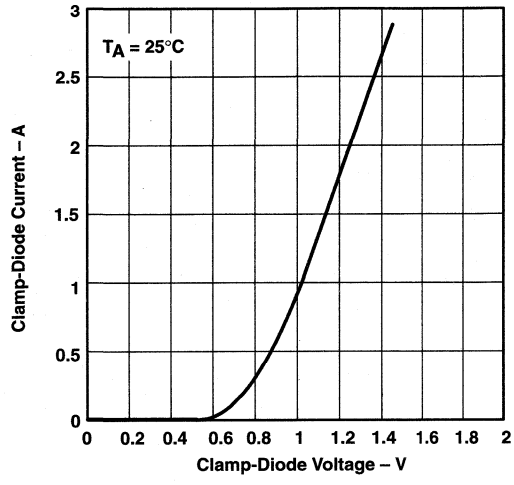


Figure 13

CLAMP-DIODE REVERSE RECOVERY TIME vs REVERSE di/dt

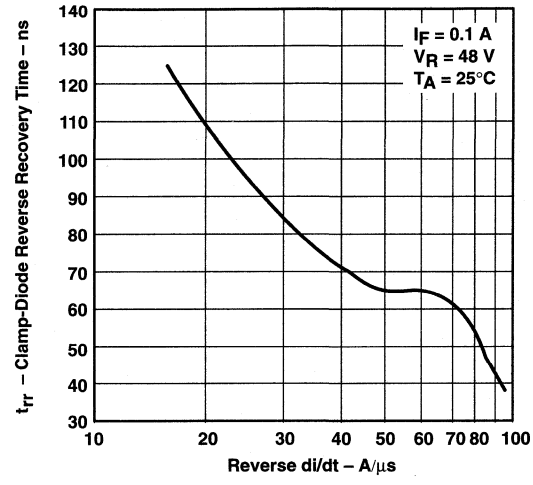
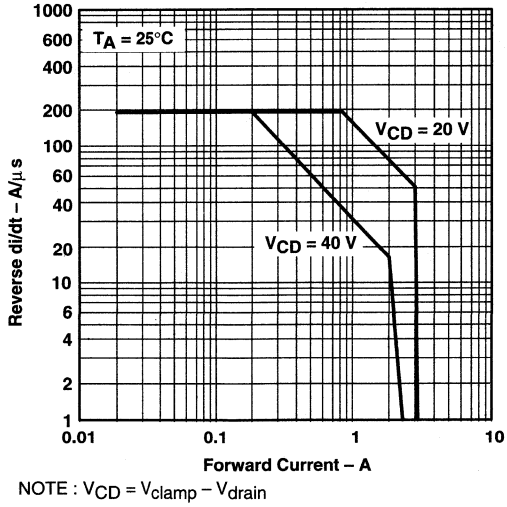


Figure 14

REVERSE di/dt vs FORWARD CURRENT



NOTE : $V_{CD} = V_{clamp} - V_{drain}$

Figure 15

TYPICAL CHARACTERISTICS

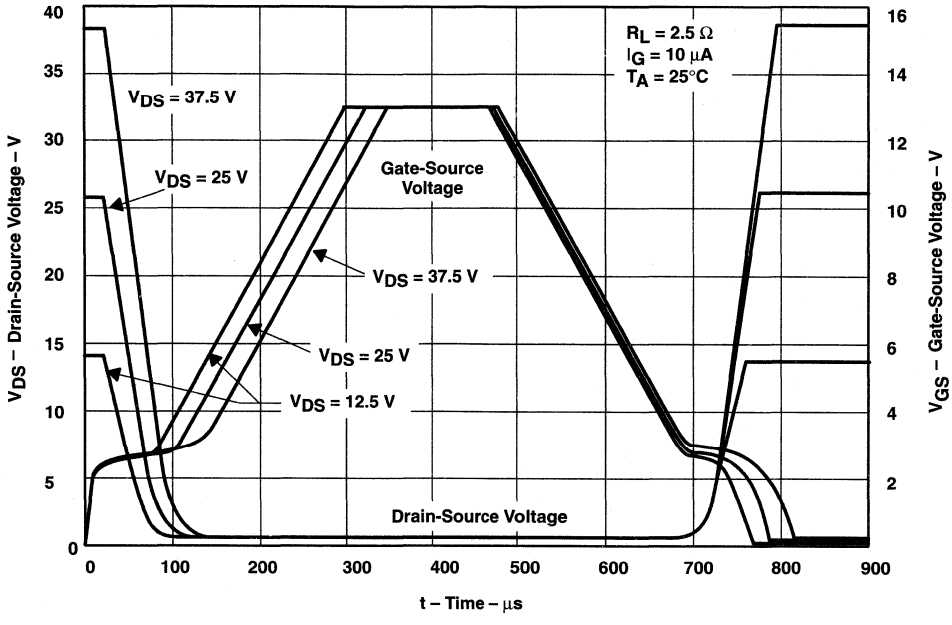


Figure 16. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DUTY CYCLE

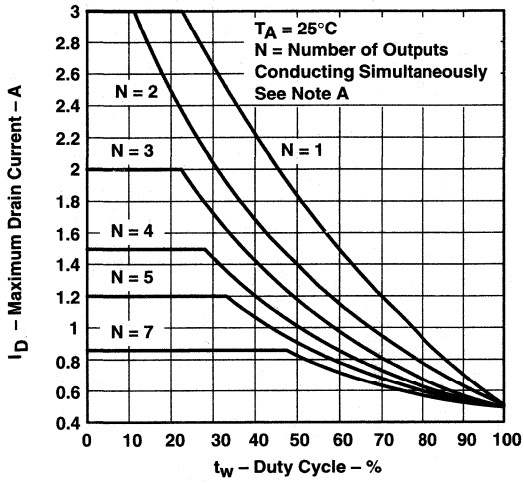


Figure 17

MAXIMUM CLAMP-DIODE CURRENT vs DUTY CYCLE

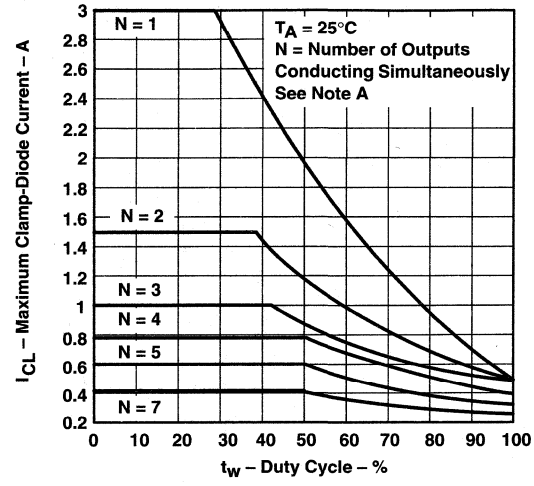
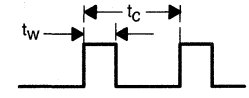


Figure 18



NOTE A: For Figures 17 and 18, $d = t_W/t_C = 10\ ms / t_C$, where t_W and t_C are defined by the following:

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

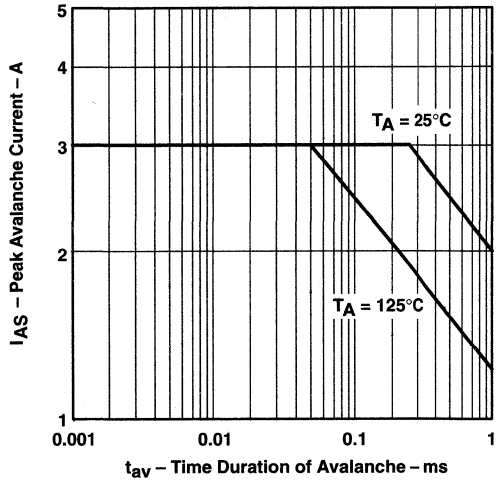


Figure 19

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

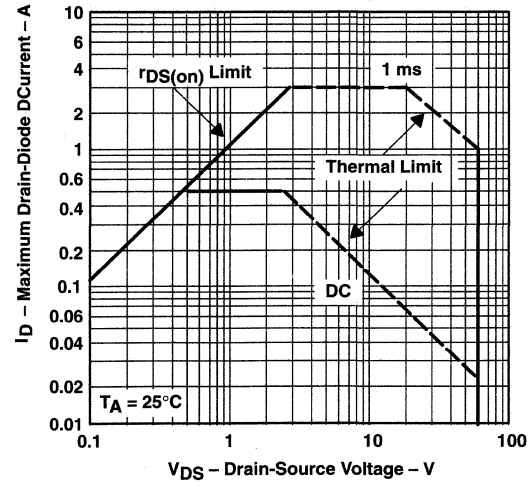
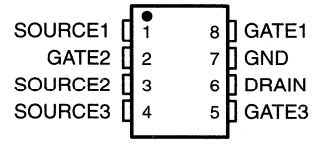


Figure 20

- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 5 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)

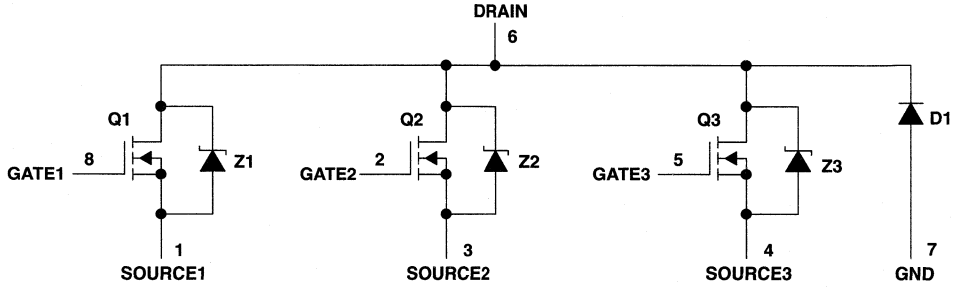


description

The TPIC3302 is a monolithic power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources. The TPIC3302 is offered in a standard eight-pin small-outline surface-mount (D) package.

The TPIC3302 is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1 A
Continuous source-to-drain diode current	1 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 6)	5 A
Single-pulse avalanche energy, T_C = 25°C, E_{AS} (see Figure 4)	9 mJ
Continuous total power dissipation at (or below) T_C = 25°C	0.95 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 10 V, See Notes 2 and 3			0.4	0.475	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A, See Notes 2 and 3			2		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0, See Notes 2 and 3			0.9	1.1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.475	Ω
			T_C = 125°C		0.63	0.7	
g_{fs}	Forward transconductance	V_{DS} = 10 V, See Notes 2 and 3	I_D = 0.5 A,	0.85	1.02		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz			115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, di/dt = 100 A/µs,	V_{DS} = 48 V, See Figure 1		35		ns
Q_{RR}	Total diode charge				0.03		µC

GND-to-drain diode characteristics, T_C = 25°C (see schematic, D1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 0.5 A, di/dt = 100 A/µs,	V_{DS} = 48 V, See Figure 1		90		ns
Q_{RR}	Total diode charge				0.2		µC

resistive-load switching characteristics, T_C = 25°C

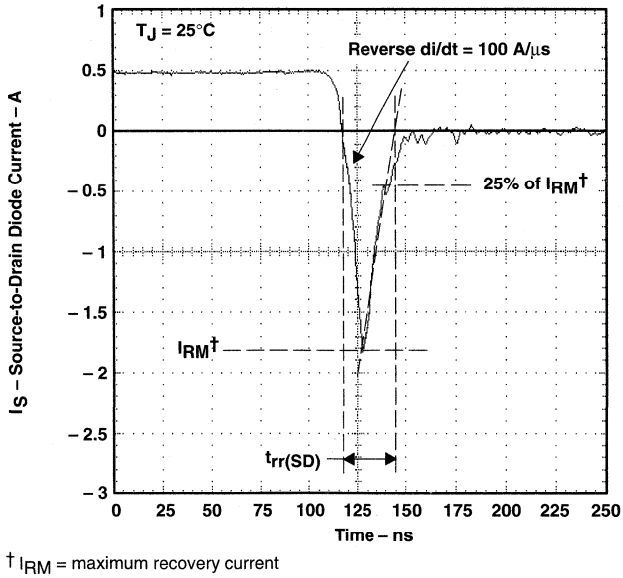
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		21	42	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_r	Rise time			5	10	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 10 V, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.3	1.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

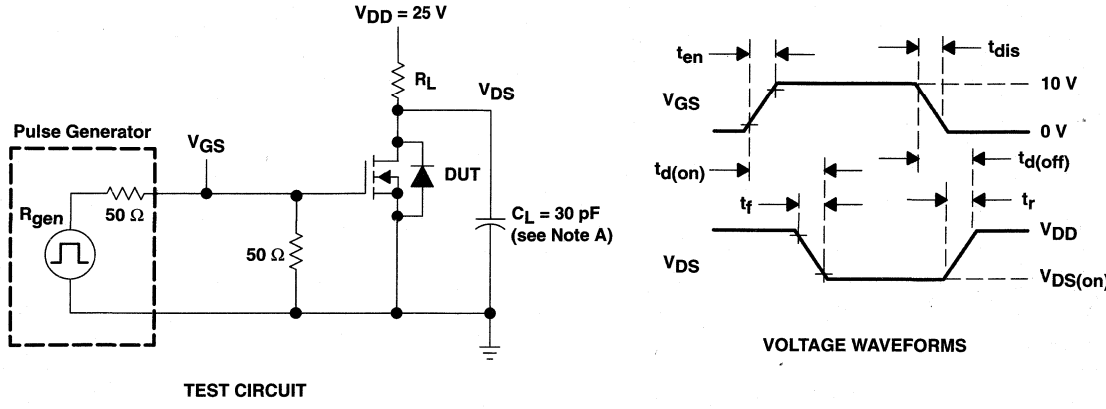
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

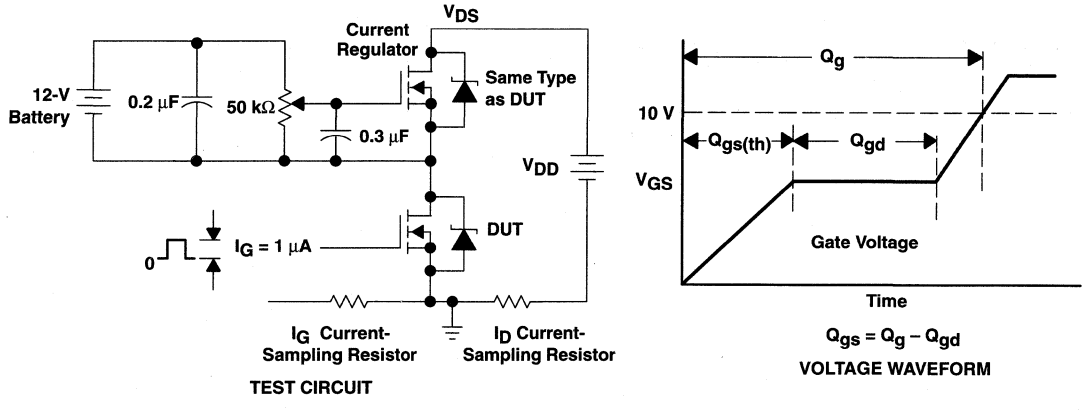
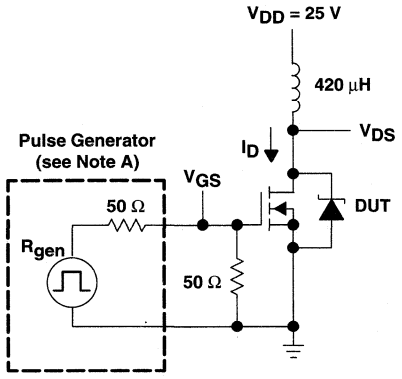
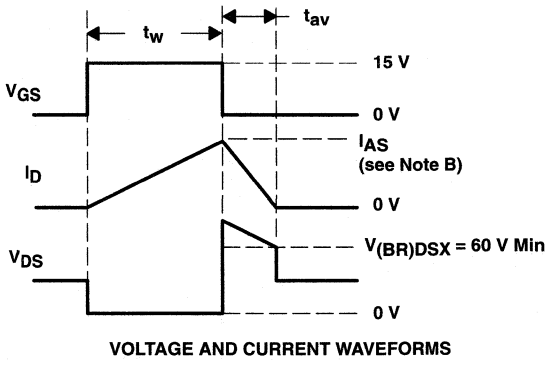


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 9$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

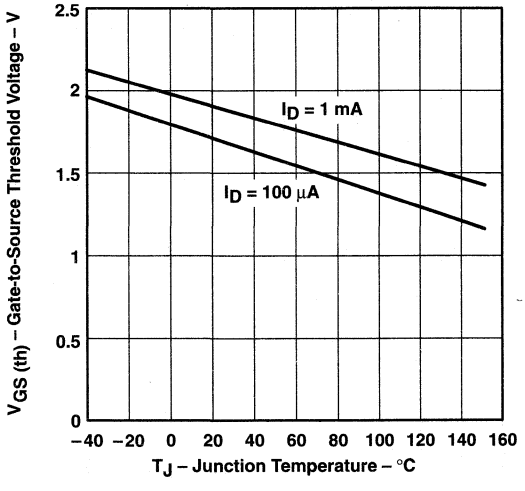


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

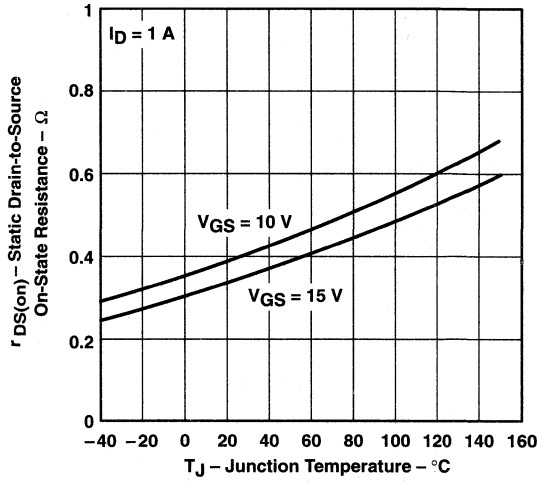


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

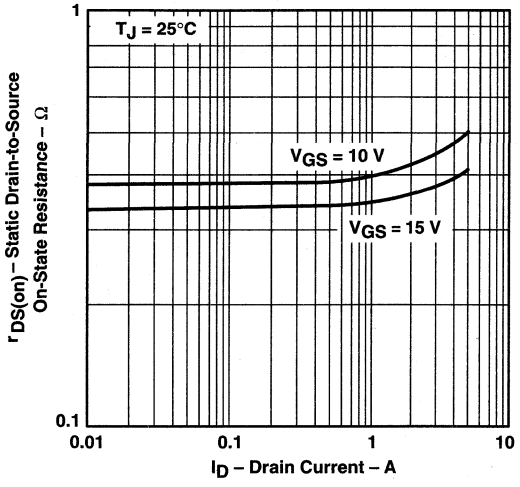


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

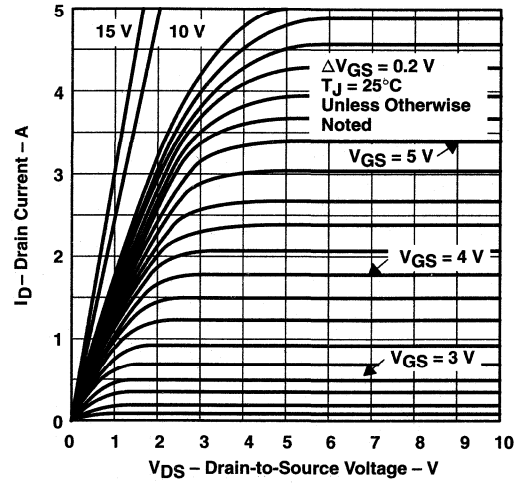


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

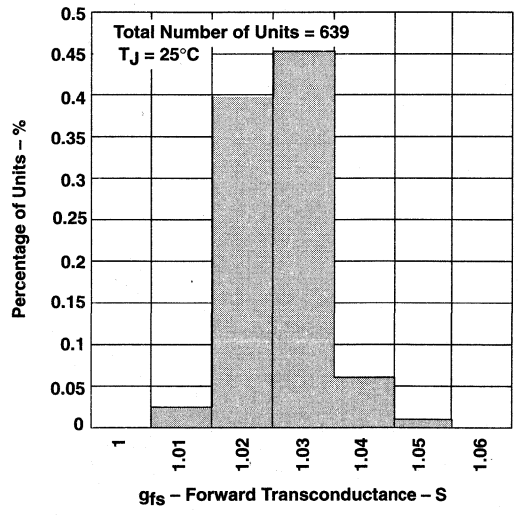


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

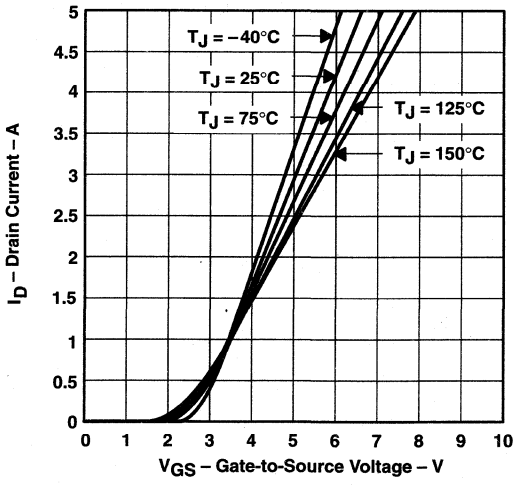


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

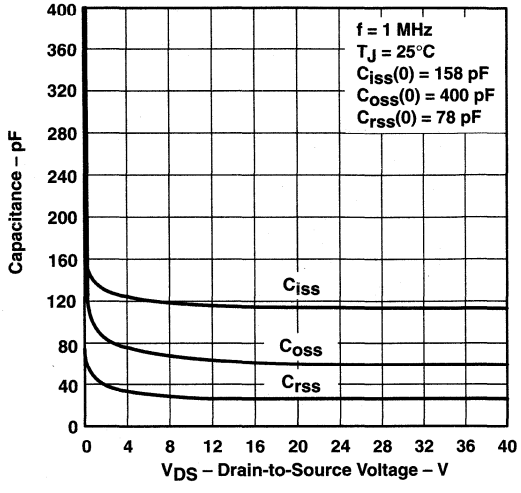


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

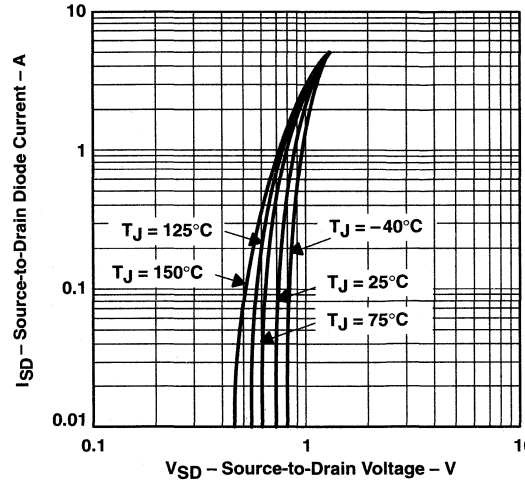


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

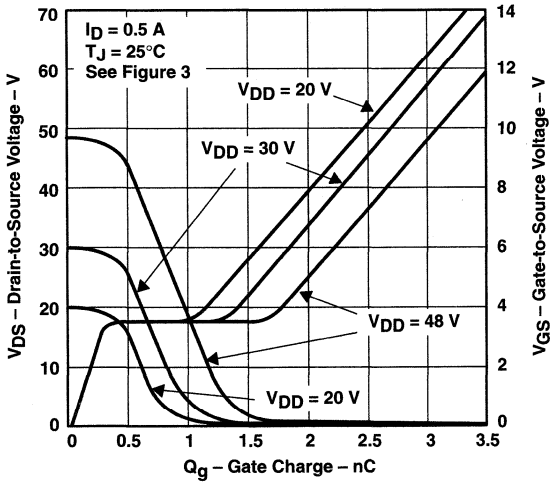


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

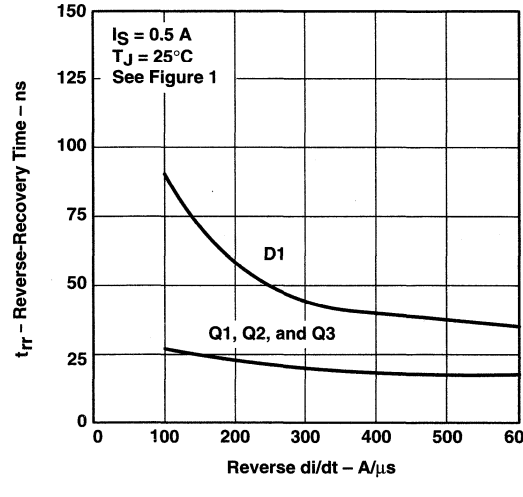
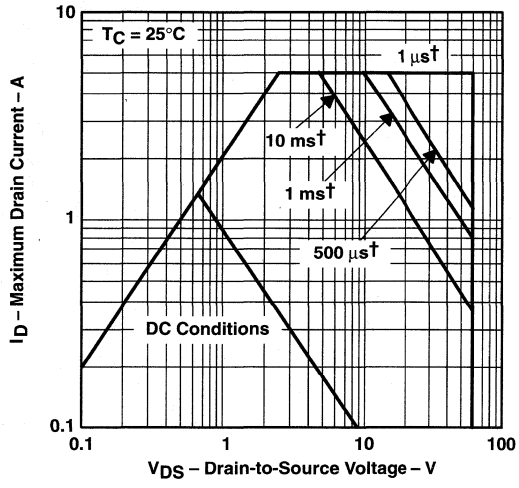


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

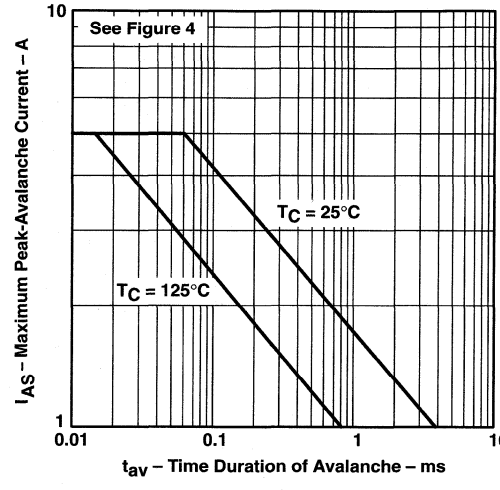
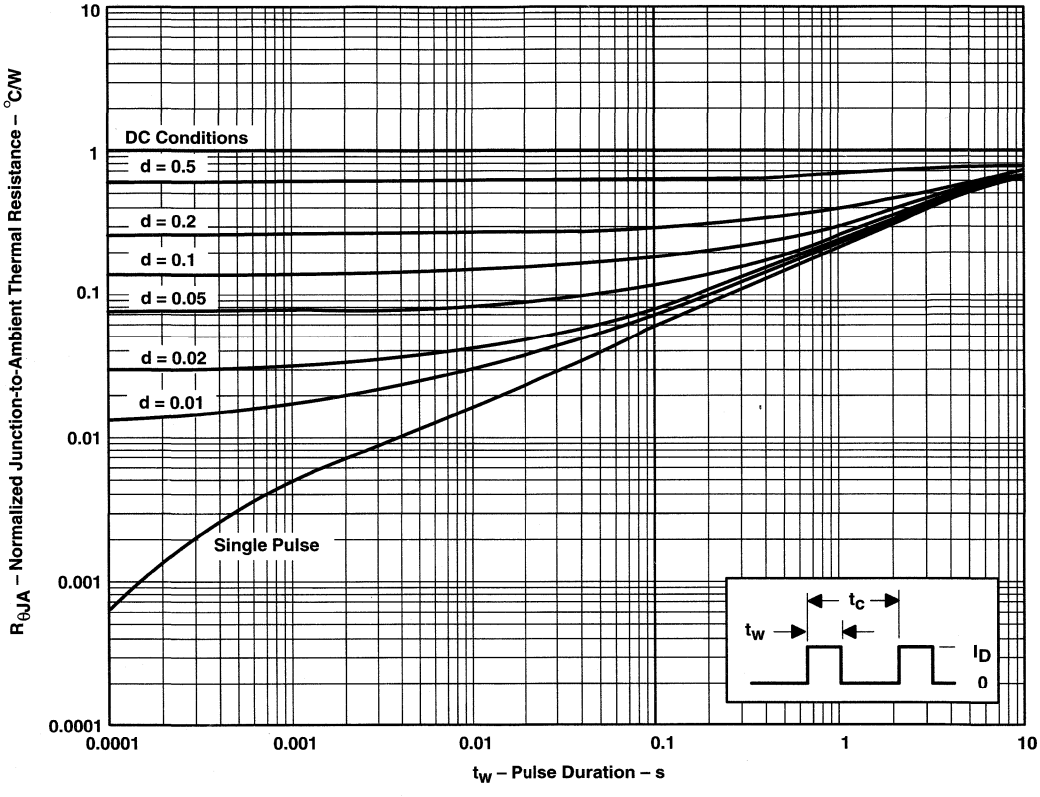


Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



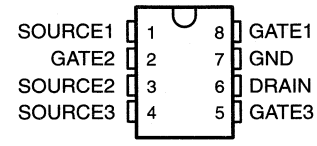
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 17

- Low $r_{DS(on)}$ . . . 0.6 Ω Typ
- High-Voltage Outputs . . . 60 V
- Pulsed Current . . . 2.25 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

D PACKAGE
(TOP VIEW)

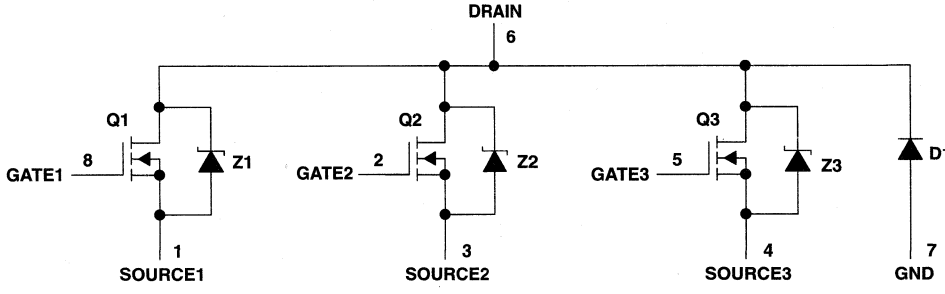


description

The TPIC3322L is a monolithic logic-level power DMOS transistor array that consists of three isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources.

The TPIC3322L is offered in a standard 8-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of −40°C to 125°C.

schematic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	0.75 A
Continuous source-to-drain diode current, T_C = 25°C	0.75 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	2.25 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	19 mJ
Continuous total power dissipation at (or below) T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.75 A, V_{GS} = 5 V, See Notes 2 and 3			0.45	0.53	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 0.75 A, See Notes 2 and 3			1.8		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 0.75 A, V_{GS} = 0, See Notes 2 and 3 and Figure 12			0.85	1	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 0.75 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.7	Ω
			T_C = 125°C		0.94	1	
g_{fs}	Forward transconductance	V_{DS} = 10 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		0.75	0.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			115	145	pF
C_{oss}	Short-circuit output capacitance, common source				60	75	
C_{rss}	Short-circuit reverse transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.375 A, di/dt = 100 A/µs, V_{GS} = 0, V_{DS} = 48 V, See Figures 1 and 14	Z1, Z2, Z3		30		ns
			D1		85		
Q_{RR}	Total diode charge		Z1, Z2, Z3		0.03		µC
			D1		0.19		

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resistive-load switching characteristics, T_C = 25°C

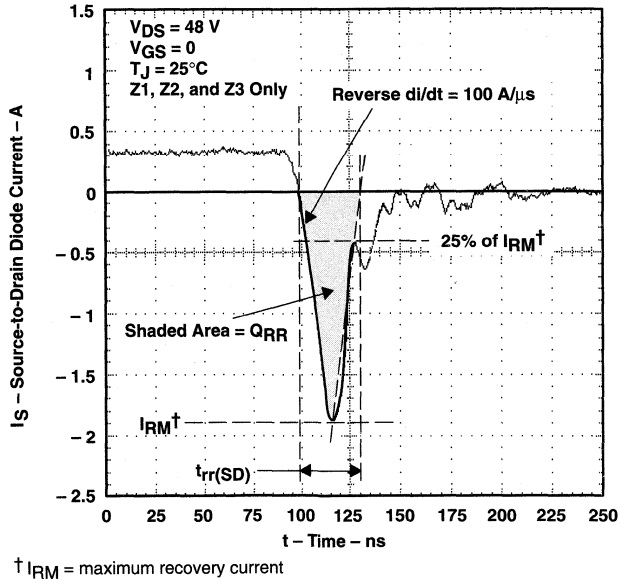
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 67 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		8	16	ns
$t_{d(off)}$	Turn-off delay time			12	24	
t_{r2}	Rise time			14	28	
t_{f2}	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.375 A, V_{GS} = 5 V, See Figure 3		1.8	2.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.1	1.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, See Note 4	All outputs with equal power		130		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

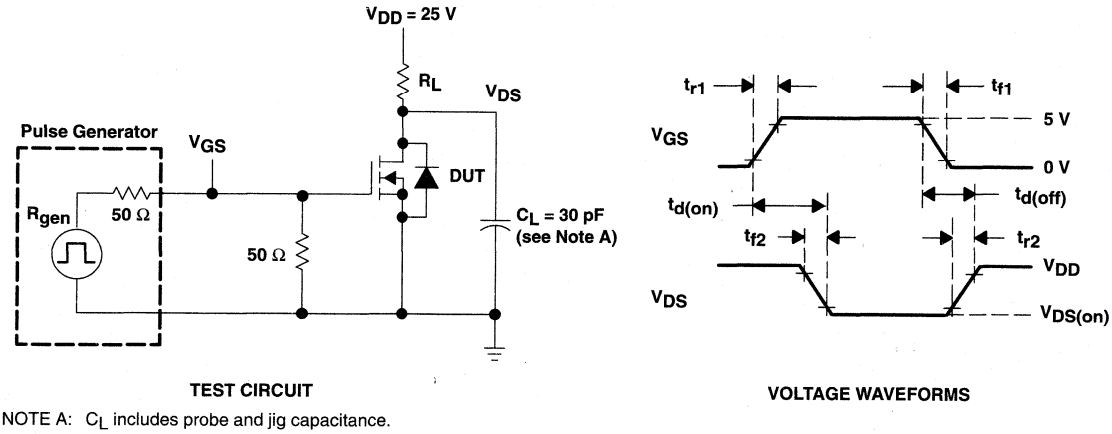
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
NOTE A. The above waveform represents D1 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION

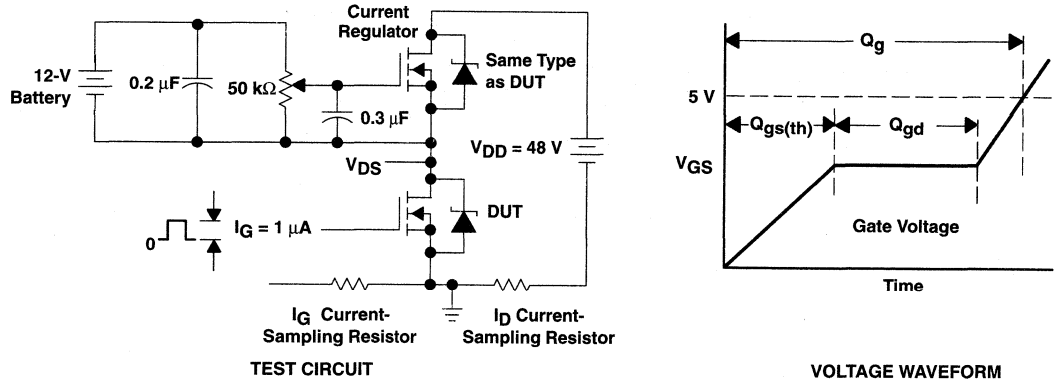


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

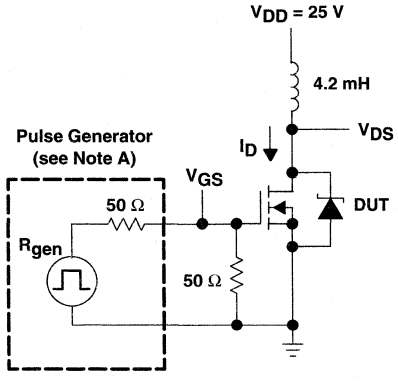


TEST CIRCUIT

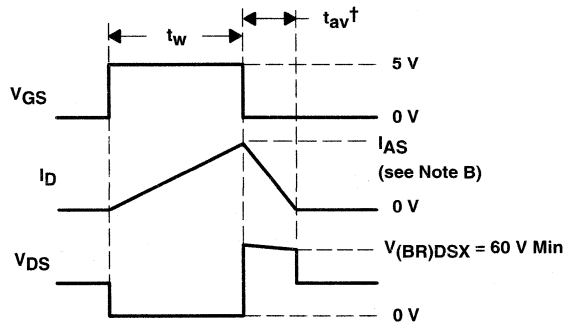
VOLTAGE WAVEFORM

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 19$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

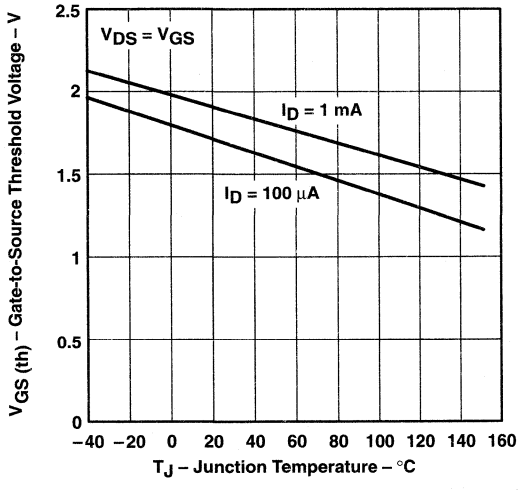


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

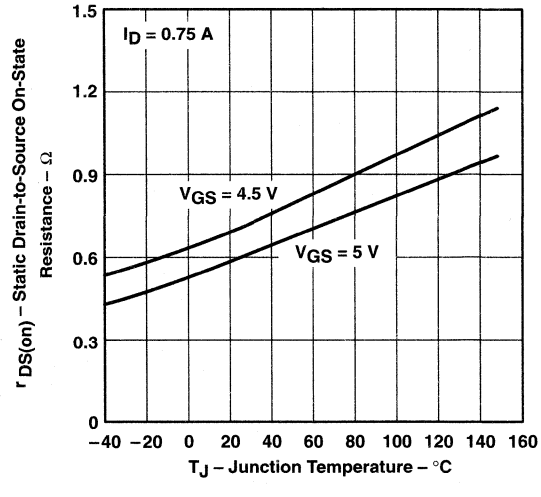


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

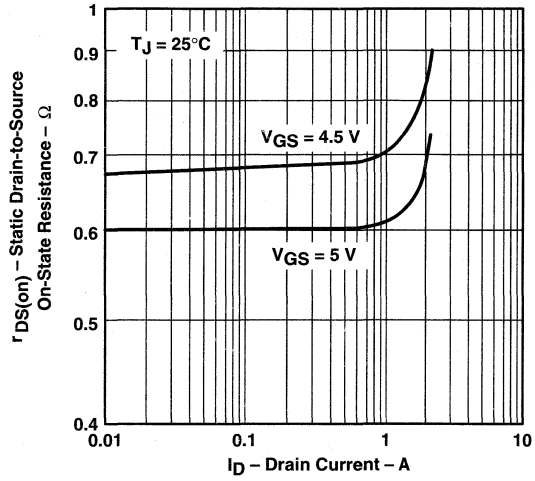


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

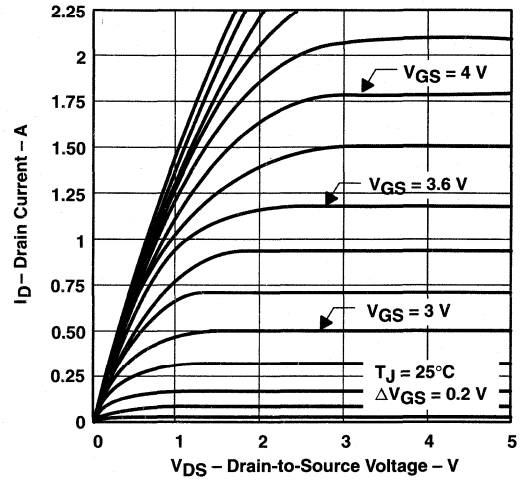


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

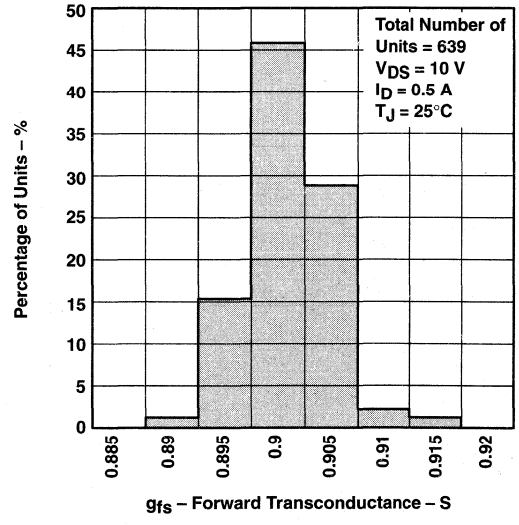


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

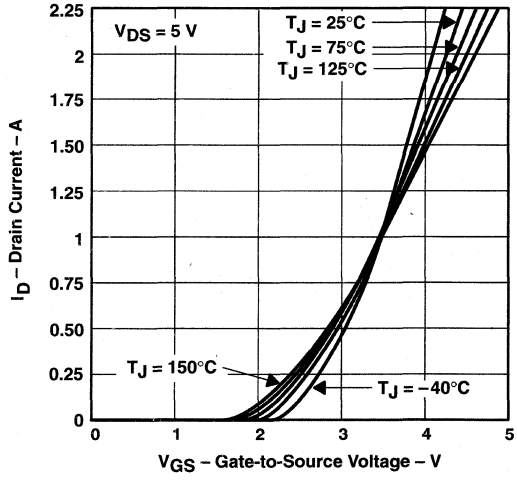


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

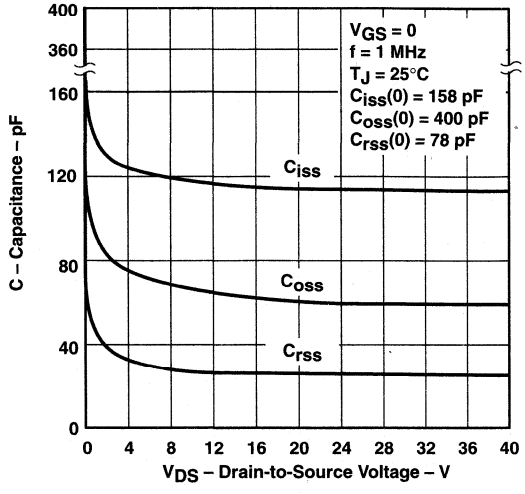


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

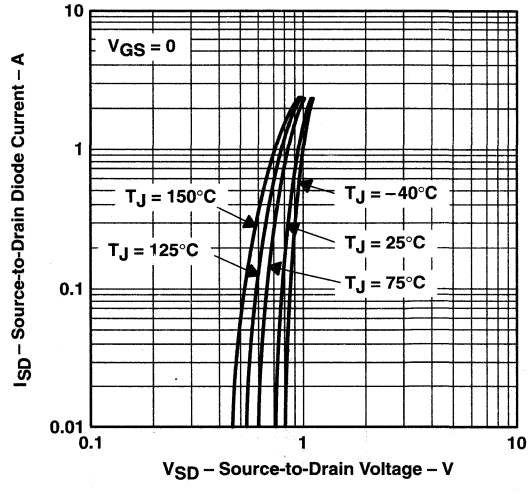


Figure 12

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

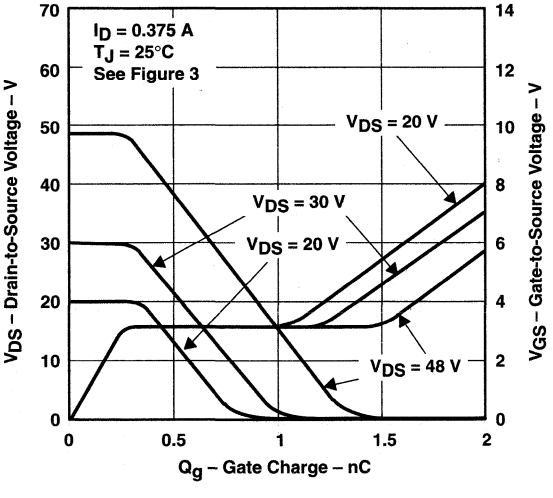


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

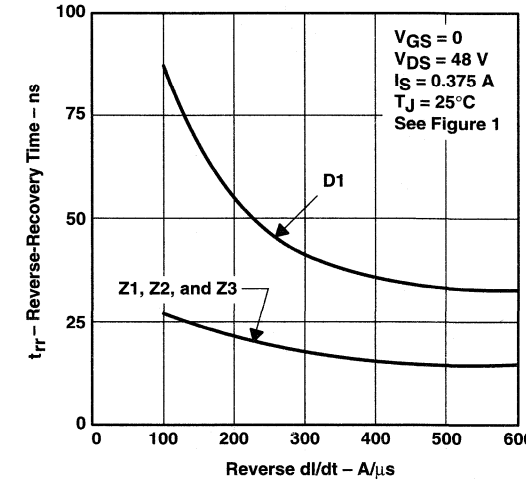
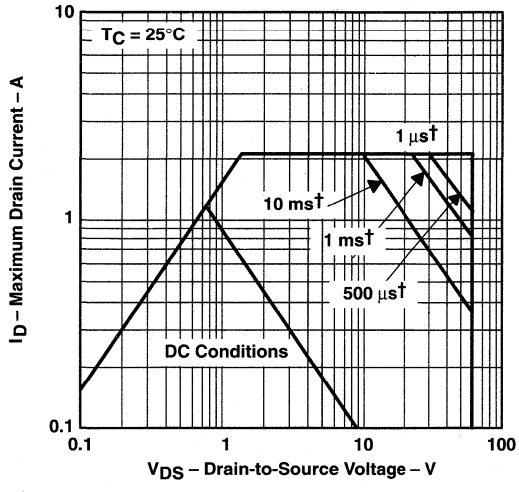


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

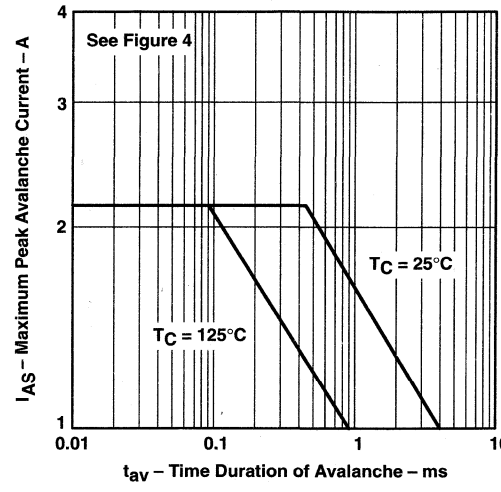
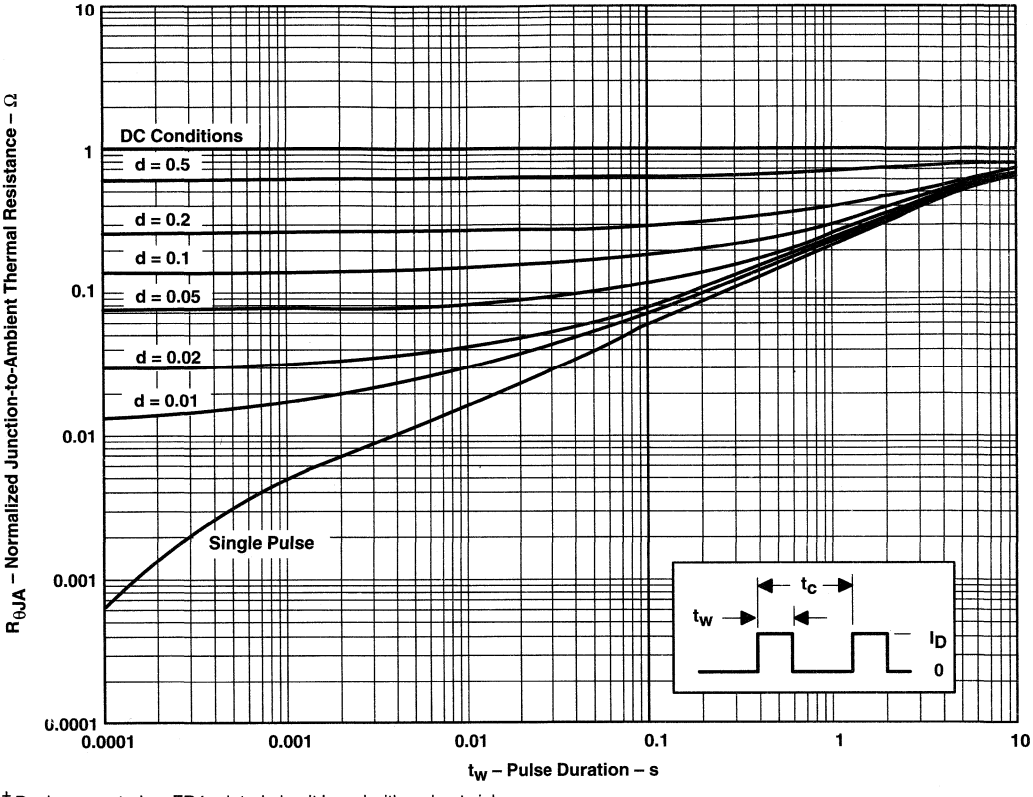


Figure 16

THERMAL INFORMATION

NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE† vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink.

NOTE A: $Z_{\theta A}(t) = r(t)\, R_{\theta JA}$

t_w = pulse duration

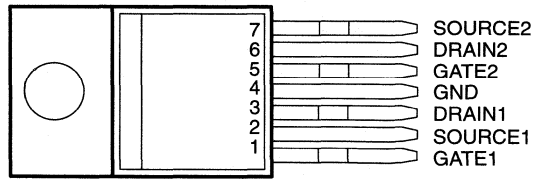
t_c = cycle time

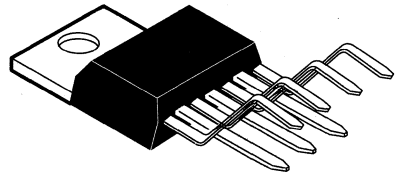
d = duty cycle = t_w/t_c

Figure 17

- **Two 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)





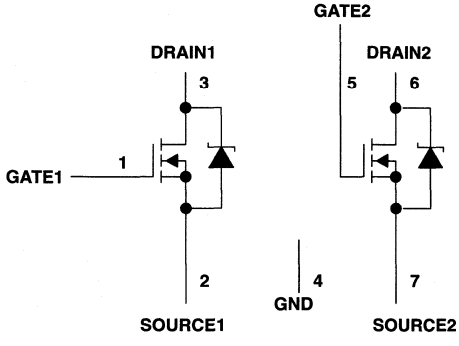
To ensure correct device operation, the source and the drain of the same transistor cannot simultaneously be taken below GND.

The tab is electrically connected to GND.

description

The TPIC5201 is a power monolithic DMOS array that consists of dual independent N-channel enhancement-mode DMOS transistors.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Source-GND voltage	60 V
Drain-GND voltage	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4			0.68	0.94	V
V_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{DS} = 0	T_C = 25°C		0.07	1	µA
			T_C = 125°C		1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C		0.09	0.125	Ω
			T_C = 125°C		0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4		2.5	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			490		pF
C_{oss}	Short-circuit output capacitance, common source				285		
C_{rss}	Short-circuit reverse transfer capacitance, common source				90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{GS} = 0, di/dt = 100 A/µs, V_{DS} = 48 V, See Figure 1		0.8	1.3	V
t_{rr}	Reverse-recovery time			200		ns
Q_{RR}	Total source-drain diode charge			1.5		µC

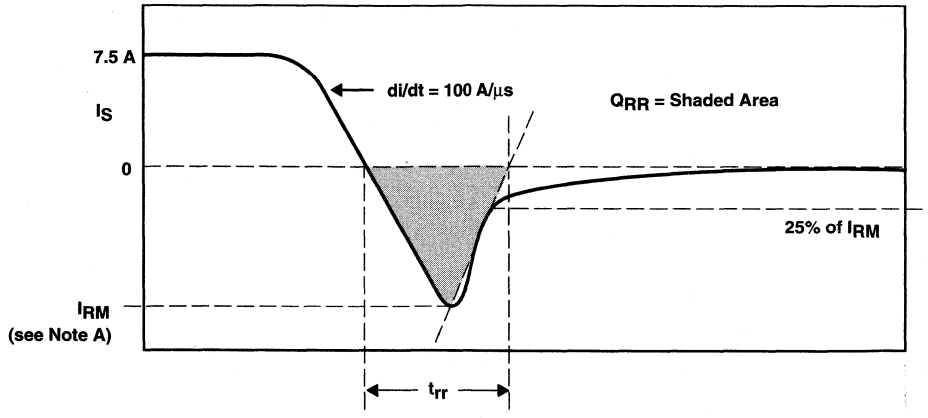
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 6.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		12		ns
t_r	Rise time			43		
$t_{d(off)}$	Turn-off delay time			100		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 2.5 A, V_{GS} = 15, See Figure 3		13.6	18	nC
Q_{gs}	Gate-source charge			8.3	11	
Q_{gd}	Gate-drain charge			5.3	7	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

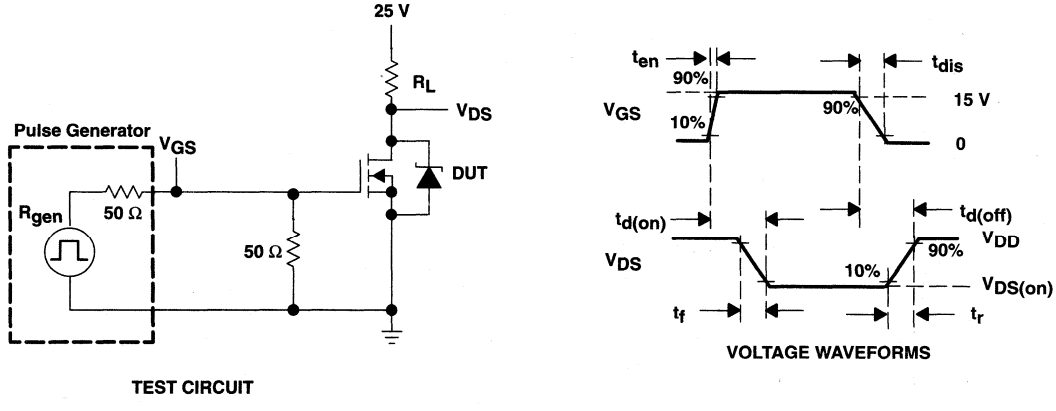


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

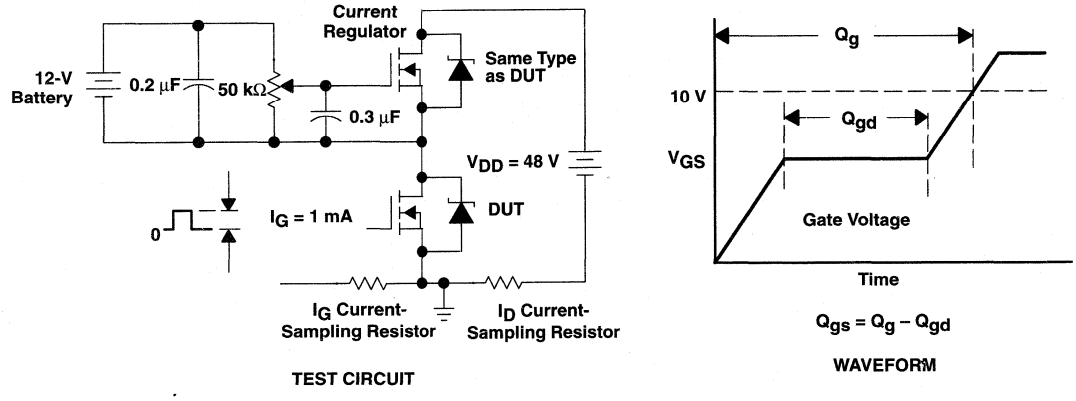
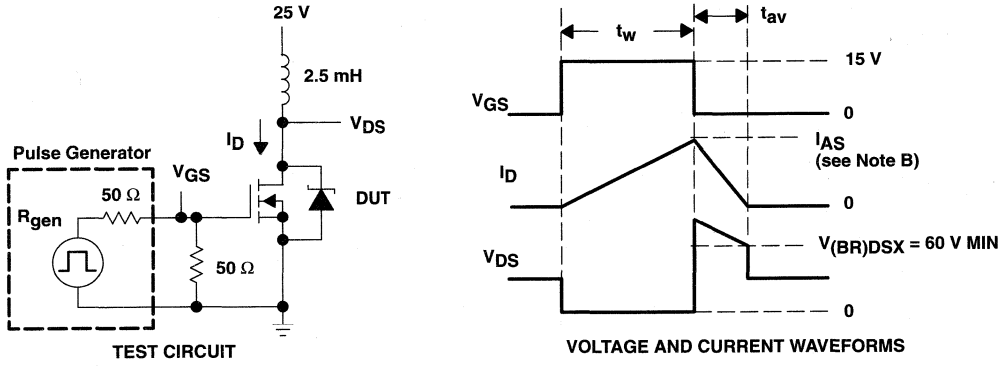


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

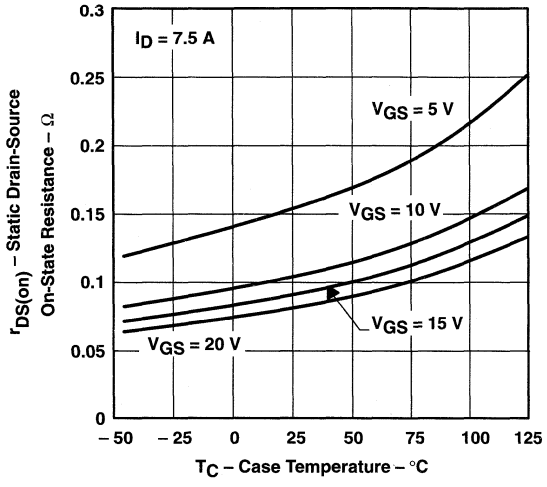


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

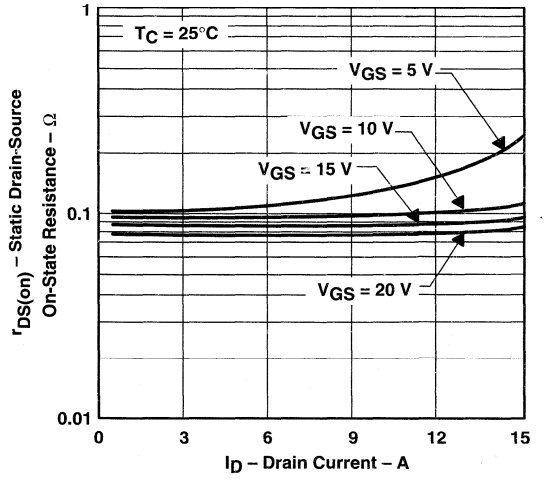


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

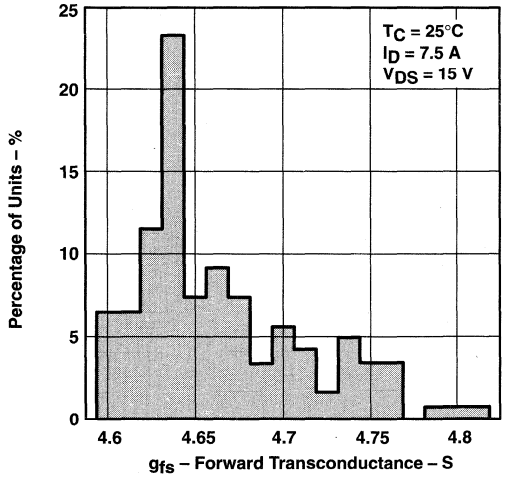


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

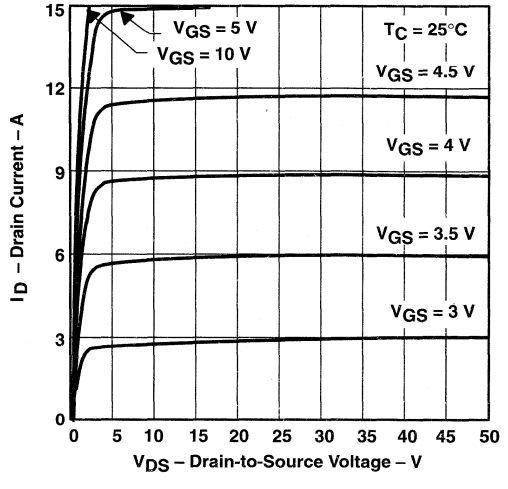


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
CASE TEMPERATURE

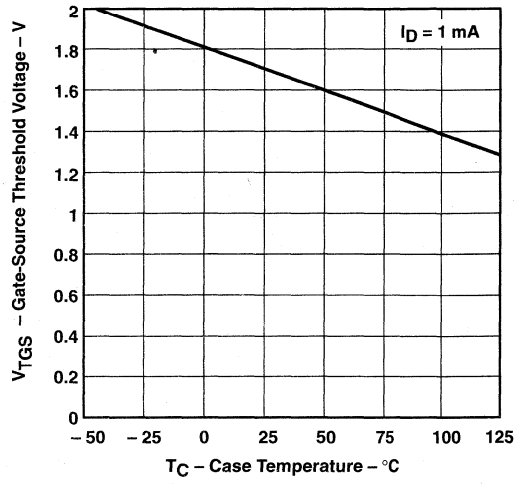


Figure 9

SOURCE-DRAIN DIODE CURRENT
vs
SOURCE-DRAIN VOLTAGE

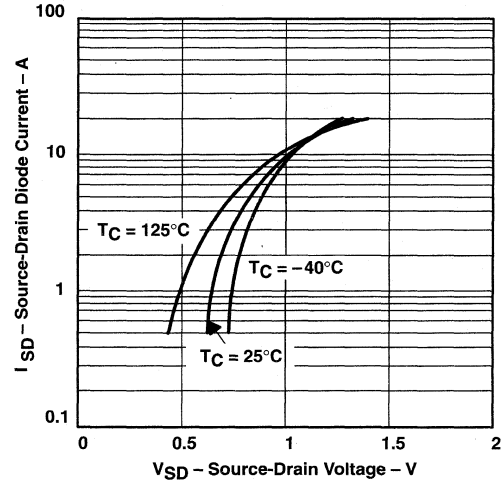


Figure 10

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

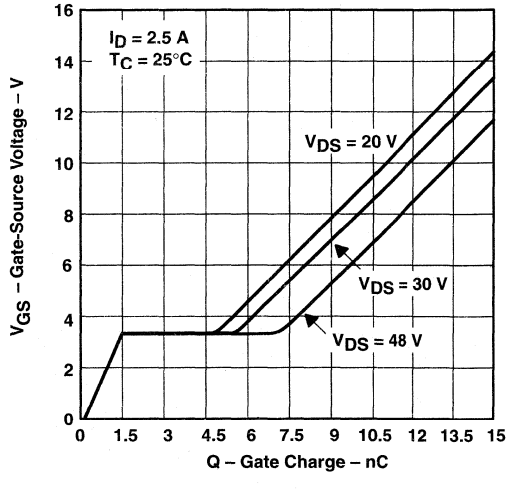


Figure 11

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

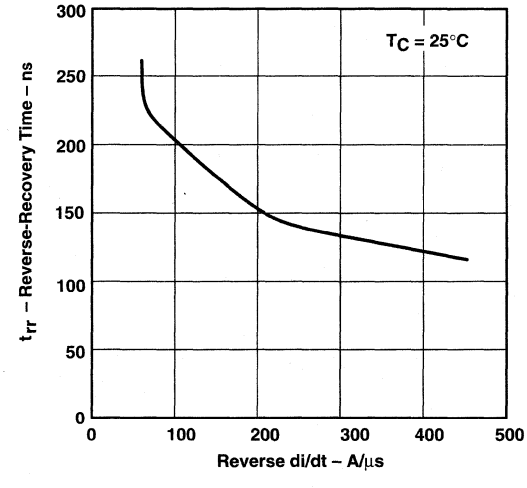


Figure 12

TYPICAL CHARACTERISTICS

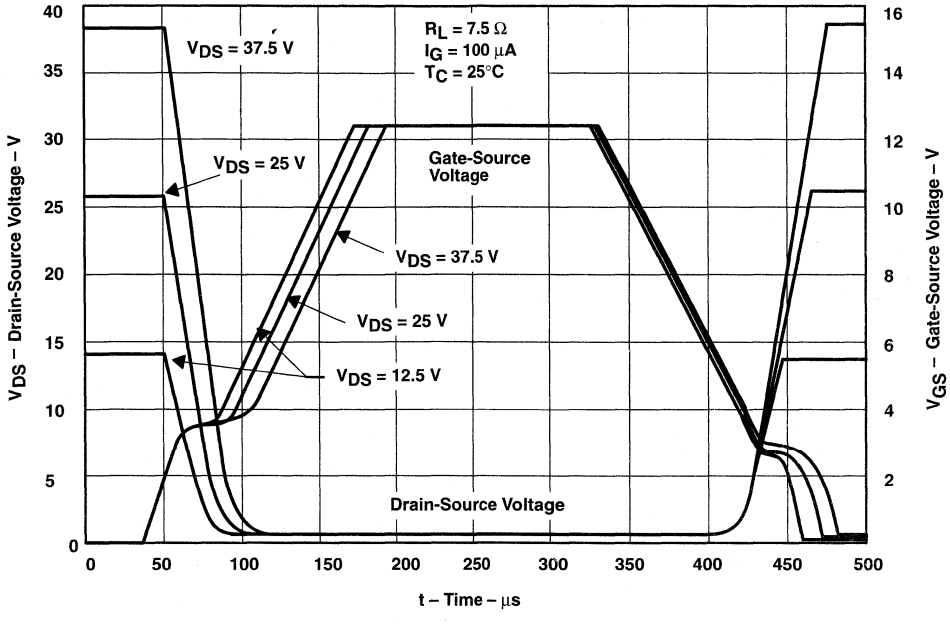


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-SOURCE VOLTAGE

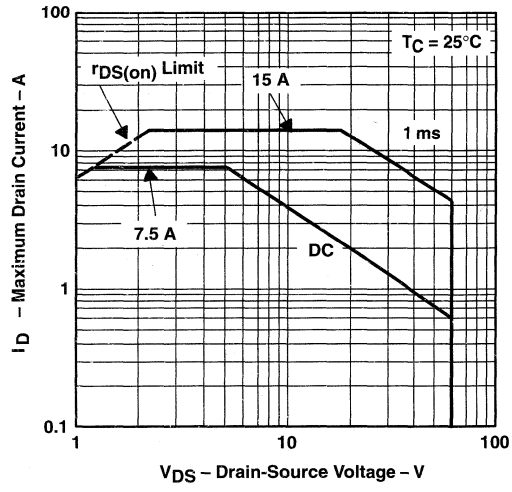


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

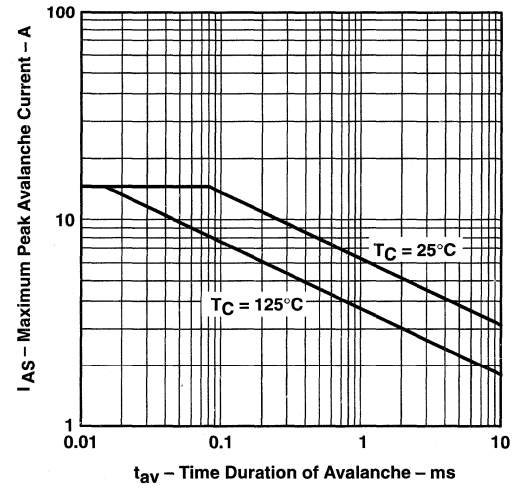
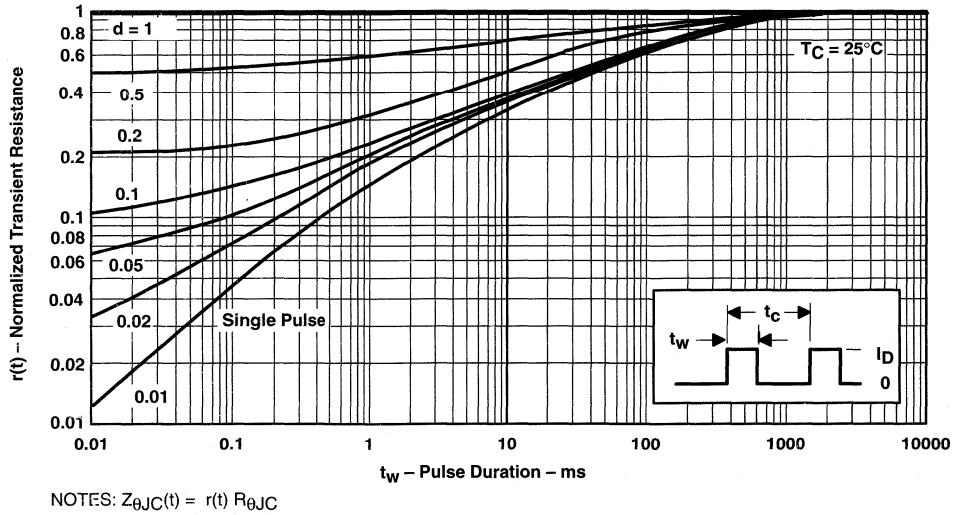


Figure 15

NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE DURATION

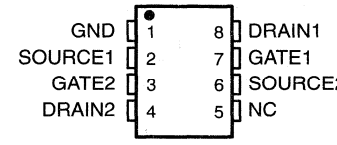


NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

Figure 16

- **Low $r_{DS(on)}$ . . . 0.26 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 8 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)



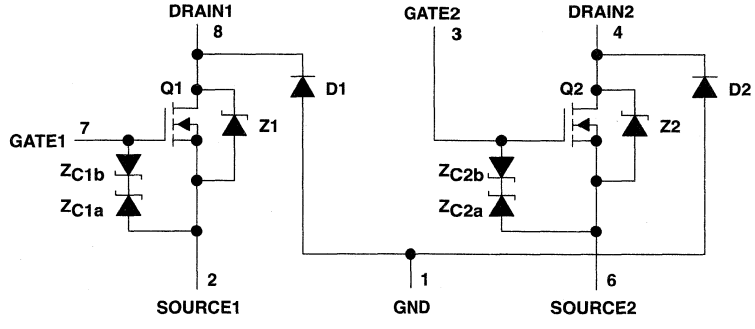
NC – No internal connection

description

The TPIC5203 is a monolithic gate-protected power DMOS array that consists of two independent electrically isolated N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5203 is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2)	100 V
Drain-to-GND voltage (Q1, Q2)	100 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1.6 A
Continuous source-to-drain diode current, T_C = 25°C	1.6 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	8 A
Continuous gate-to-source zener diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	21.6 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	962 mW
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	2.05	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.6 A, V_{GS} = 10 V, See Notes 2 and 3			0.42	0.5	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.6 A, V_{GS} = 0 (Z1, Z2), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.6 A (D1, D2), See Notes 2 and 3			5		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1.6 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.26	0.31	Ω
			T_C = 125°C		0.41	0.45	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 800 mA, See Notes 2 and 3 and Figure 9		1.5	1.83		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			150	275	pF
C_{oss}	Short-circuit output capacitance, common source				100	150	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 800 mA, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, See Figures 1 and 14	Z1 and Z2		50		ns
			D1 and D2		265		
Q_{RR}	Total diode charge		Z1 and Z2		63		nC
			D1 and D2		1240		

resistive-load switching characteristics, T_C = 25°C

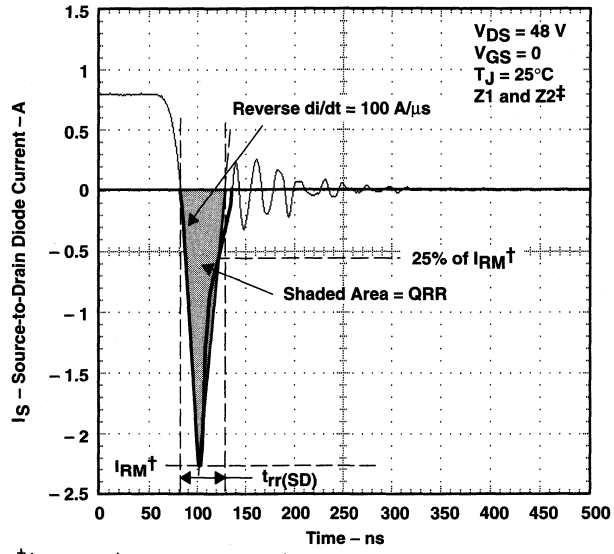
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 30 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			27	50	
t_r	Rise time			15	30	
t_f	Fall time			7	15	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.8 A, V_{GS} = 10 V, See Figure 3		4.7	5.9	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			1.9	2.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		130		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		79		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		34		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink
5. Package mounted on a 24 inch^2, 4-layer FR4 printed-circuit board
6. Package mounted in intimate contact with infinite heatsink
7. All outputs with equal power

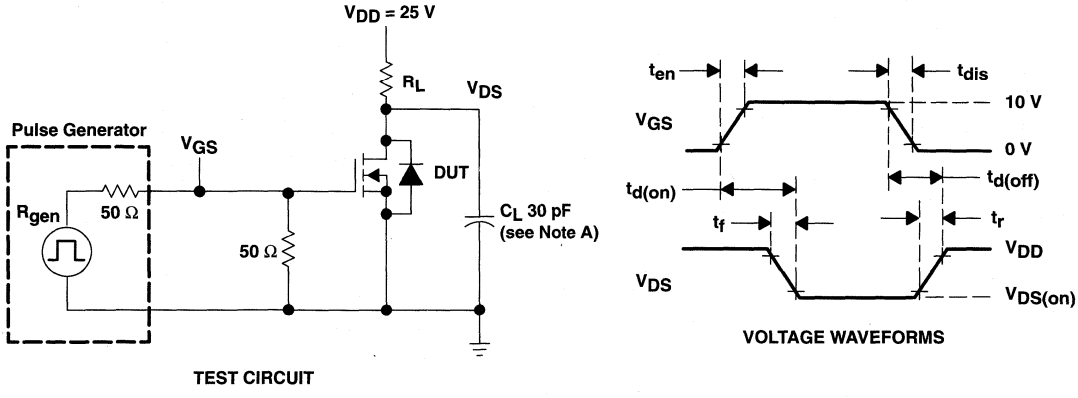
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1 and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

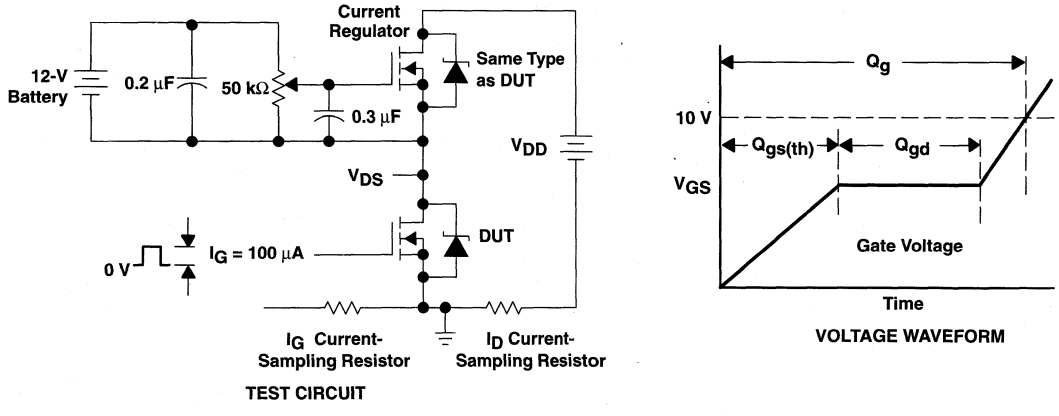
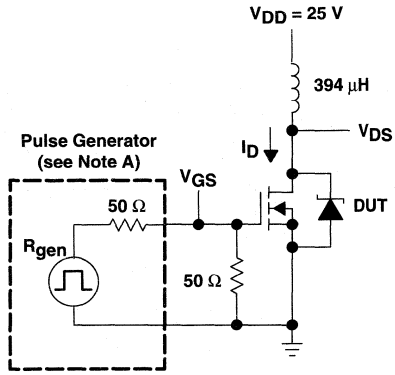
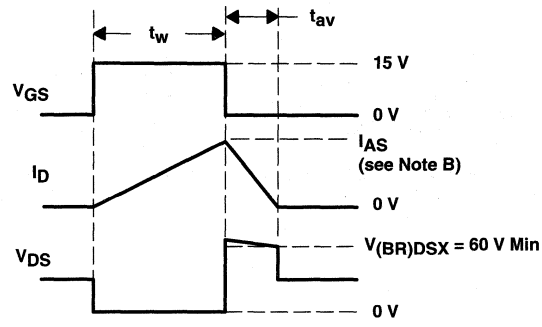


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 8$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21.6$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

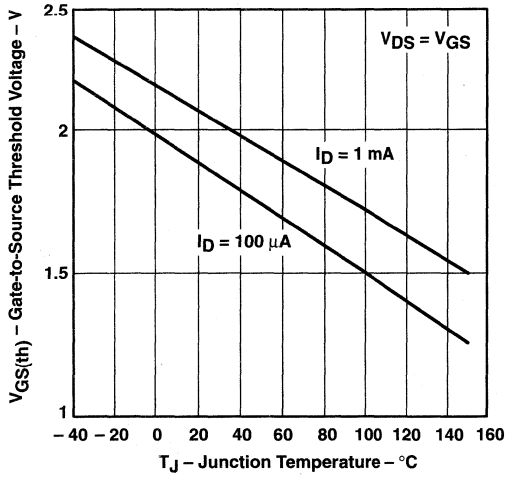


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

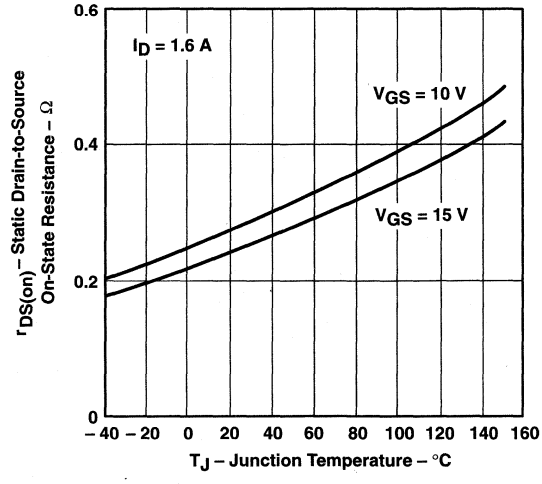


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

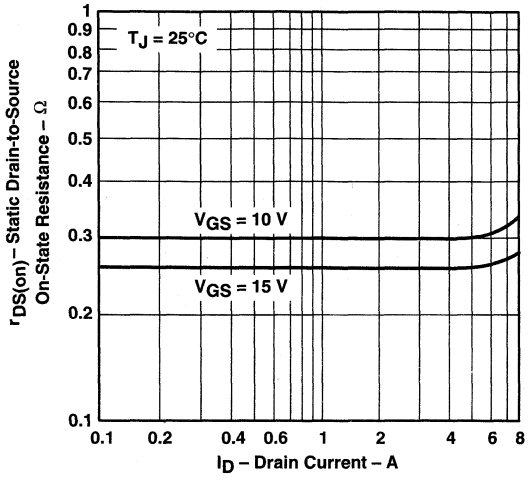


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

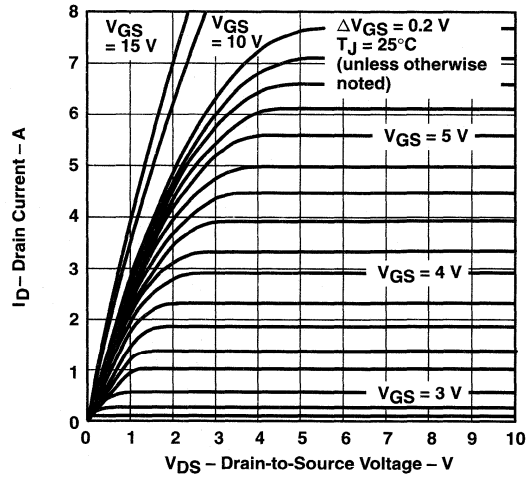


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

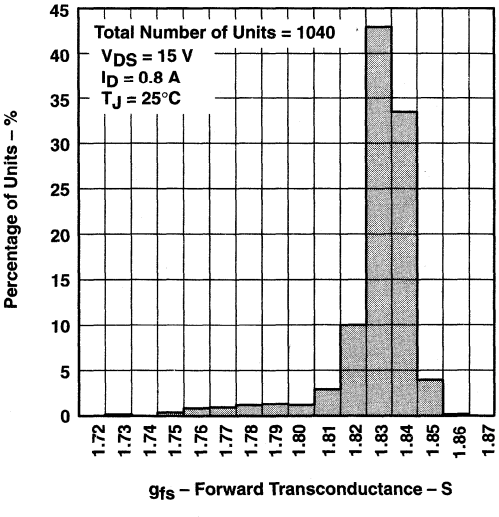


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

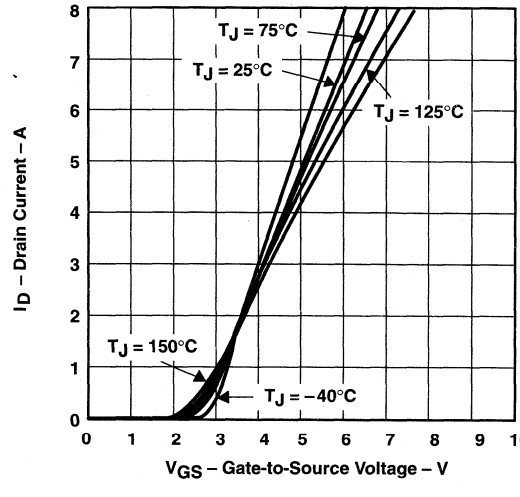


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

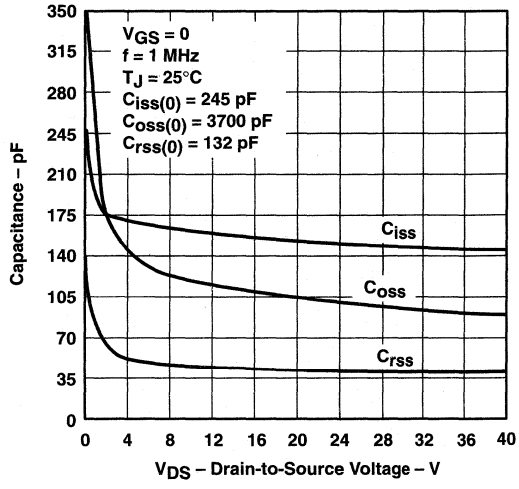


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

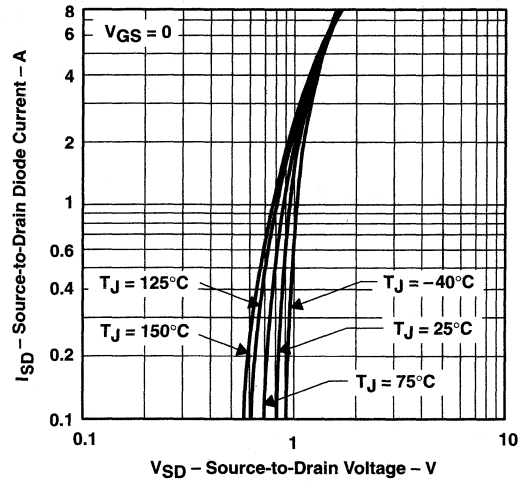


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

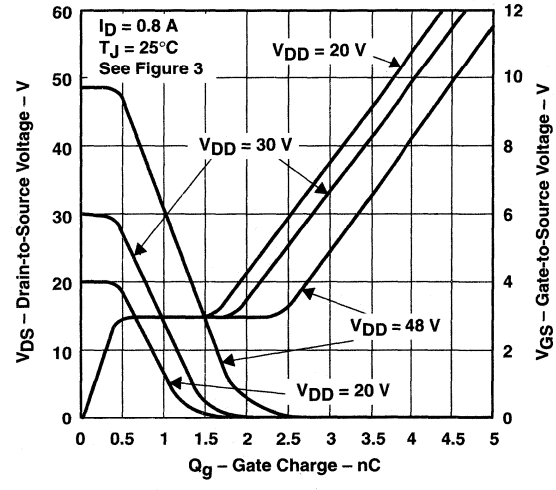


Figure 13

REVERSE RECOVERY TIME
vs
REVERSE di/dt

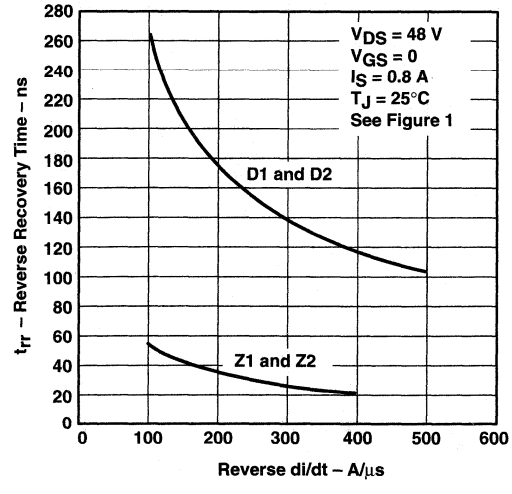
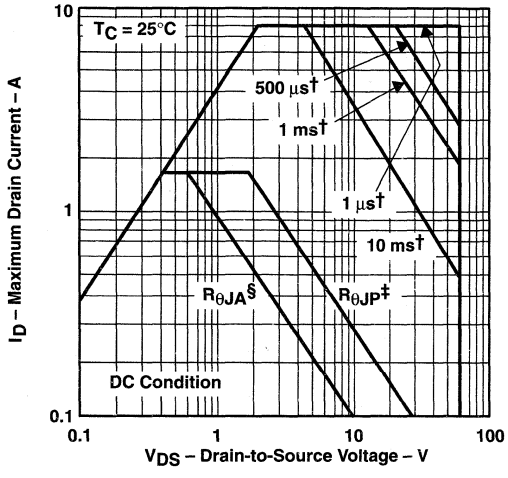


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted in intimate contact with infinite heatsink.
§ Device mounted on FR4 printed circuit board with no heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

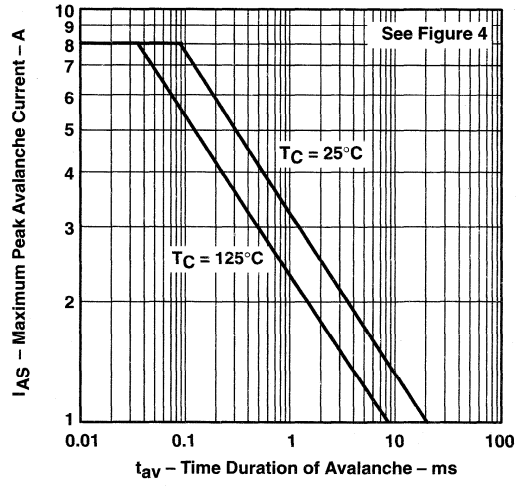
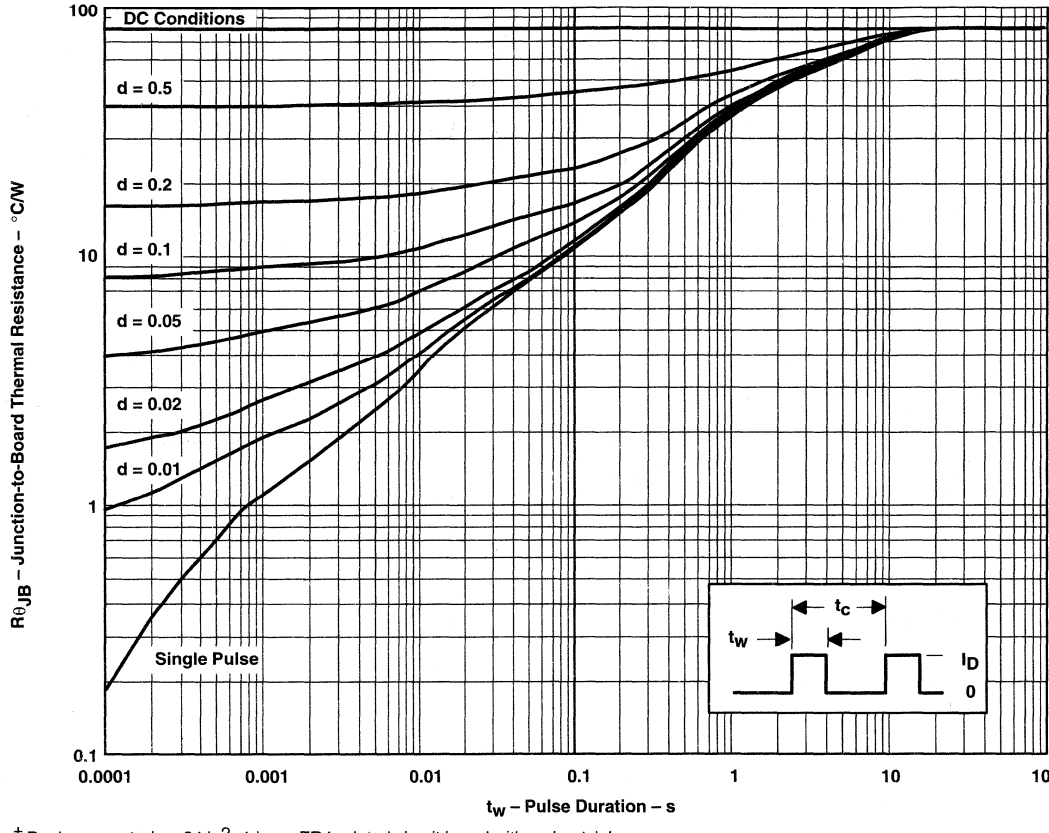


Figure 16

THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



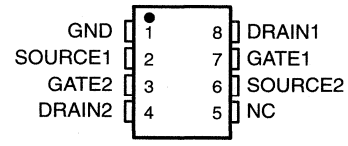
† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink

NOTE A. $Z_{\theta JB}(t) = r(t)R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

- **Low $r_{DS(on)}$ . . . 0.38 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)



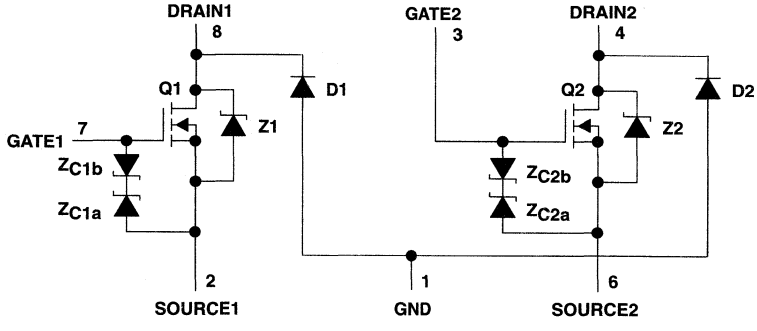
NC – No internal connection

description

The TPIC5223L is a monolithic gate-protected logic-level power DMOS array that consists of two electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5223L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	108 mJ
Continuous total power dissipation, T_C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	2.05	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.375	0.425	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2), See Notes 2 and 3 and Figure 12			0.85	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			3		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.38	0.43	Ω
			T_C = 125°C		0.61	0.65	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 500 mA, See Notes 2 and 3 and Figure 9		1.2	1.49		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			150	190	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 500 mA, V_{DS} = 48 V, V_{GS} = 0, di/dt = 100 A/µs, See Figures 1 and 14	Z1 and Z2		50		ns
			D1 and D2		210		
Q_{RR}	Total diode charge		Z1 and Z2		50		nC
			D1 and D2		800		

resistive-load switching characteristics, T_C = 25°C

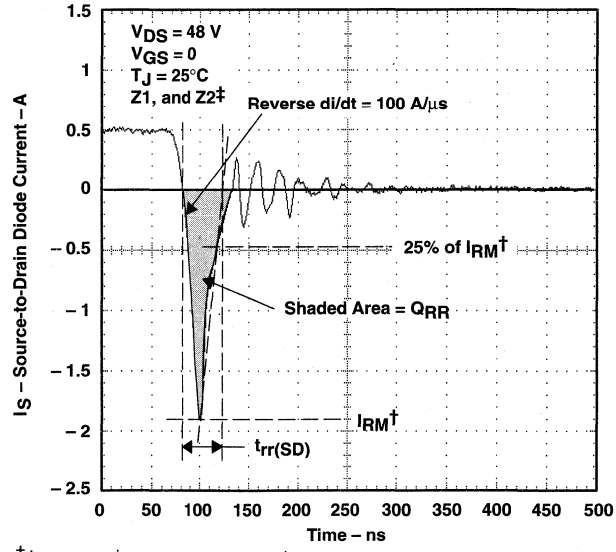
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		34	70	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_{r1}	Rise time			28	55	
t_{f2}	Fall time			15	30	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 500 mA, V_{GS} = 5 V, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			1.9	2.3	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		130		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		78.6		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		34		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

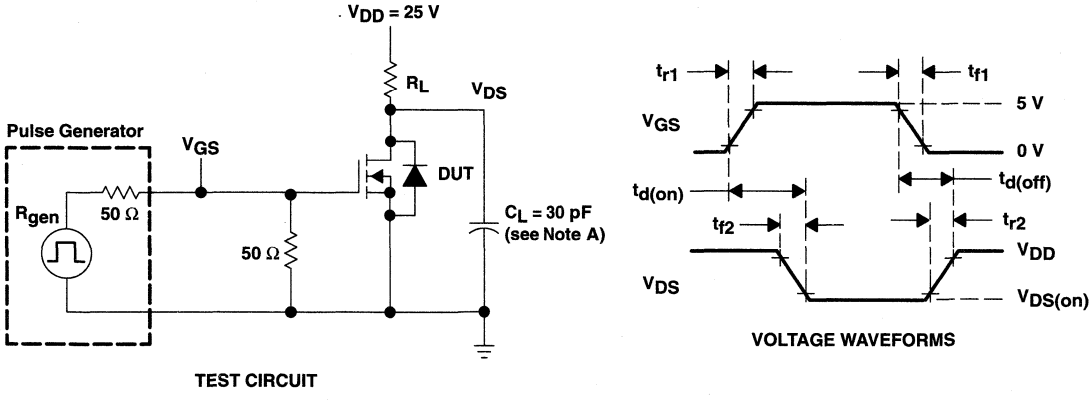
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1 and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

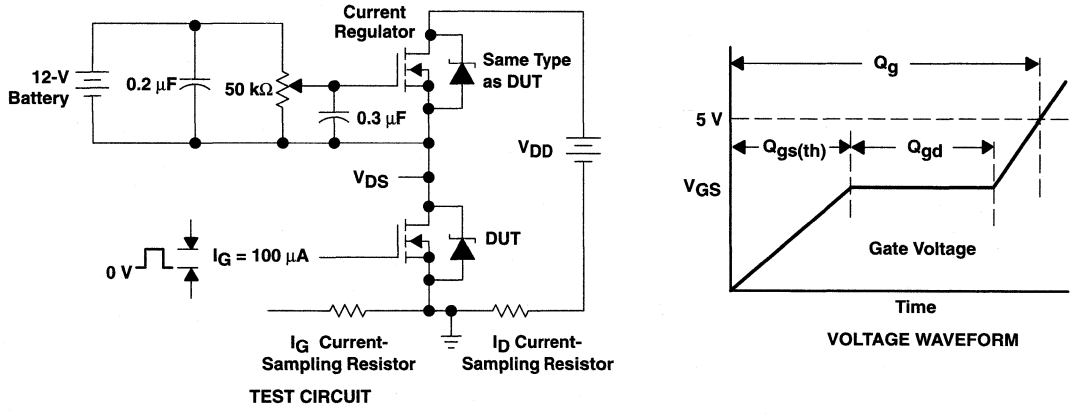
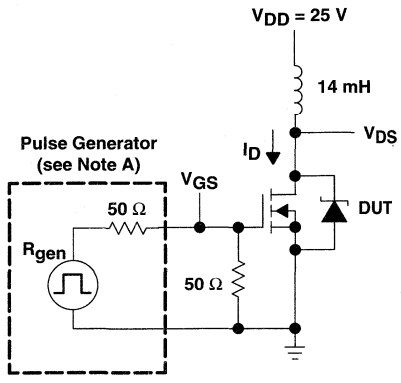
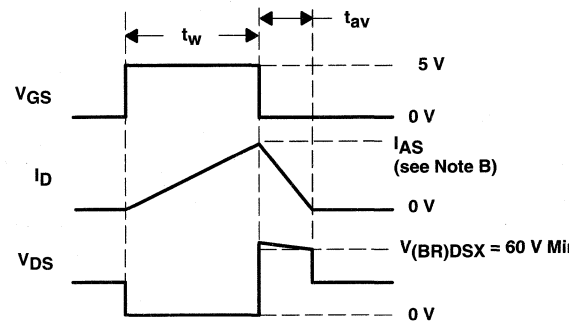


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 108$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

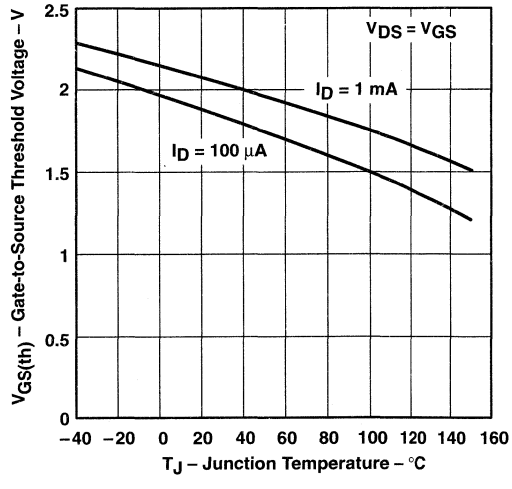


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

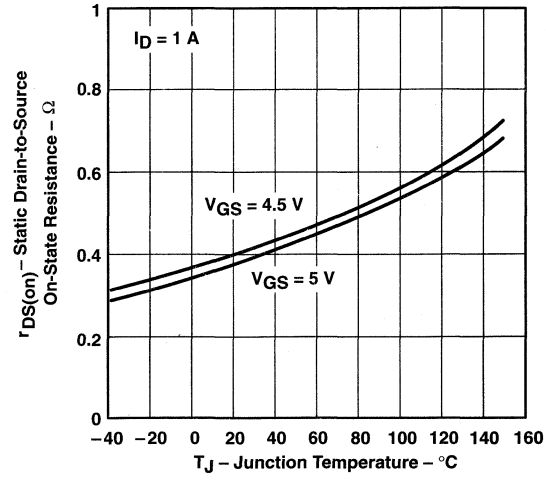


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

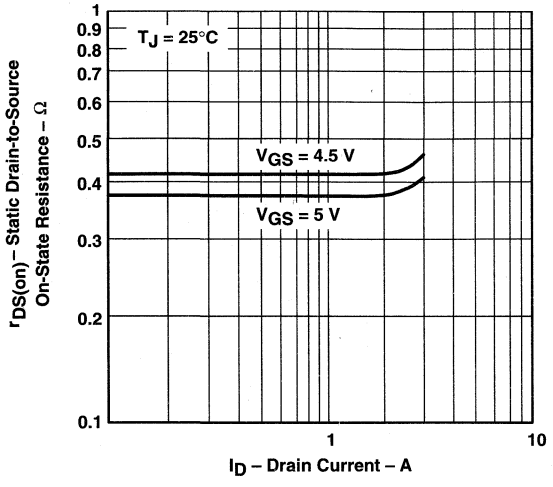


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

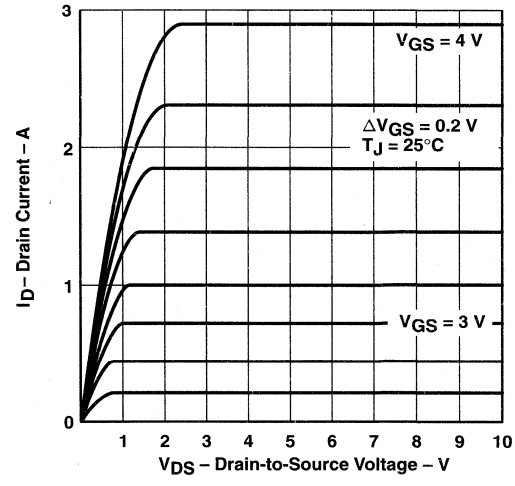


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

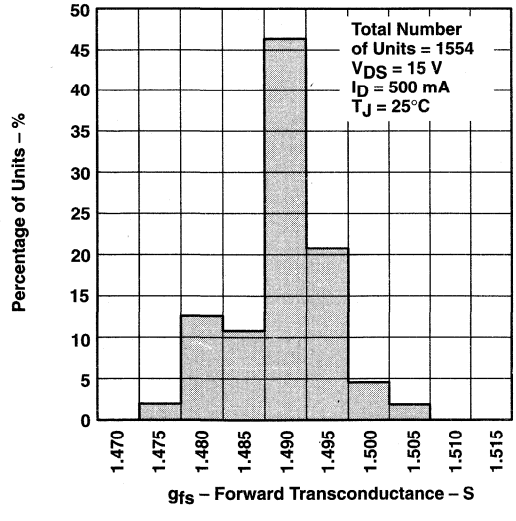


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

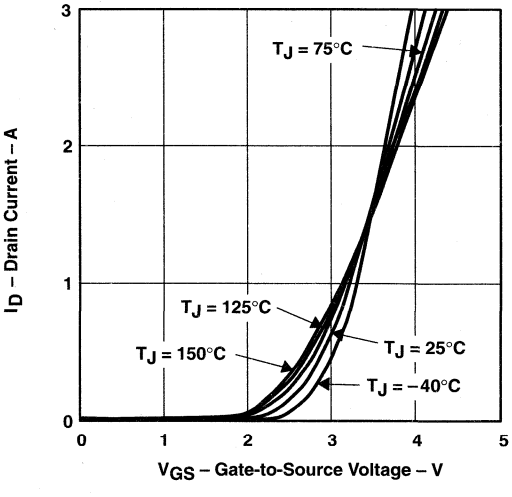


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

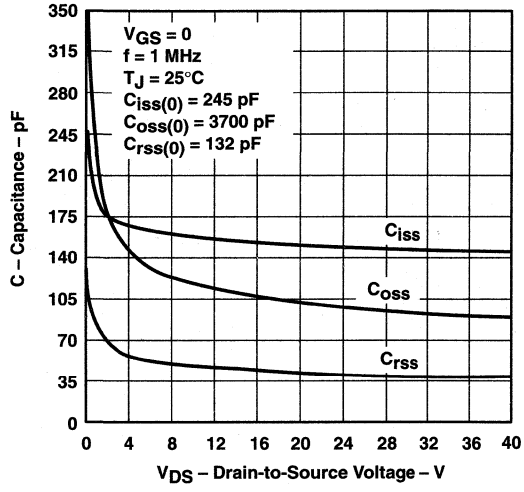


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

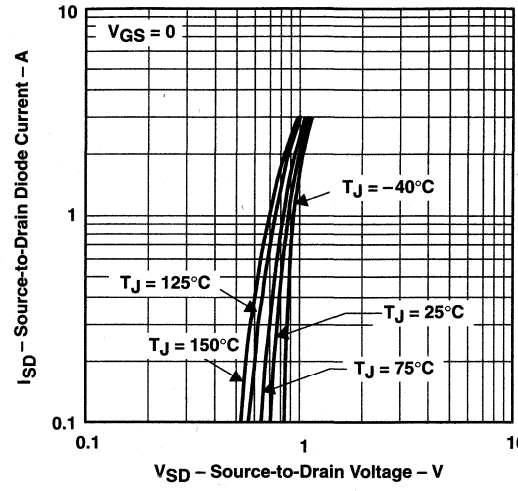


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

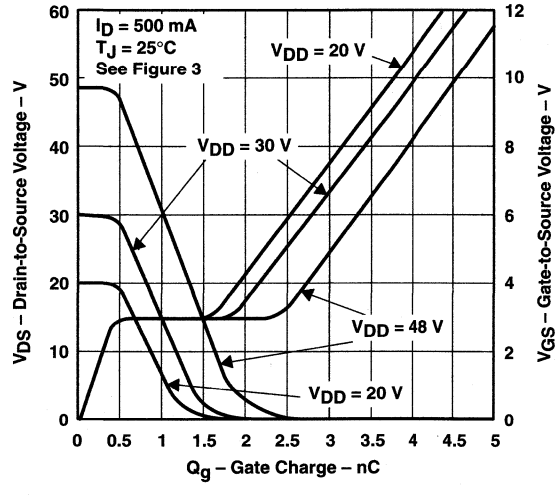


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

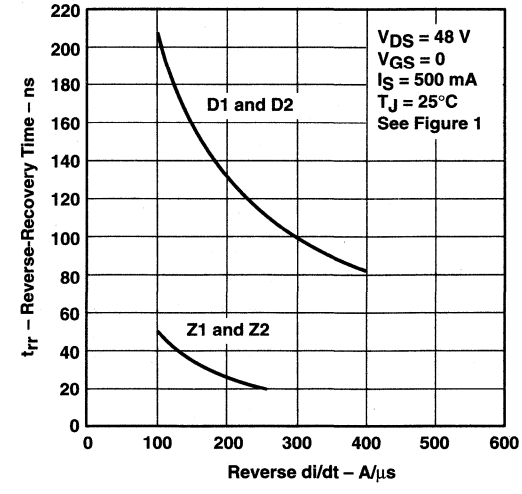
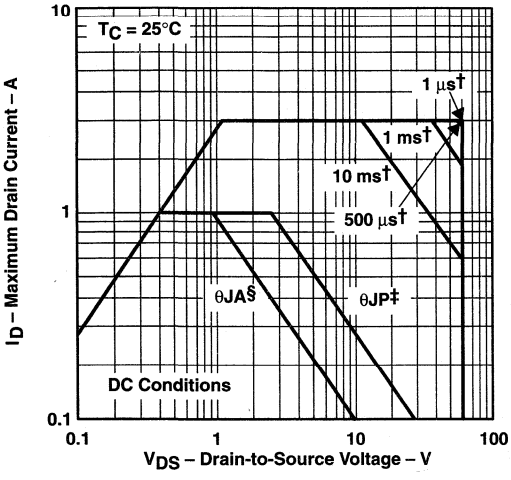


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted in intimate contact with infinite heatsink.
§ Device mounted on FR4 printed-circuit board with no heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

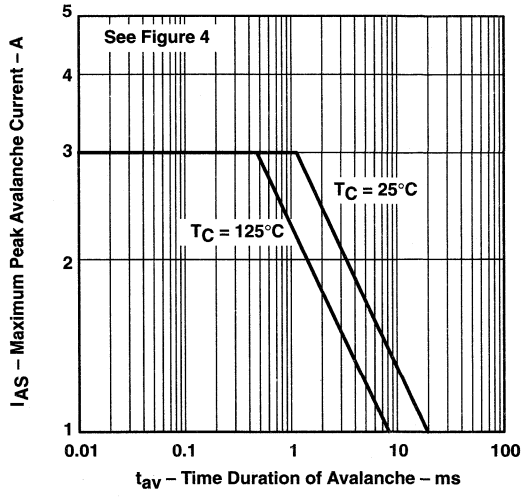
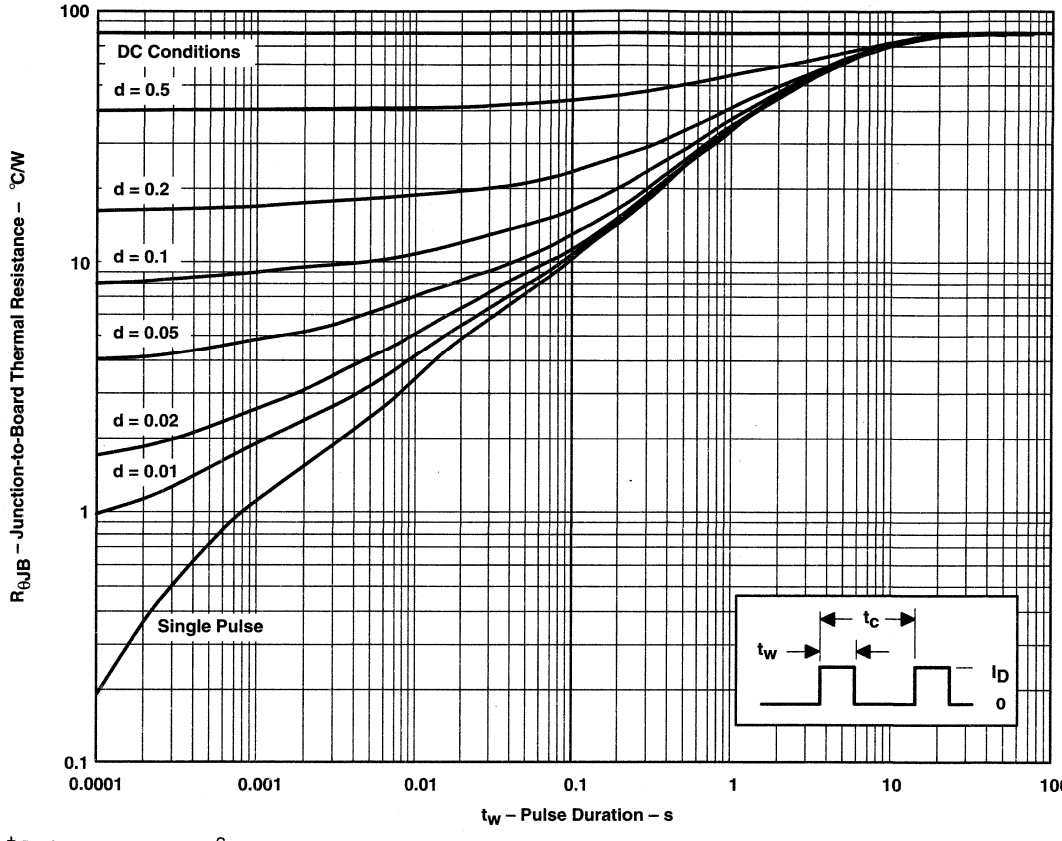


Figure 16

THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



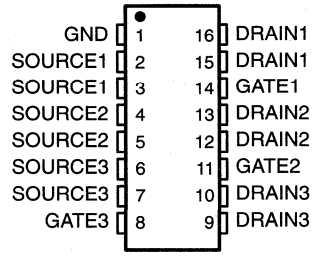
† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 17

- **Low $r_{DS(on)}$ . . . 0.3 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 7 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)

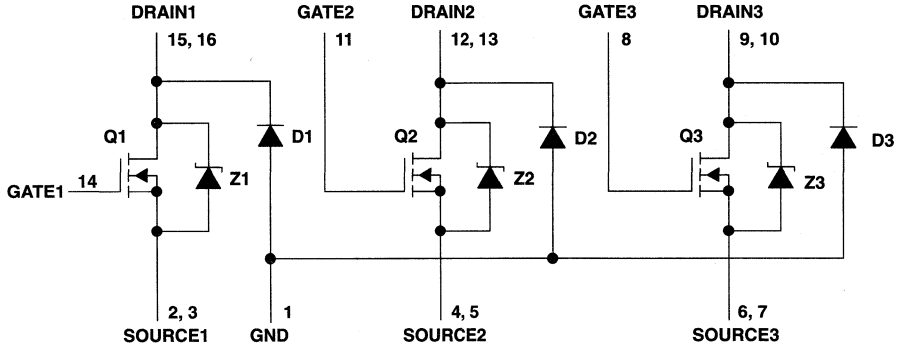


description

The TPIC5302 is a monolithic power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors. The TPIC5302 is offered in a standard 16-pin small-outline surface-mount (D) package.

The TPIC5302 is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1.4 A
Continuous source-to-drain diode current	1.4 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 6)	7 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	10.5 mJ
Continuous total power dissipation at (or below) T_C = 25°C	1087 mW
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.4 A, V_{GS} = 10 V, See Notes 2 and 3			0.42	0.49	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.4 A, V_{GS} = 0 (Z1, Z2, Z3), See Notes 2 and 3			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.4 A			4.8		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1.4 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.41	0.5	
g_{fs}	Forward transconductance	V_{DS} = 10 V, See Notes 2 and 3	I_D = 0.7 A,	1.15	1.41		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz	V_{GS} = 0,		135	170	pF
C_{oss}	Short-circuit output capacitance, common source				80	100	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum and pulse duration ≤5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		35		ns
Q_{RR}	Total diode charge			0.04		µC

GND-to-drain diode characteristics, T_C = 25°C (see schematic, D1, D2, and D3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 0.5 A, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		130		ns
Q_{RR}	Total diode charge			0.4		µC

resistive-load switching characteristics, T_C = 25°C

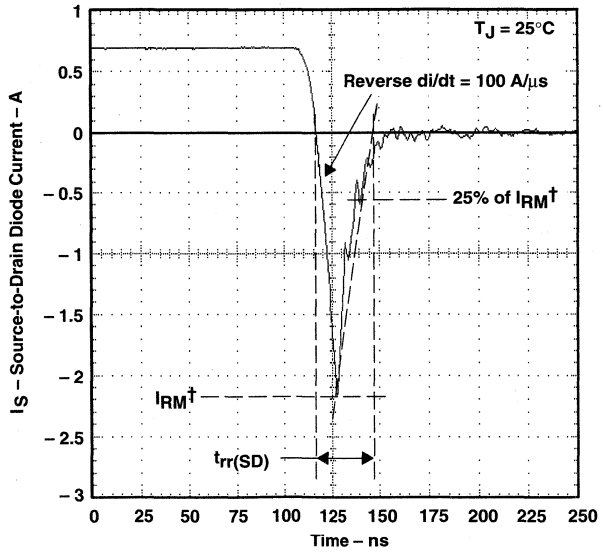
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		23	46	ns
$t_{d(off)}$	Turn-off delay time			25	50	
t_{r2}	Rise time			5	10	
t_{f2}	Fall time			17	34	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 10 V, See Figure 3		8	9.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.63	
Q_{gd}	Gate-to-drain charge			1.5	1.85	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		115		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			32		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

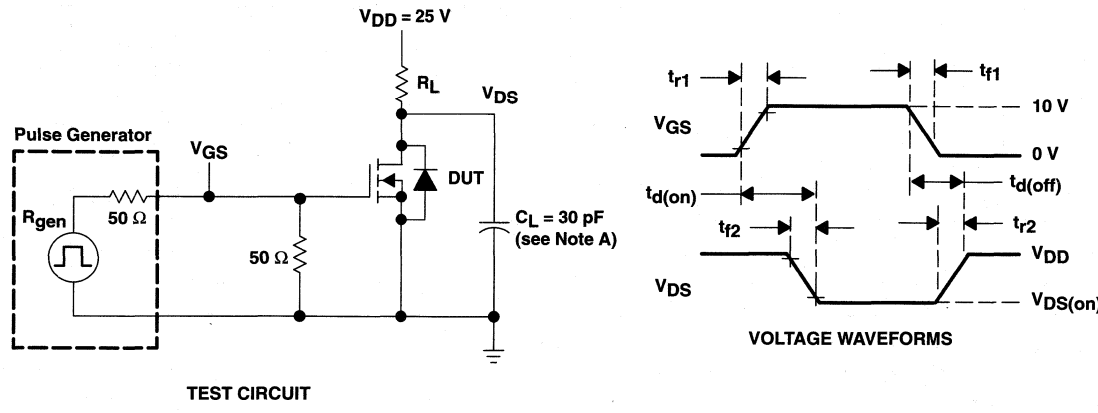
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

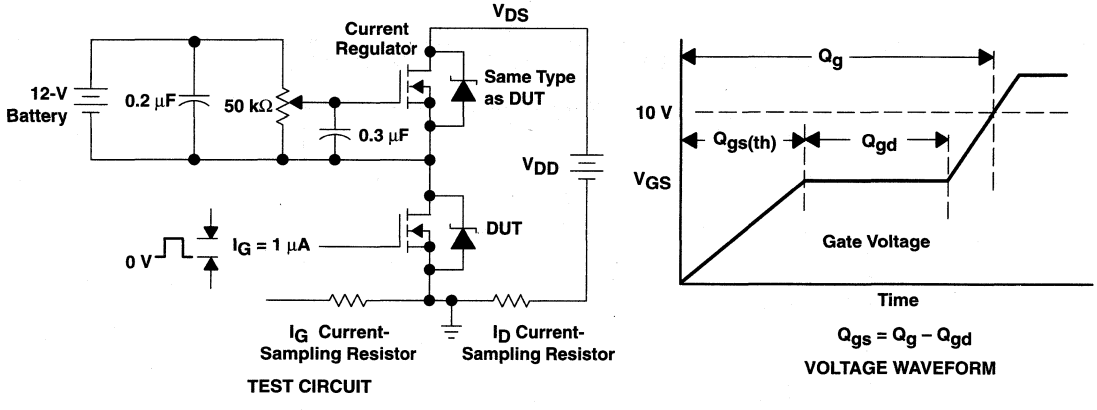


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

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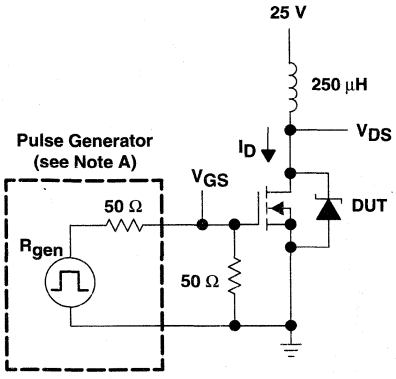
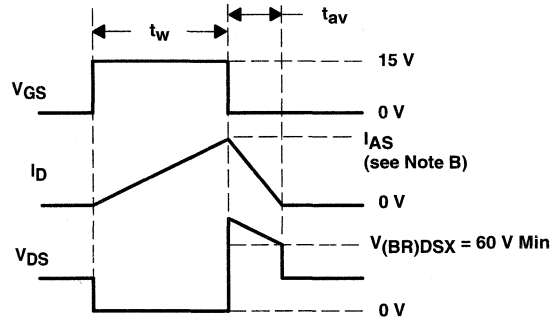
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7$ A, where t_{av} = avalanche time.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 10.5$ mJ

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

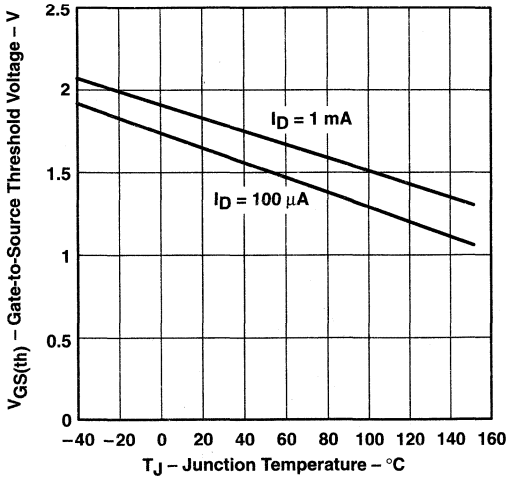


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

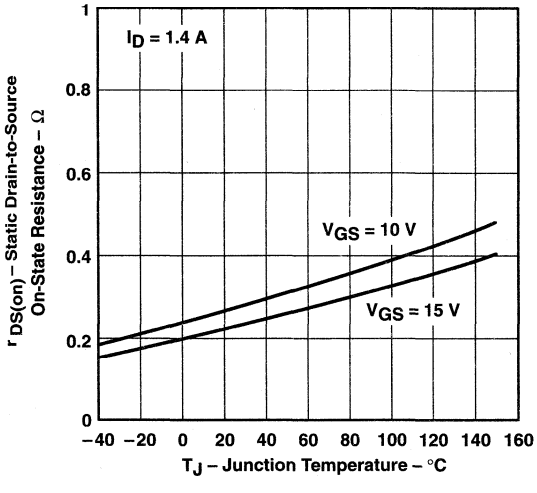


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

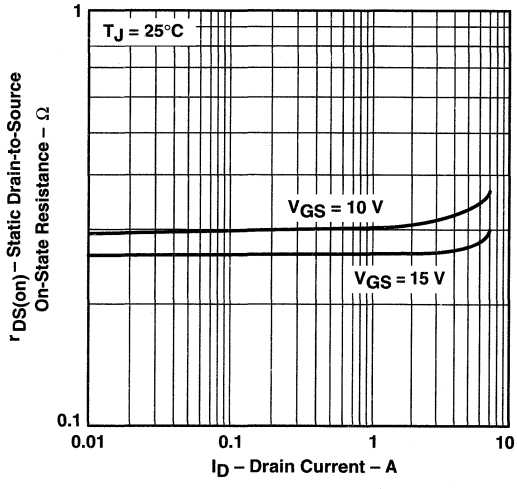


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

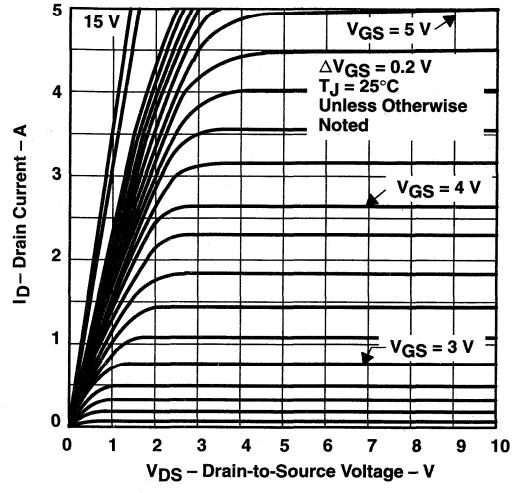


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

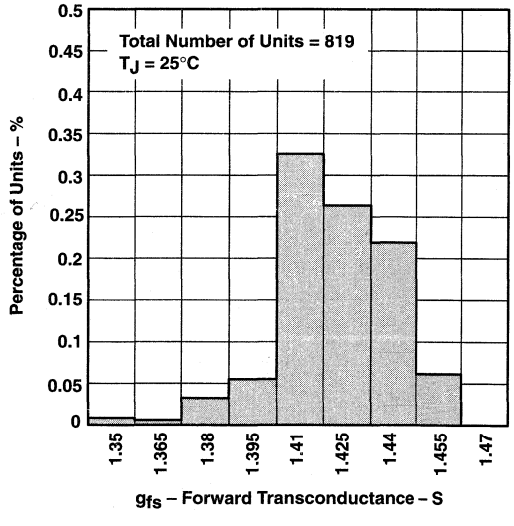


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

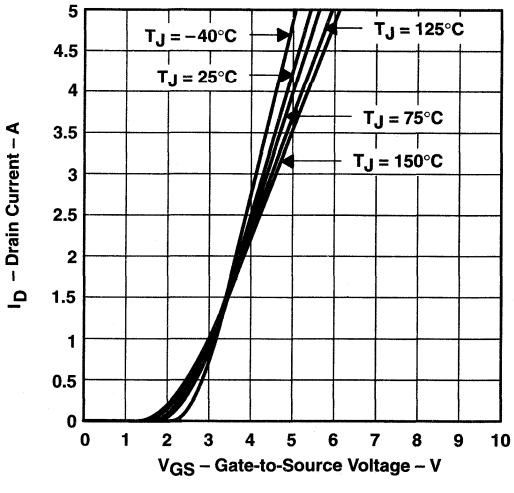


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

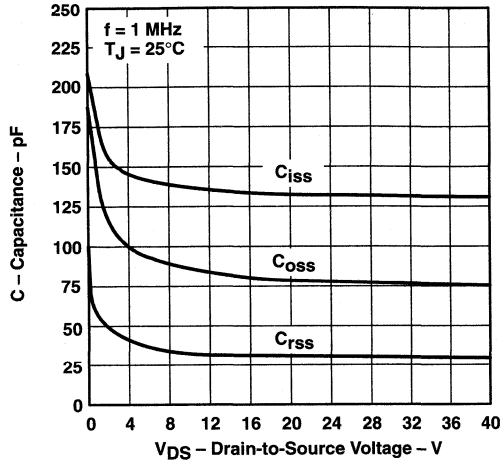


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

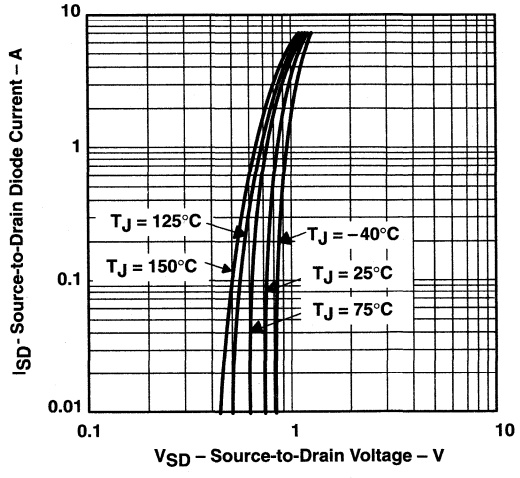


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

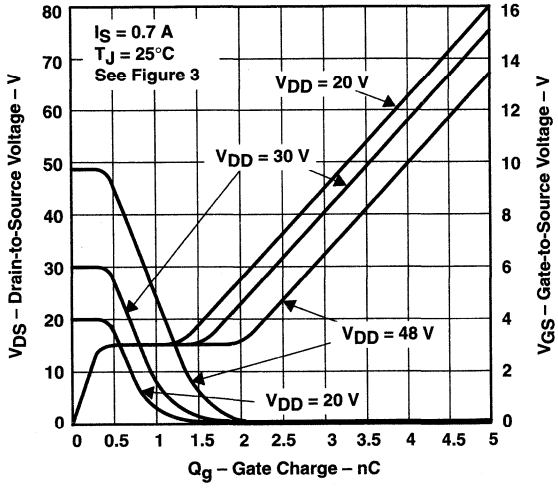


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

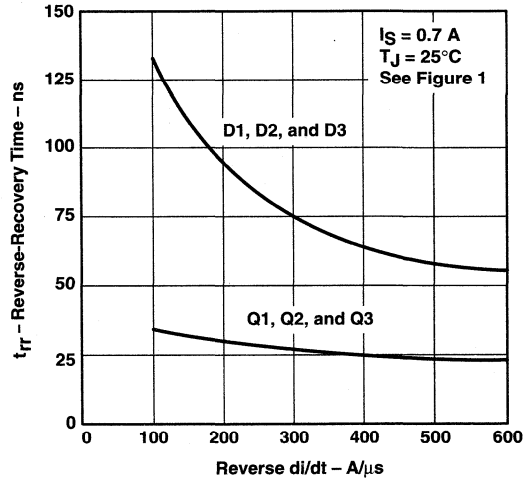
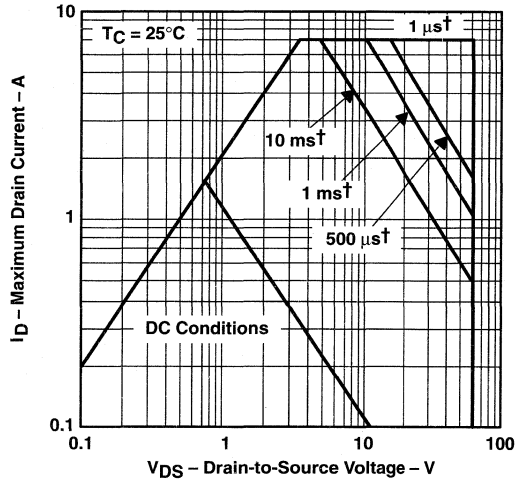


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

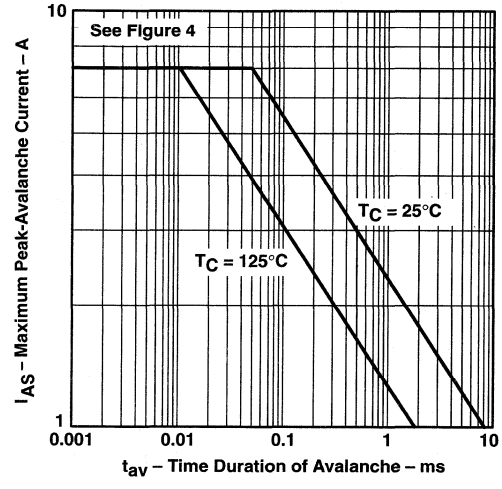


Figure 16

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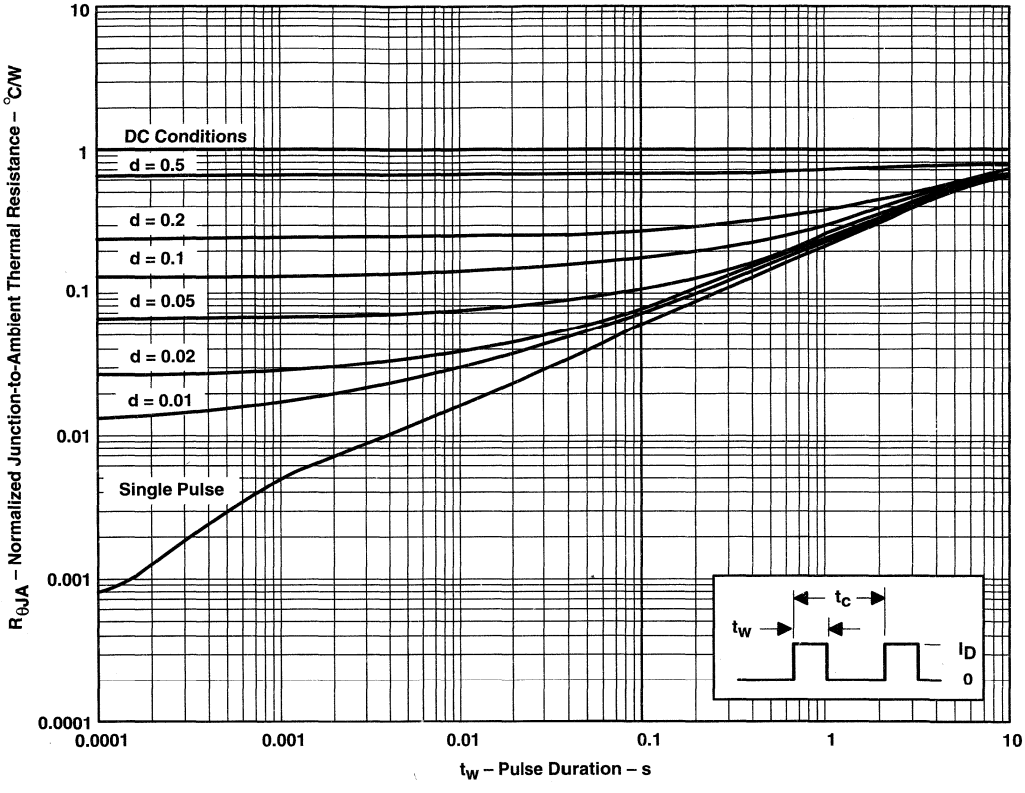
THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



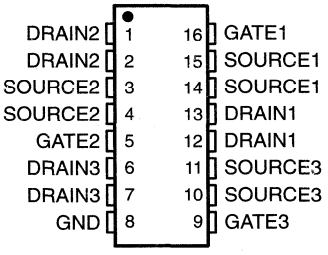
† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 5 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)

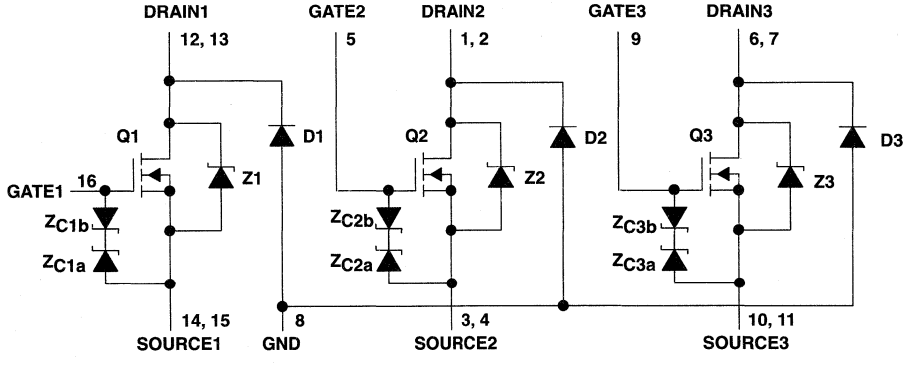


description

The TPIC5303 is a monolithic gate-protected power DMOS array that consists of three independent electrically isolated N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5303 is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal pin may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q1, Q2, and Q3)	100 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1.4 A
Continuous source-to-drain diode current, T_C = 25°C	1.4 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	5 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	10.2 mJ
Continuous total power dissipation, T_C = 25°C (see Figure 15)	1.08 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.8	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.4 A, V_{GS} = 10 V, See Notes 2 and 3			0.56	0.64	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.4 A, V_{GS} = 0 (Z1, Z2, Z3), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.4 A (D1, D2, D3), See Notes 2 and 3			5		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1.4 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.46	Ω
			T_C = 125°C		0.62	0.66	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.7 A, See Notes 2 and 3 and Figure 9		1	1.19		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			107	137	pF
C_{oss}	Short-circuit output capacitance, common source				71	89	
C_{rss}	Short-circuit reverse transfer capacitance, common source				22	28	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.7 A, V_{GS} = 0, See Figures 1 and 14	Z1, Z2, and Z3		92		ns
		V_{DS} = 48 V, di/dt = 100 A/µs,	D1, D2, and D3		244		
Q_{RR}	Total diode charge		Z1, Z2, and Z3		0.1		µC
			D1, D2, and D3		1.3		

resistive-load switching characteristics, T_C = 25°C

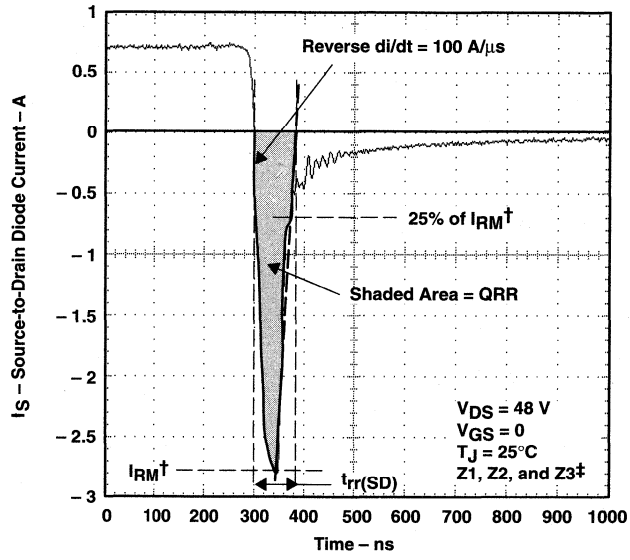
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{f1} = 10 ns,	R_L = 36 Ω, See Figure 2	t_{r1} = 10 ns,		25	40	ns
$t_{d(off)}$	Turn-off delay time					27	40	
t_{r2}	Rise time					15	25	
t_{f2}	Fall time					7	14	
Q_g	Total gate charge	V_{DS} = 48 V, See Figure 3	I_D = 0.7 A,	V_{GS} = 10 V,		2.1	2.6	nC
$Q_{gs(th)}$	Threshold gate-to-source charge					0.3	0.38	
Q_{gd}	Gate-to-drain charge					1.2	1.5	
L_D	Internal drain inductance					5		nH
L_S	Internal source inductance					5		
R_g	Internal gate resistance					0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		115		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		64		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		33		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 inch^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

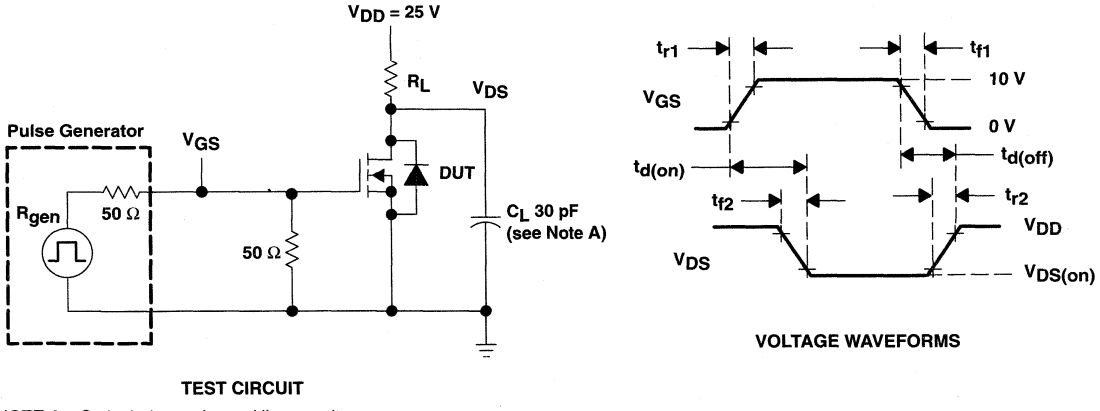
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

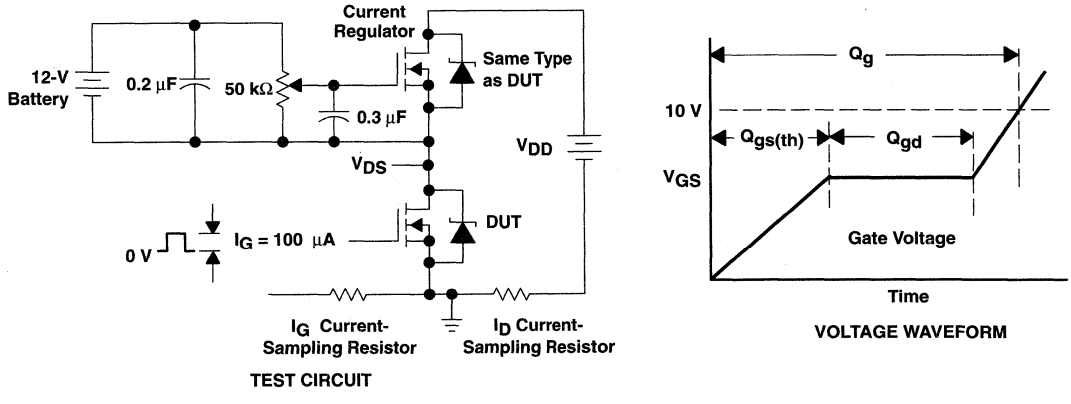
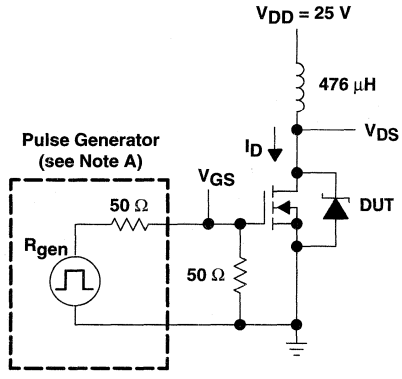
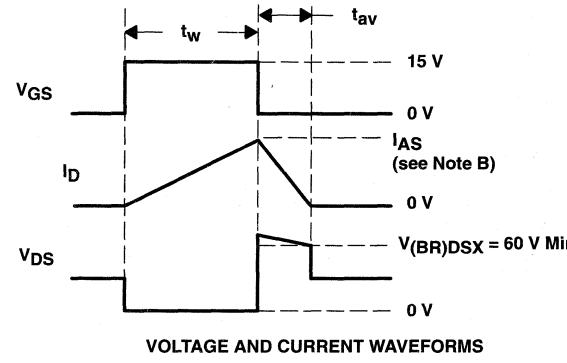


Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 10.2$ mJ, where

t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

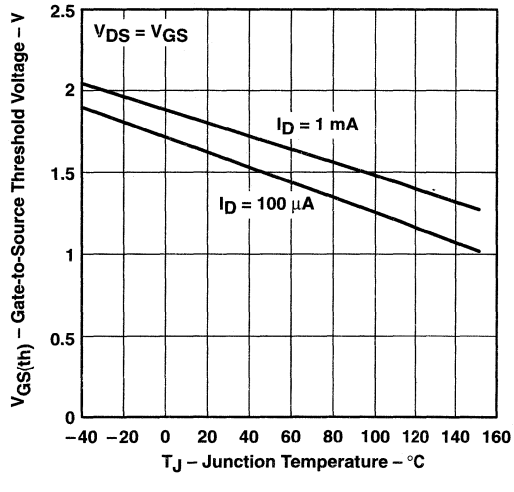


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

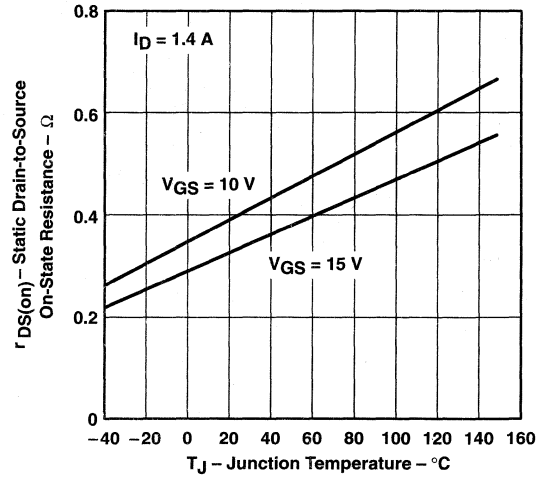


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

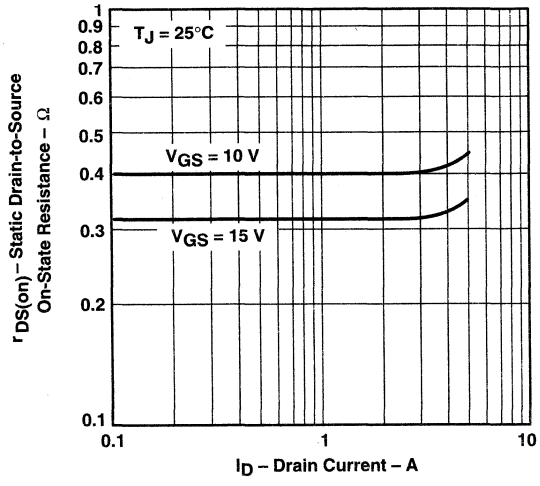


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

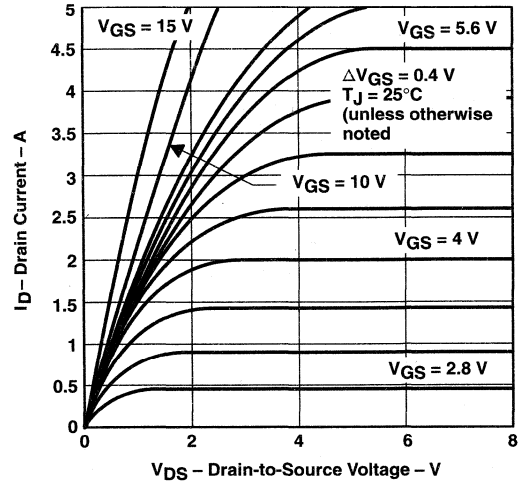


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

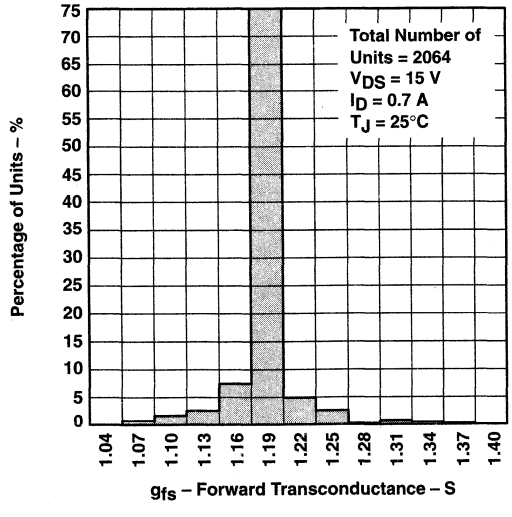


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

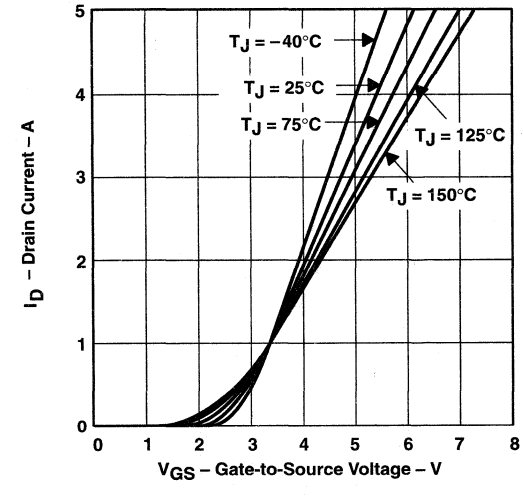


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

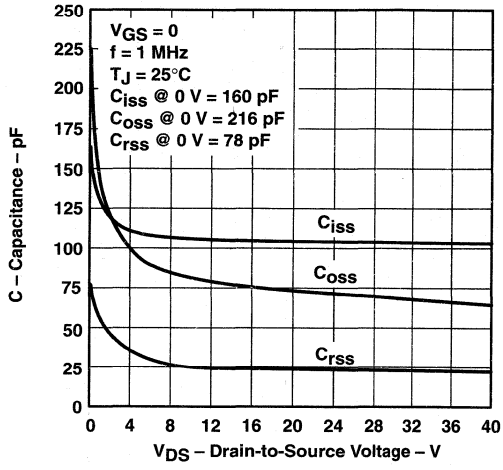


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

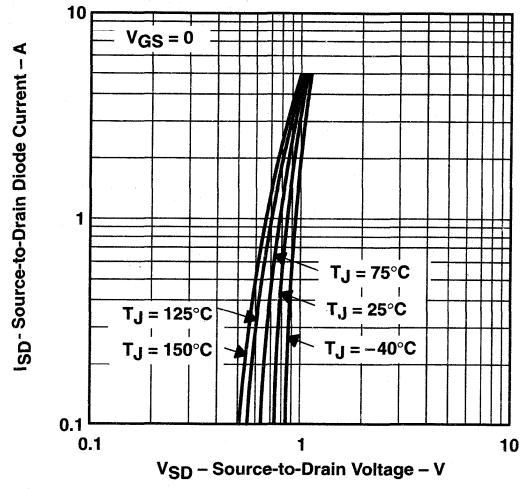


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

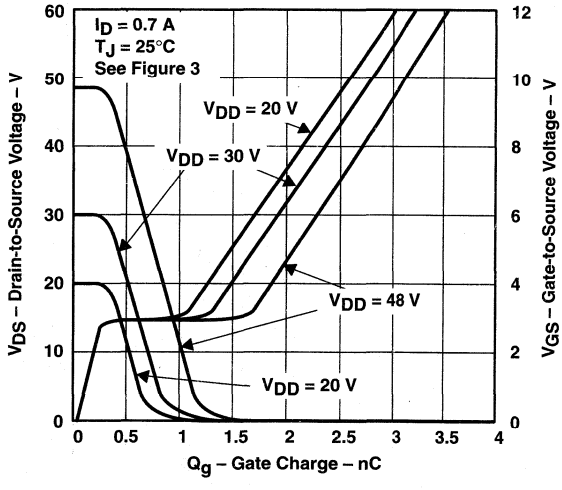


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

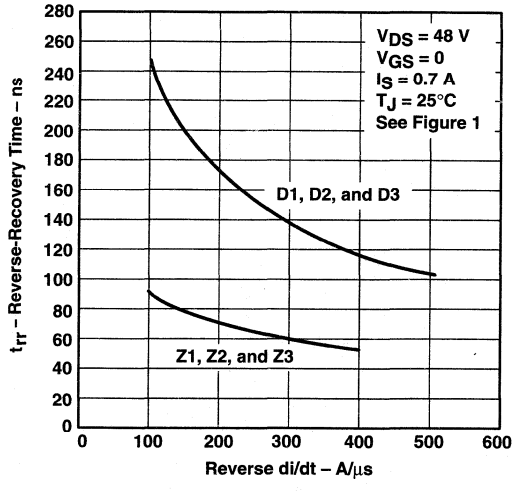


Figure 14

TEXAS INSTRUMENTS
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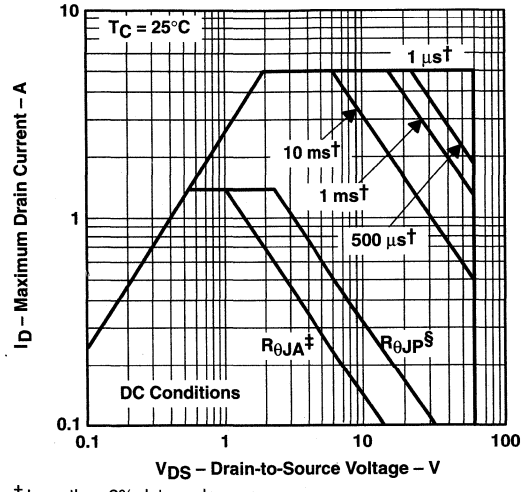
THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
§ Device mounted in intimate contact with infinite heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

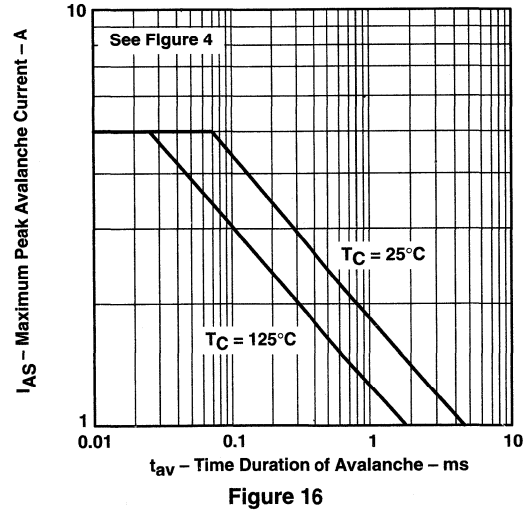
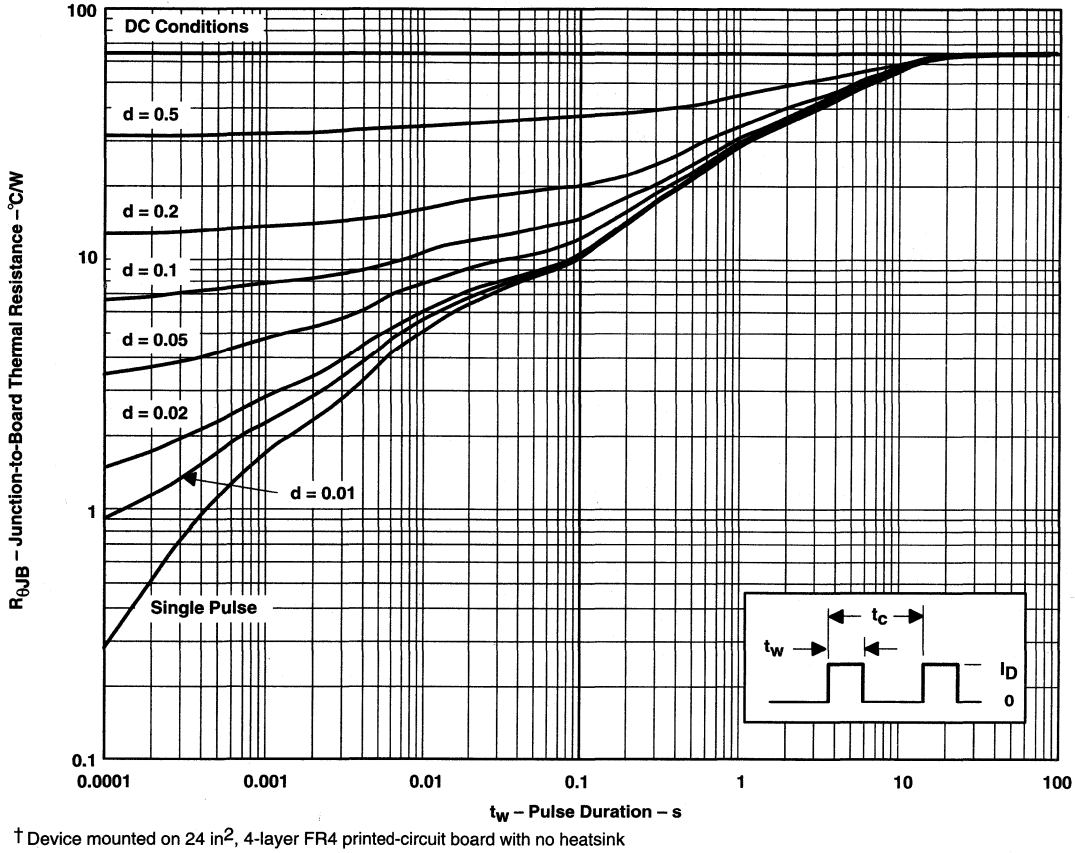


Figure 16

THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink

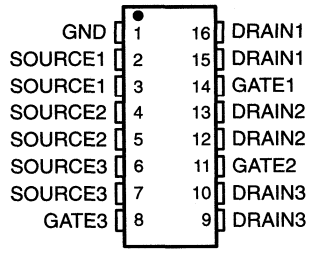
NOTE A: $Z_{\theta JB}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

- **Low $r_{DS(on)}$ . . . 0.45 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)

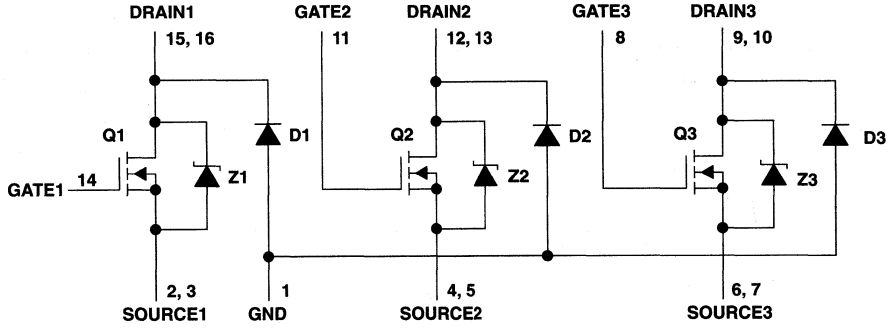


description

The TPIC5322L is a monolithic logic-level power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors.

The TPIC5322L is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	40.5 mJ
Continuous total power dissipation at (or below) T_C = 25°C	1.09 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.45	0.525	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0, See Notes 2 and 3 and Figure 12			0.85	1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A			3.7		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.45	0.525	Ω
			T_C = 125°C		0.7	0.78	
g_{fs}	Forward transconductance	V_{DS} = 10 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		1	1.24		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			135	170	pF
C_{oss}	Short-circuit output capacitance, common source				80	100	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.5 A, V_{DS} = 48 V, V_{GS} = 0, di/dt = 100 A/µs, See Figures 1 and 14	Z1, Z2, Z3		35		ns
			D1, D2, D3		110		
Q_{RR}	Total diode charge		Z1, Z2,Z3		0.035		µC
			D1, D2, D2		0.35		

resistive-load switching characteristics, T_C = 25°C

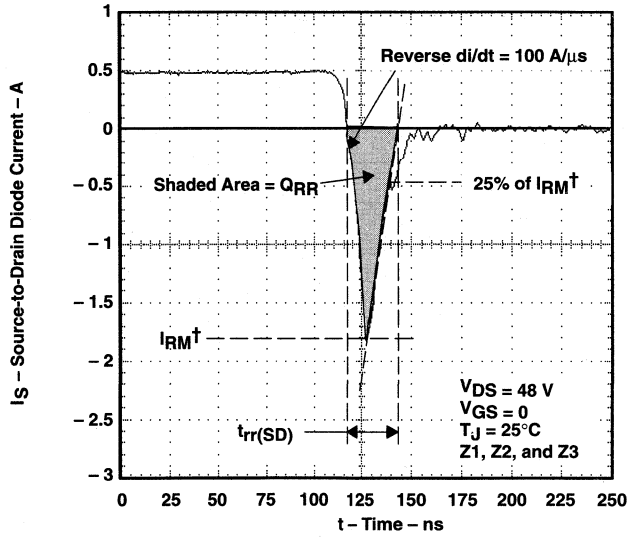
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		21	42	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_r	Rise time			5	10	
t_f	Fall time			13	26	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 5 V, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
Q_{gd}	Gate-to-drain charge			1.3	1.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	All outputs with equal power		115		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			32		°C/W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

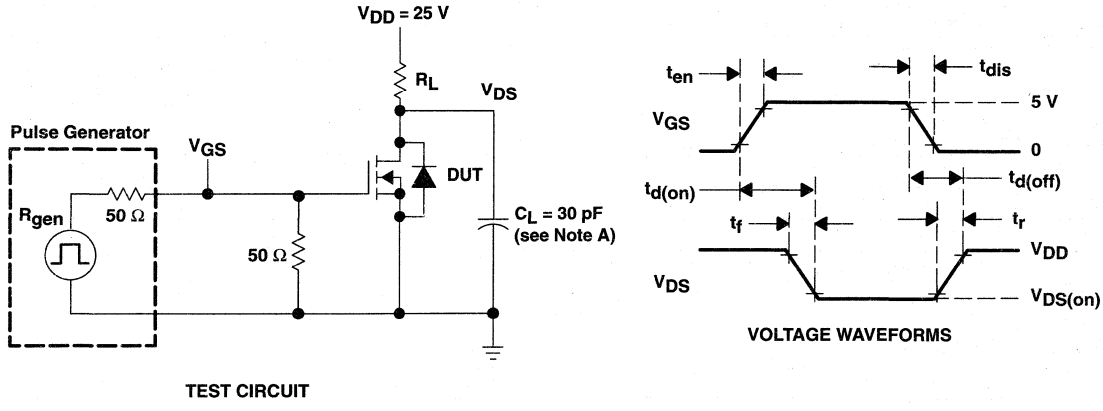
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
NOTE A. The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

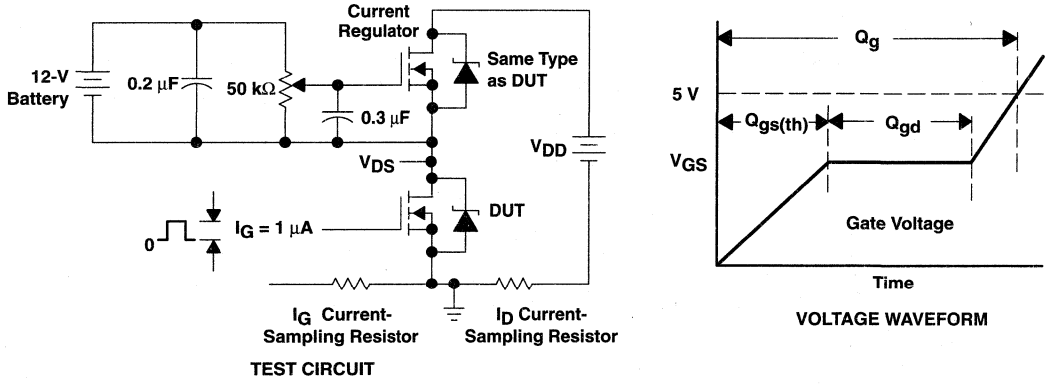
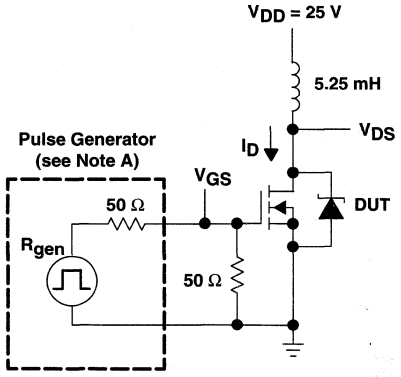
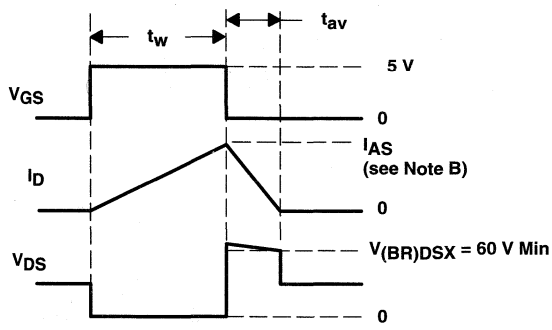


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 40.5$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

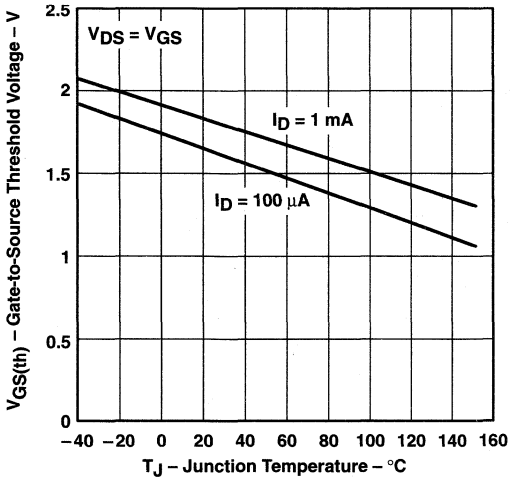


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

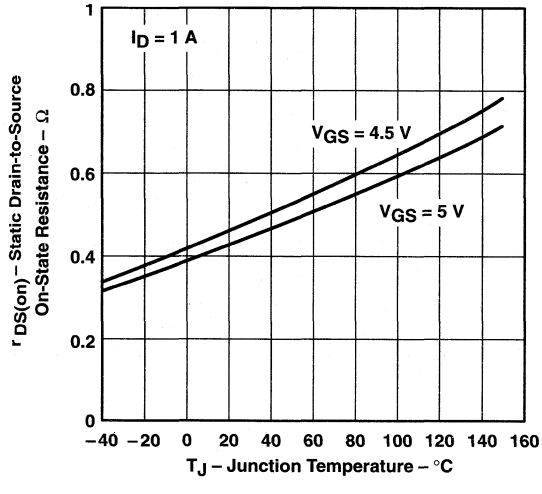


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

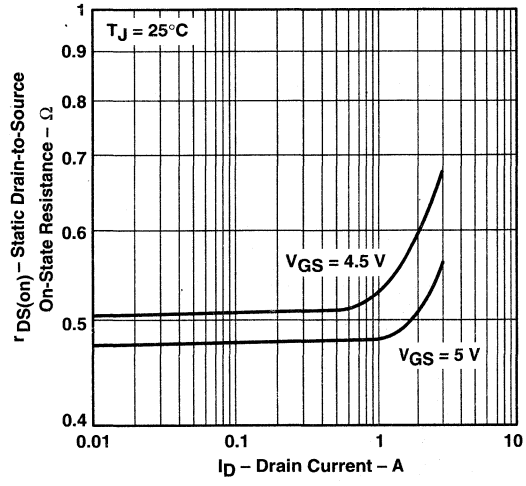


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

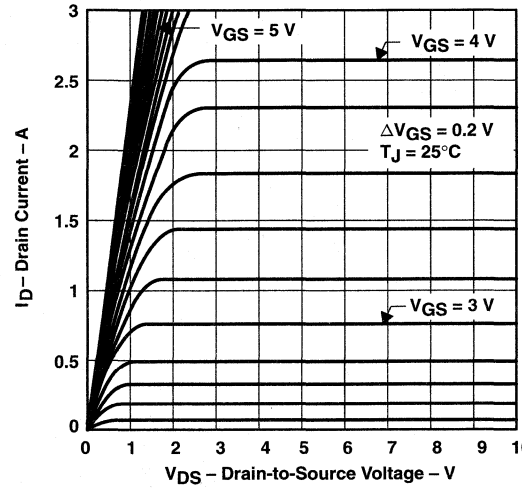


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

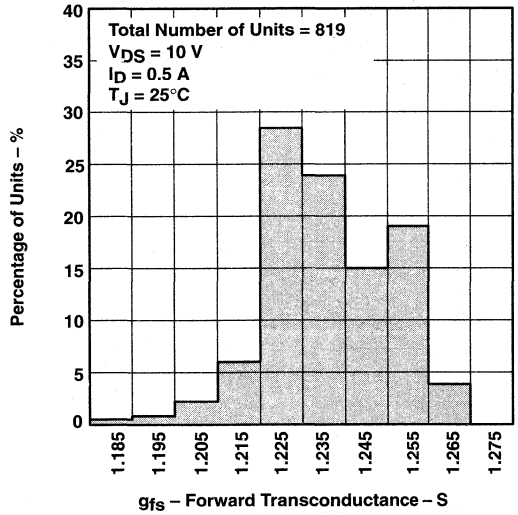


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

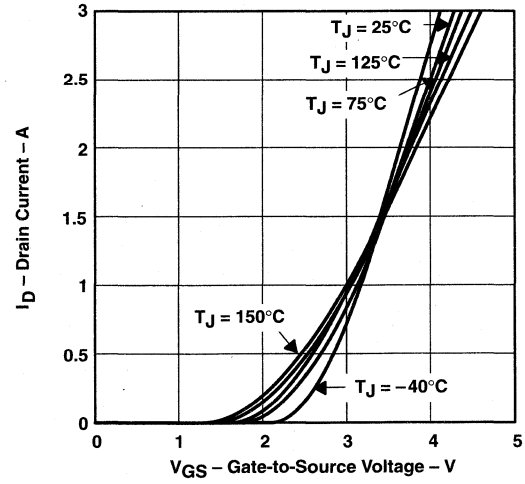


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

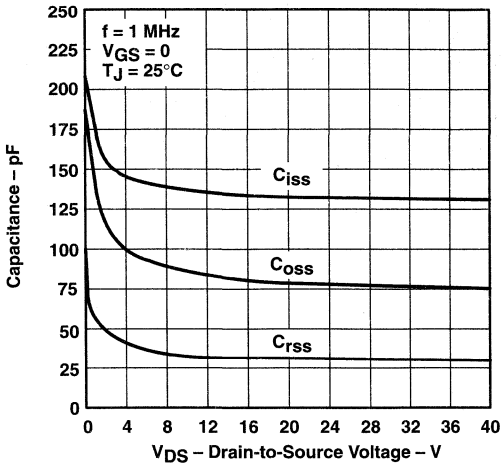


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

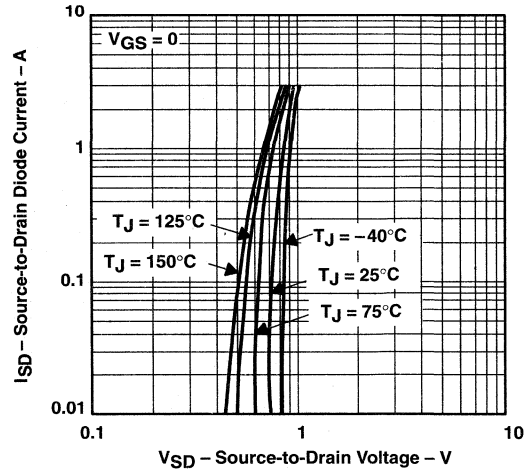


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

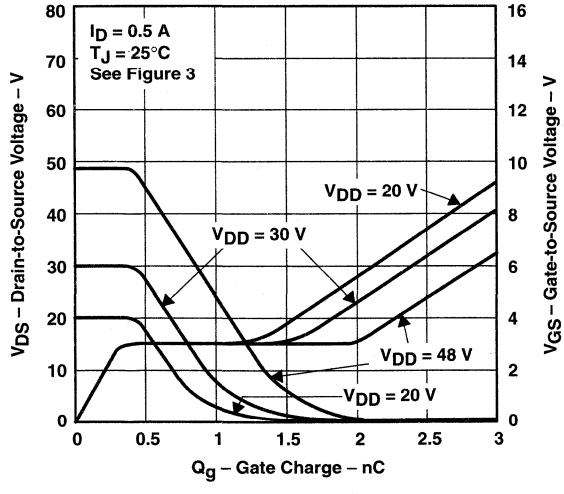


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

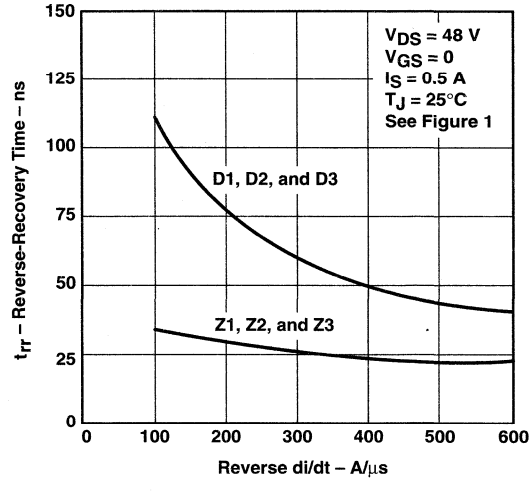
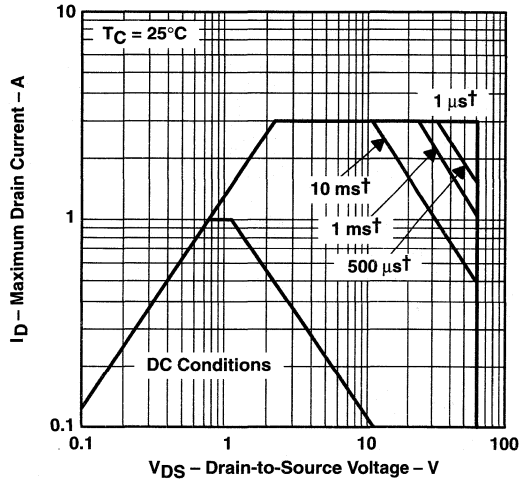


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

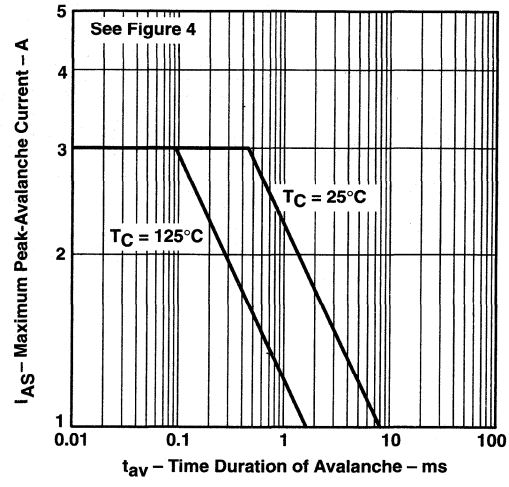
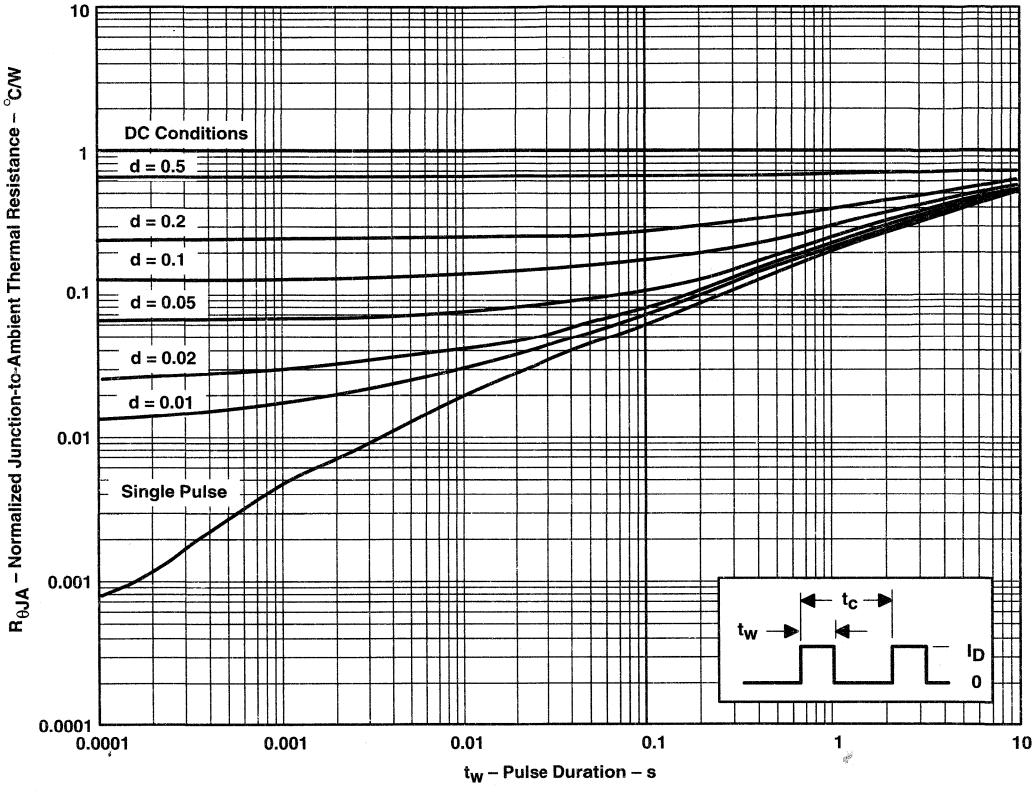


Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



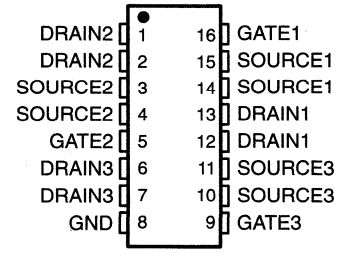
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

- **Low $r_{DS(on)}$ . . . 0.6 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

D PACKAGE
(TOP VIEW)

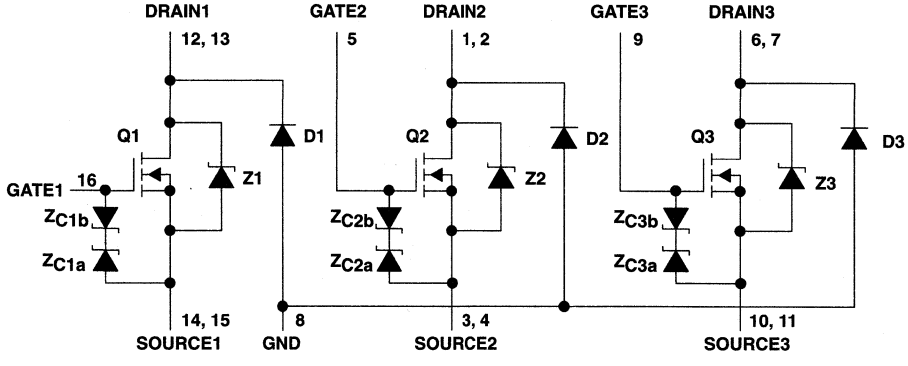


description

The TPIC5323L is a monolithic gate-protected logic-level power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5323L is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal can be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	22.5 mJ
Continuous total power dissipation, T_C = 25°C (see Figure 15)	1.09 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.8	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.6	0.7	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2, D3), See Notes 2 and 3			4		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.6	0.65	Ω
			T_C = 125°C		0.85	0.9	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 500 mA, See Notes 2 and 3 and Figure 9		0.89	1.06		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			107	137	pF
C_{oss}	Short-circuit output capacitance, common source				71	89	
C_{rss}	Short-circuit reverse transfer capacitance, common source				22	28	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 500 mA, V_{GS} = 0, See Figures 1 and 14 V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, and Z3		75		ns
			D1, D2, and D3		190		
Q_{RR}	Total diode charge		Z1, Z2, and Z3		0.08		µC
			D1, D2, and D3		0.85		

resistive-load switching characteristics, T_C = 25°C

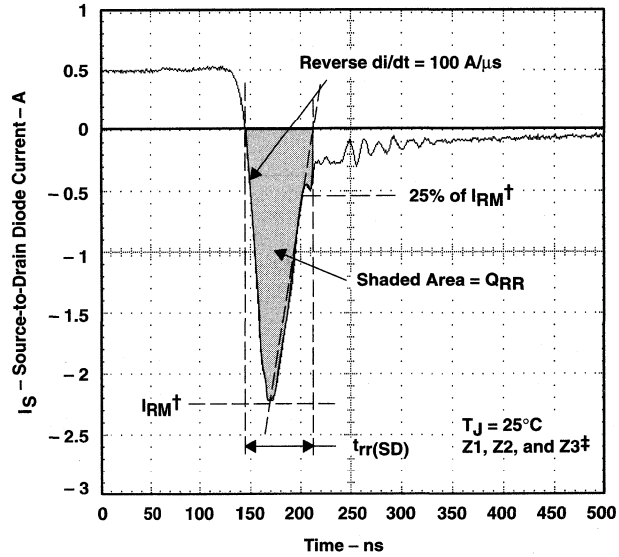
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		34	50	ns
$t_{d(off)}$	Turn-off delay time			50	70	
t_{r2}	Rise time			20	30	
t_{f2}	Fall time			15	25	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 500 mA, V_{GS} = 5 V, See Figure 3		2	2.45	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.3	0.95	
Q_{gd}	Gate-to-drain charge			1.2	1.48	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		115		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		64		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		33		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power

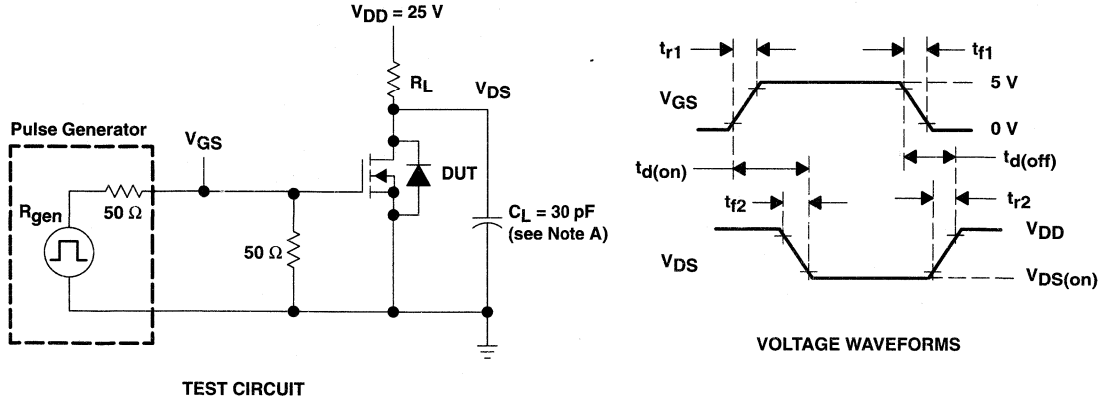
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

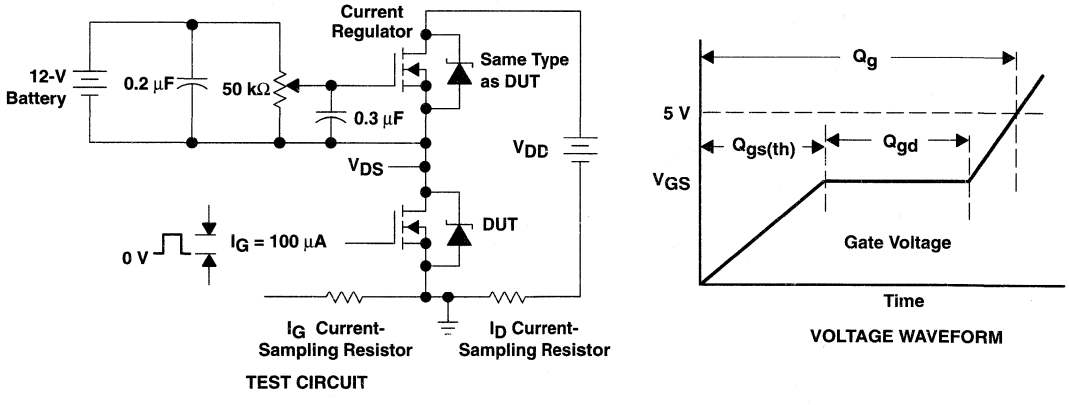
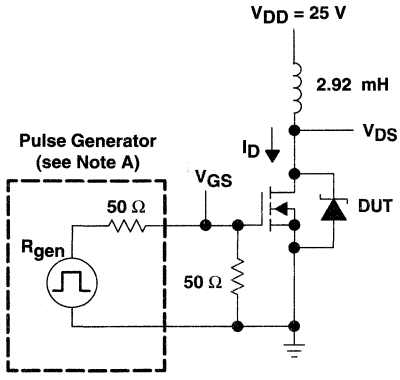
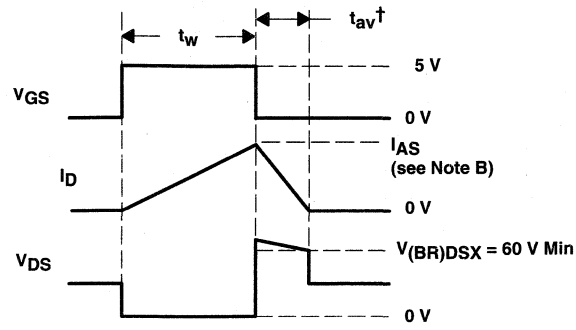


Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22.5$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

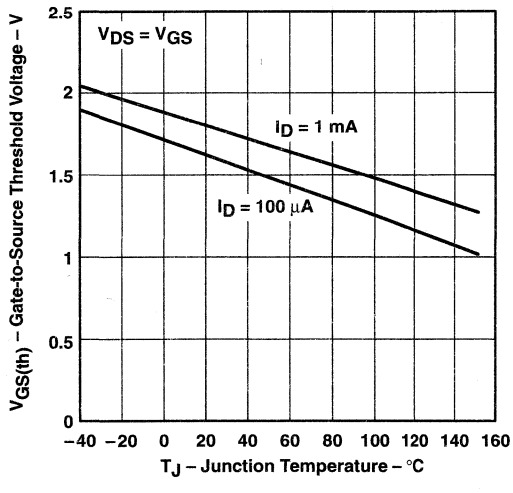


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

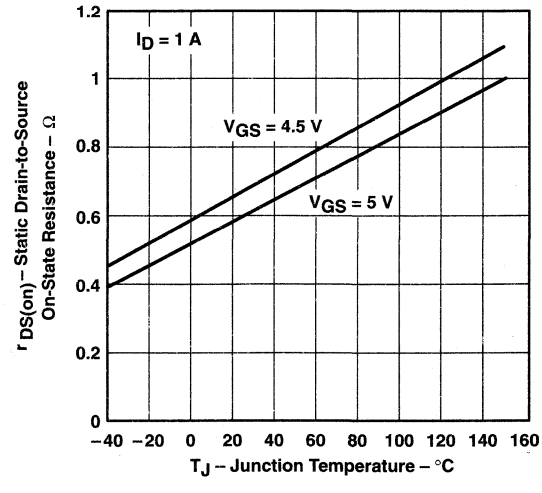


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

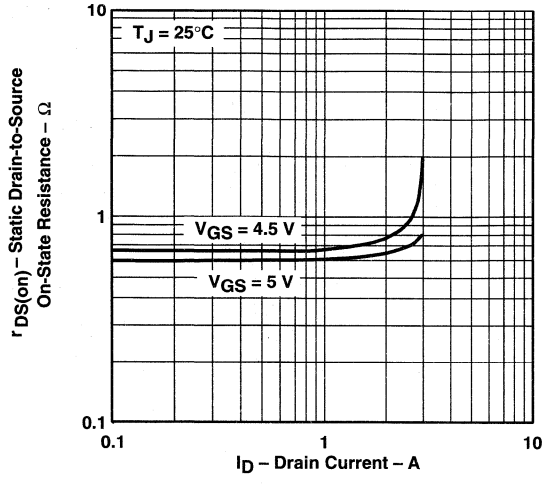


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

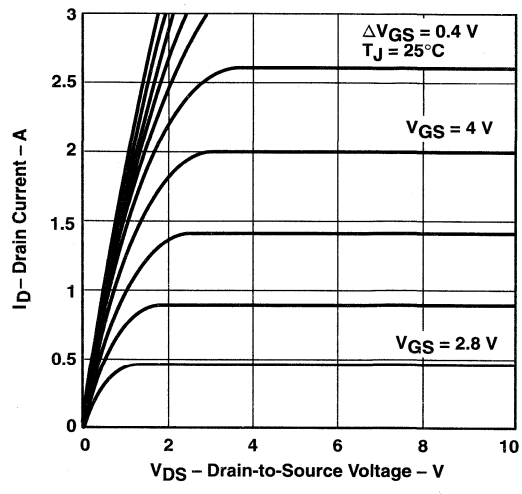


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

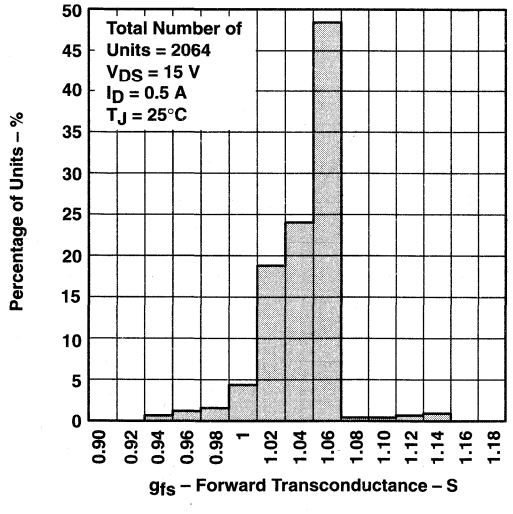


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

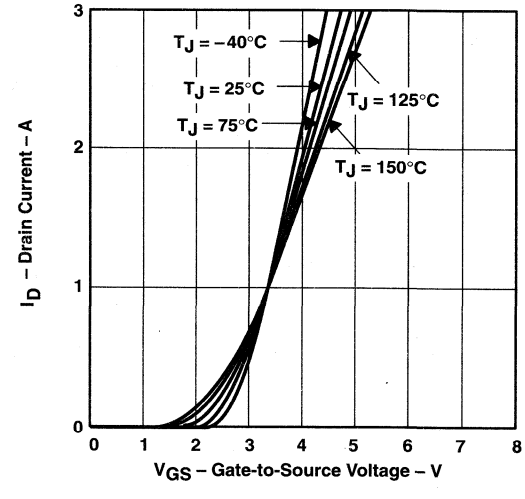


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

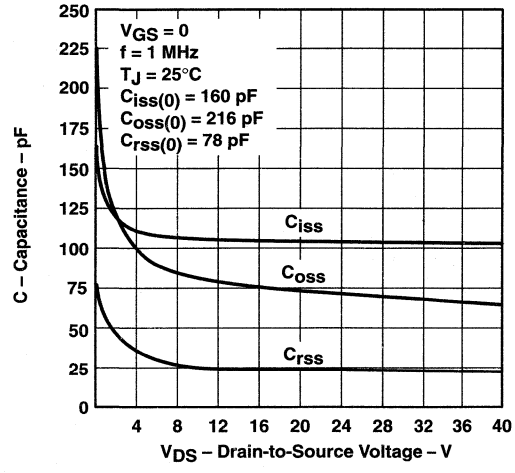


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

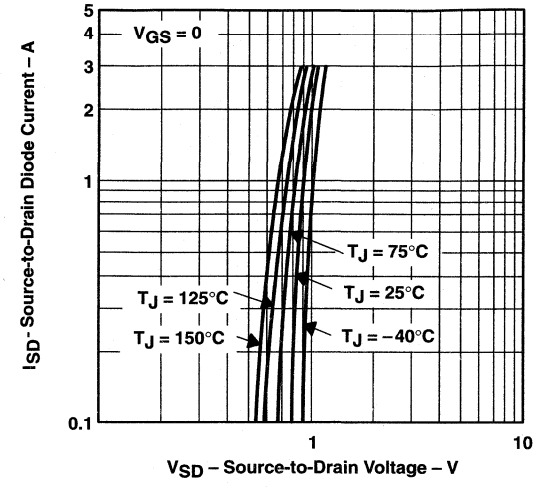


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

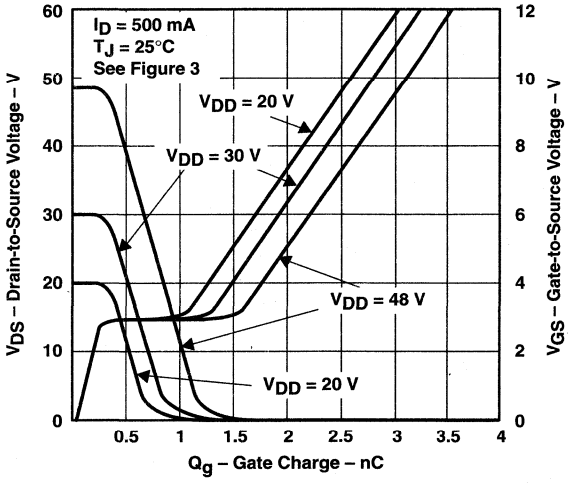


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

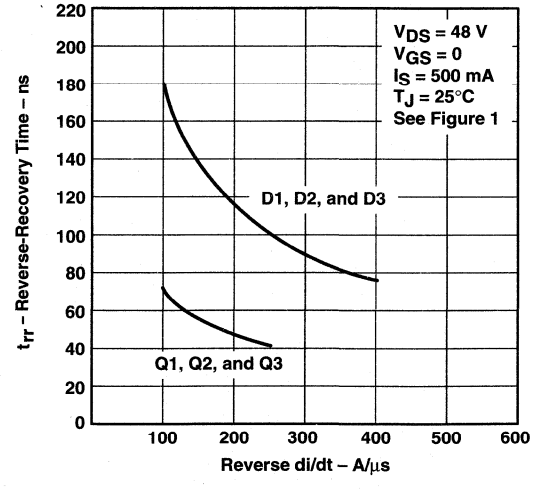
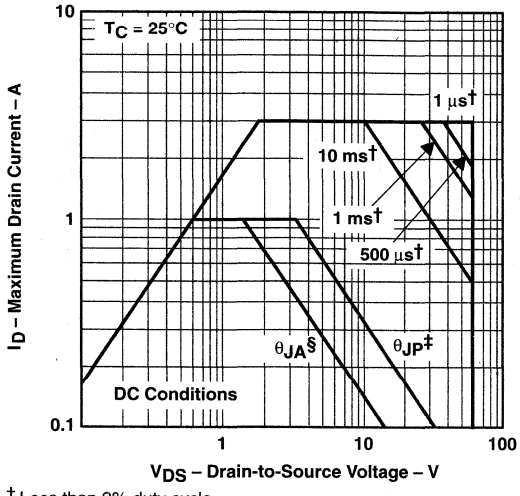


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted in intimate contact with infinite heatsink.
§ Device mounted on FR4 printed-circuit board with no heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

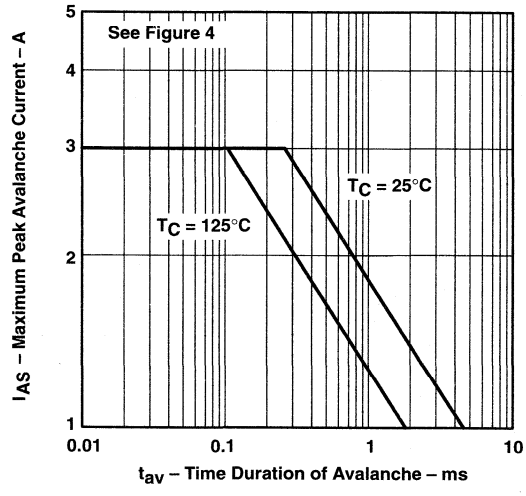
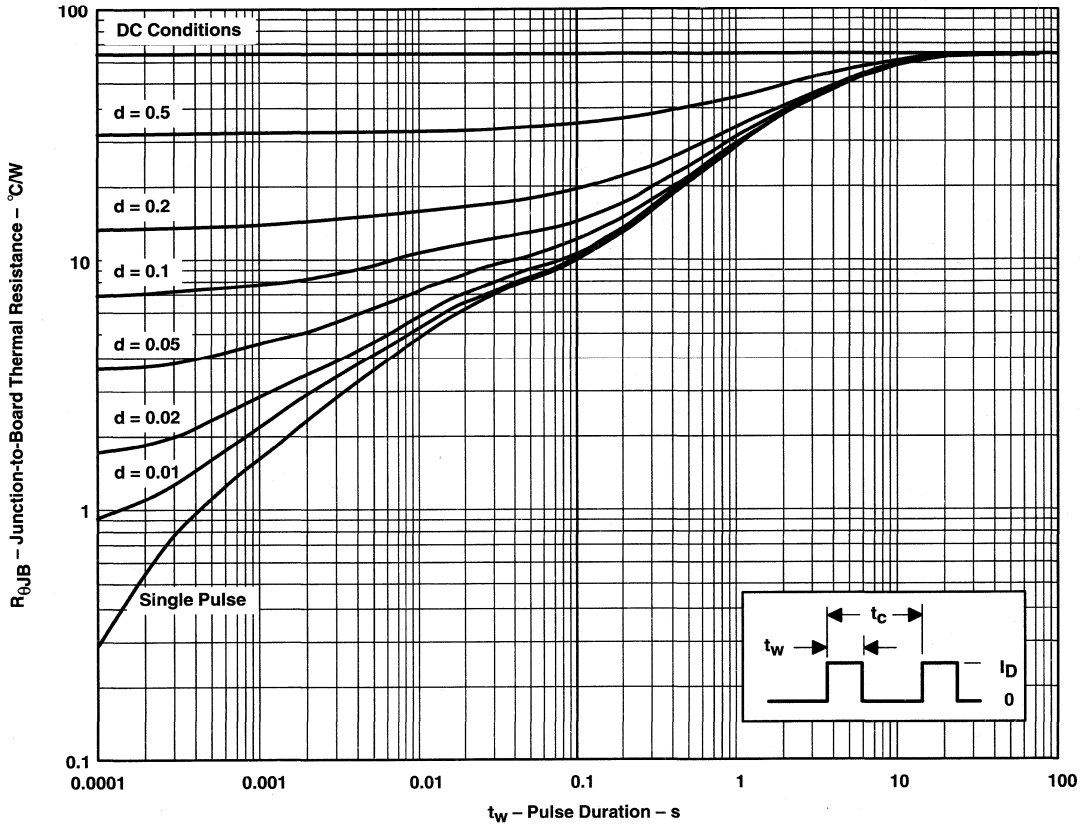


Figure 16

THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 17

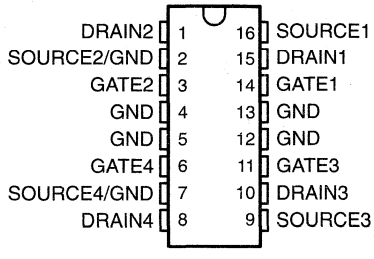
- **Low $r_{DS(on)}$ . . . 0.3 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 10 A Per Channel**
- **Fast Commutation Speed**

description

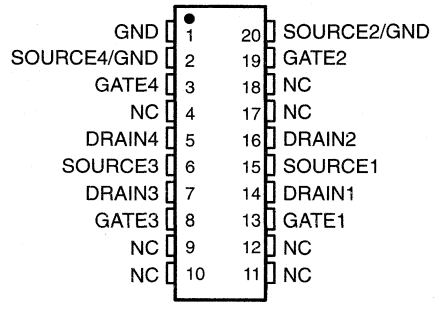
The TPIC5401 is a monolithic gate-protected power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5401 is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of −40°C to 125°C.

NE PACKAGE
(TOP VIEW)

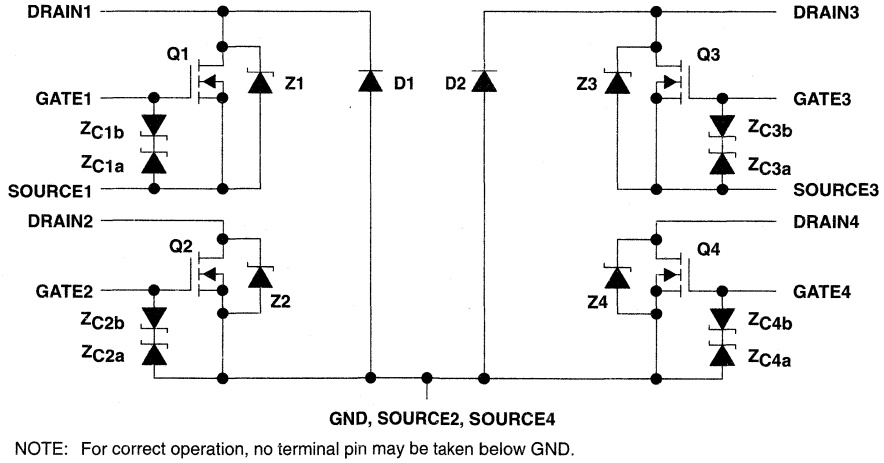


DW PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C: DW package	1.7 A
NE package	2 A
Continuous source-to-drain diode current, T_C = 25°C	2 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	10 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	21 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.85	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, See Notes 2 and 3	V_{GS} = 10 V,		0.6	0.7	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2 A (D1, D2), See Notes 2 and 3			7.5		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V,	V_{DS} = 0		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.47	0.5	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 1 A,	1.6	1.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs, Z1 and Z3		120		ns
			Z2 and Z4		280		
			D1 and D2		260		
Q_{RR}	Total diode charge		Z1 and Z3		0.12		µC
			Z2 and Z4		0.9		
			D1 and D2		2.2		

resistive-load switching characteristics, T_C = 25°C

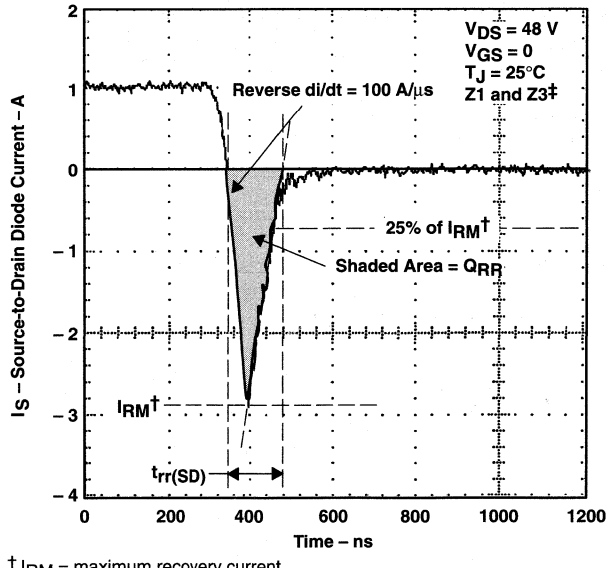
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		32	65	ns
$t_{d(off)}$	Turn-off delay time			40	80	
t_r	Rise time			15	30	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.8	1	
Q_{gd}	Gate-to-drain charge			2.6	3.2	
L_d	Internal drain inductance			5		nH
L_s	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistances

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	DW	All outputs with equal power		90		°C/W
		NE			60		
$R_{\theta JB}$	Junction-to-board thermal resistance	DW			53		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW			30		
		NE			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heatsink.

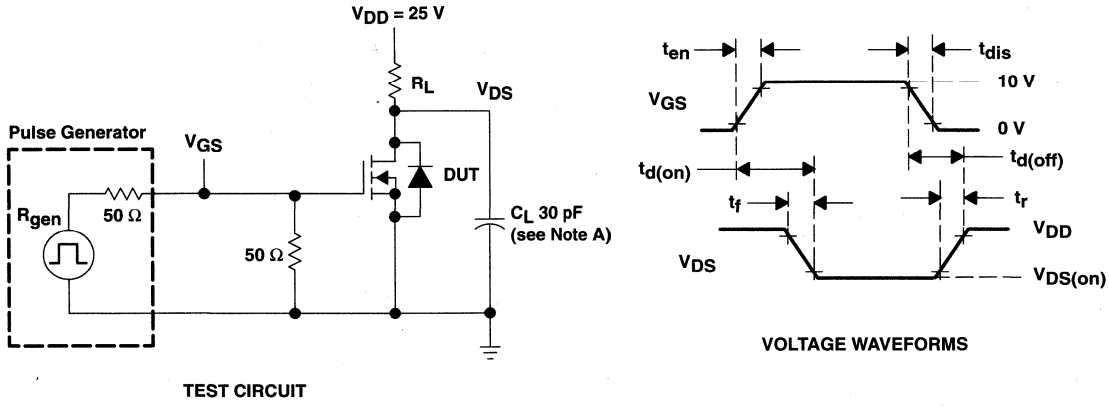
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

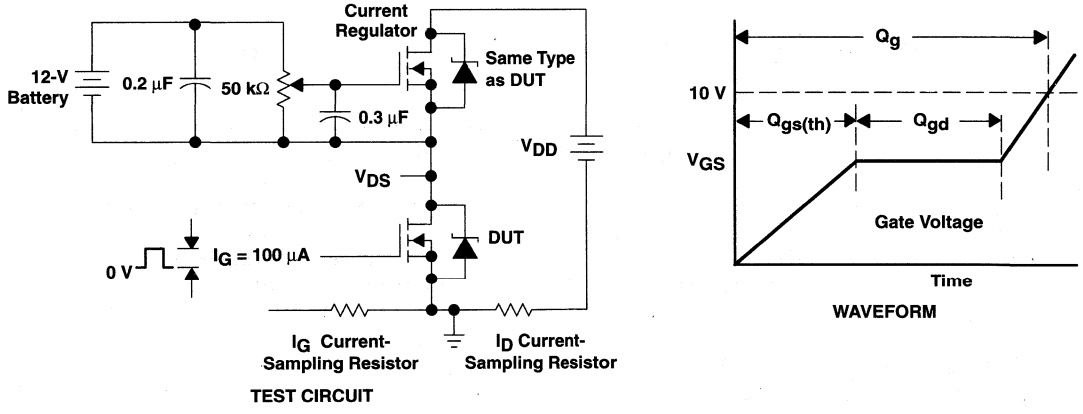
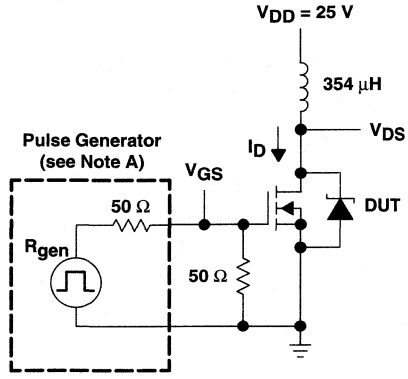
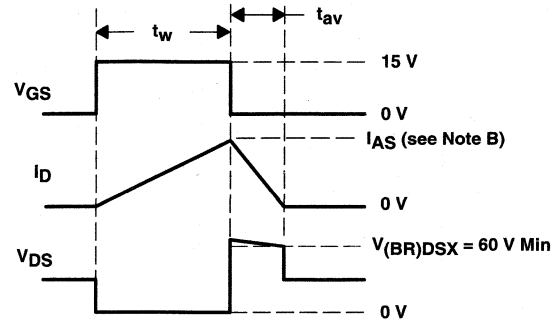


Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 10$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

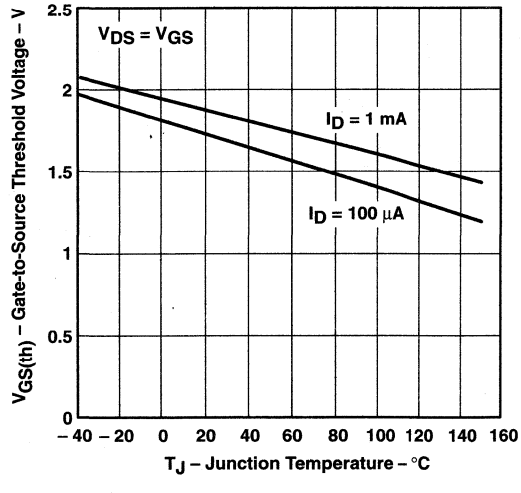


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

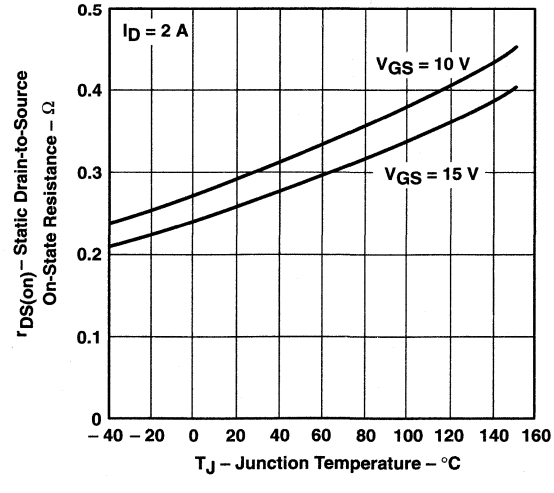


Figure 6

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

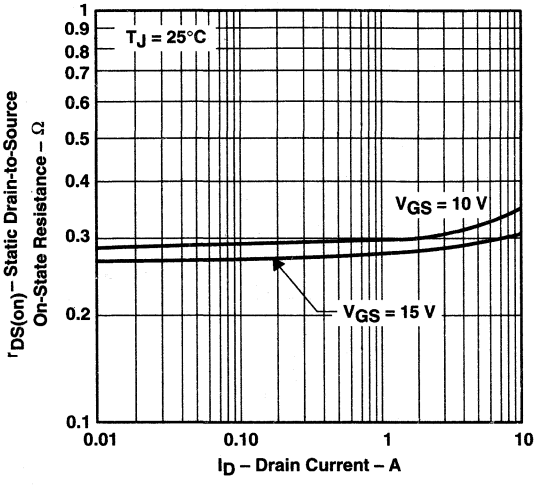


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

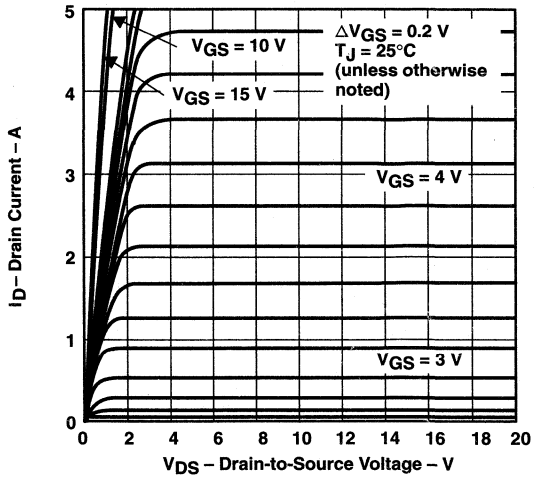


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

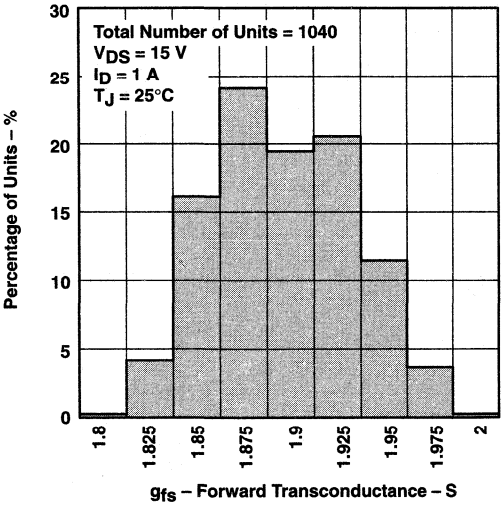


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

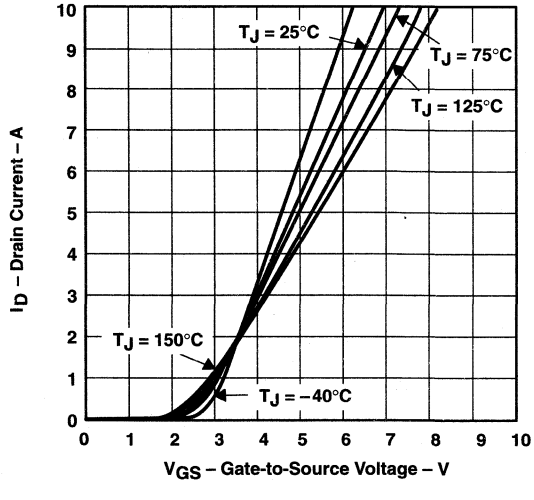


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

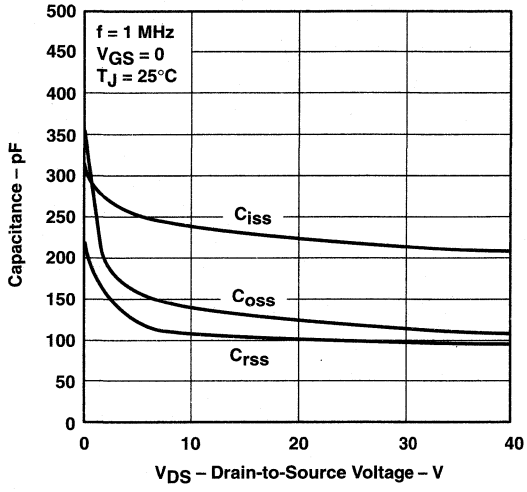


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

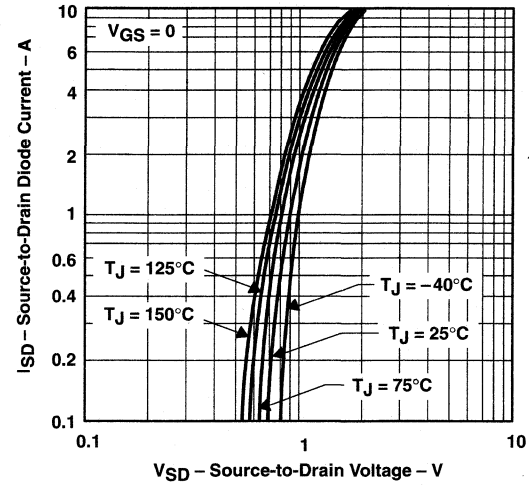


Figure 12

DRAIN-TO-SOURCE VOLTAGE
AND GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

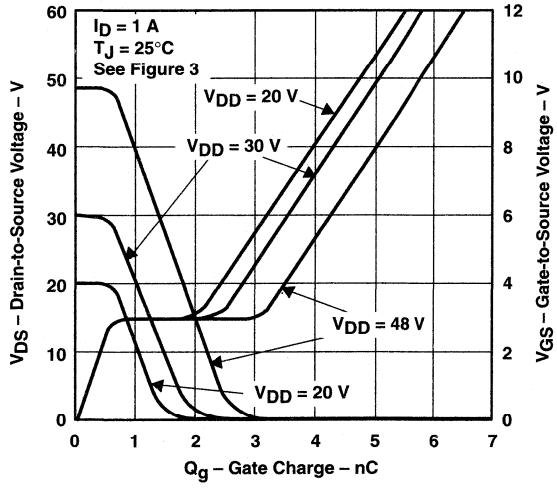


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

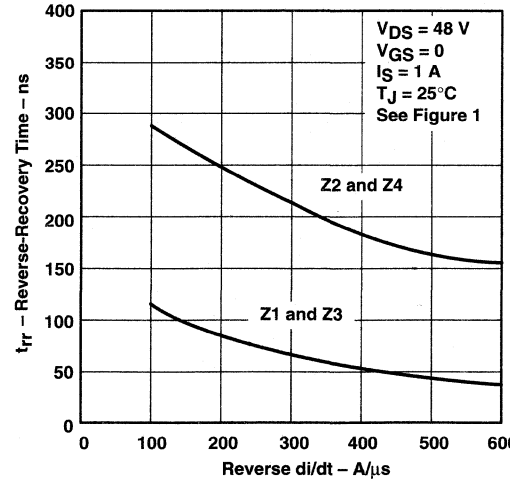
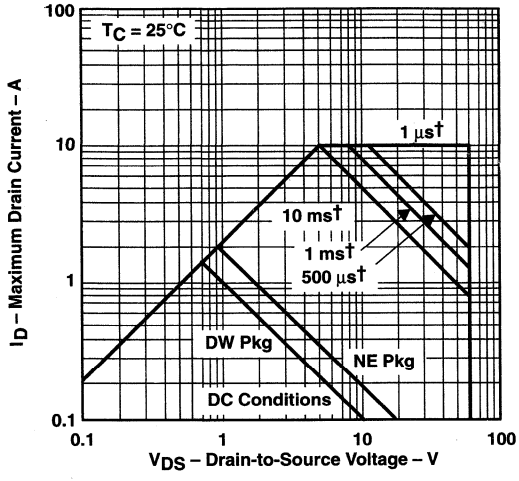


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

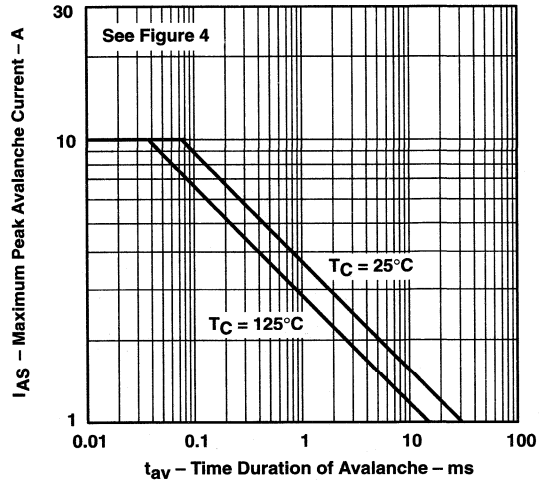
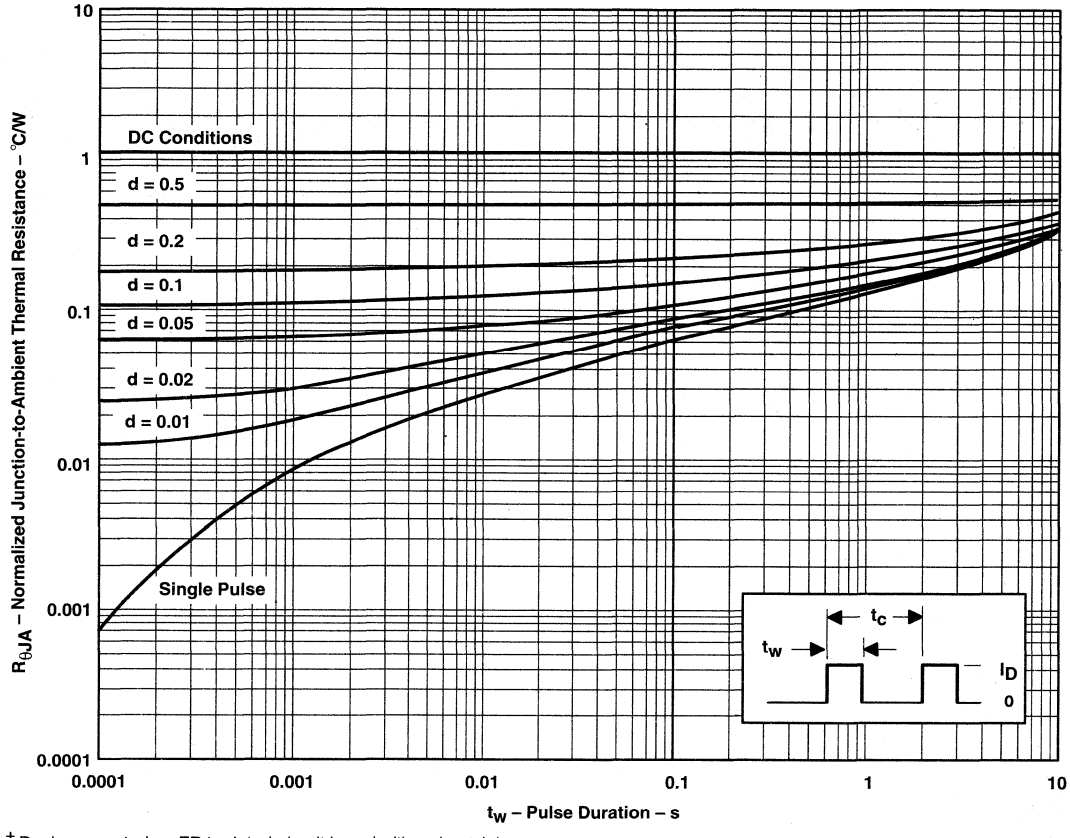


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



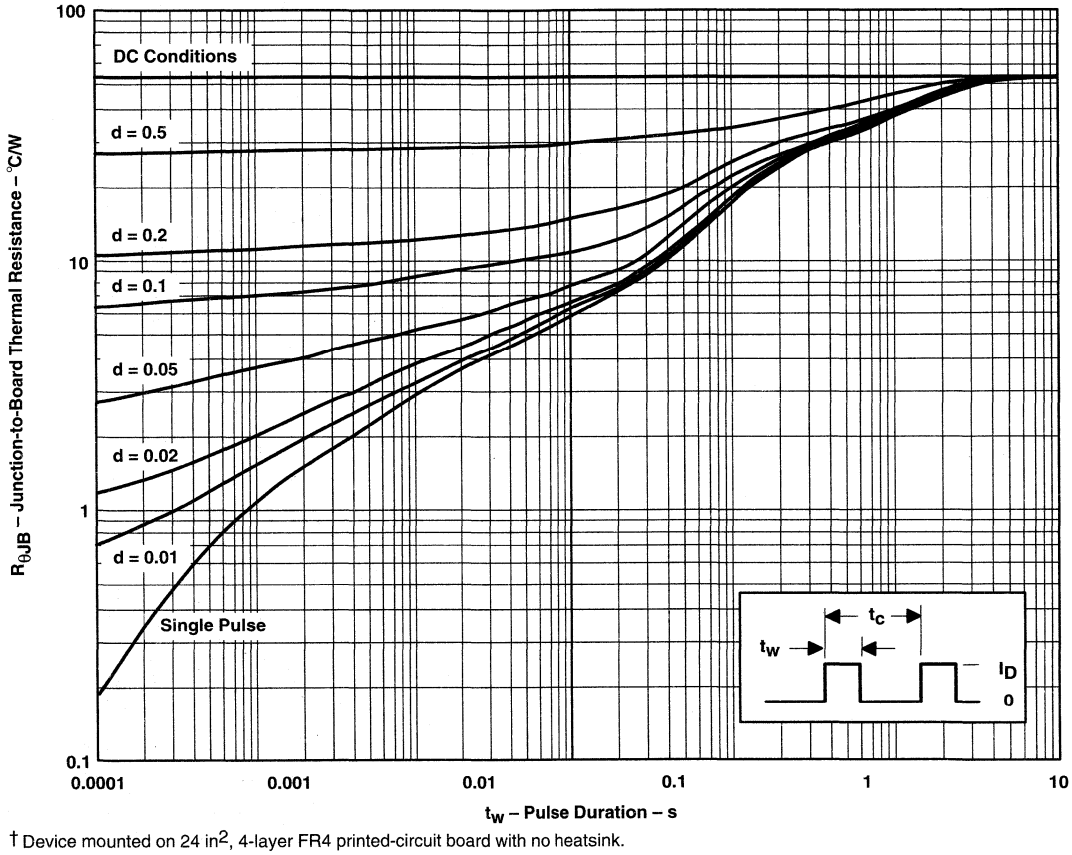
† Device mounted on FR4 printed-circuit board with no heatsink.

NOTE A. $Z_{\theta JA}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 17

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



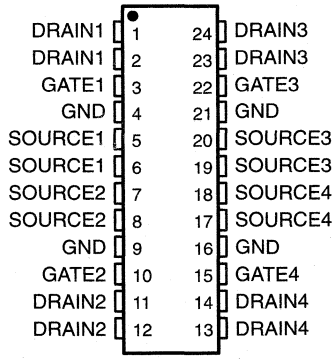
† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE B. $Z_{\theta JB}(t) = r(t)\ R_{\theta JB}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 18

- **Low $r_{DS(on)}$ . . . 0.23 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 11.25 A Per Channel**
- **Fast Commutation Speed**

DW PACKAGE
(TOP VIEW)

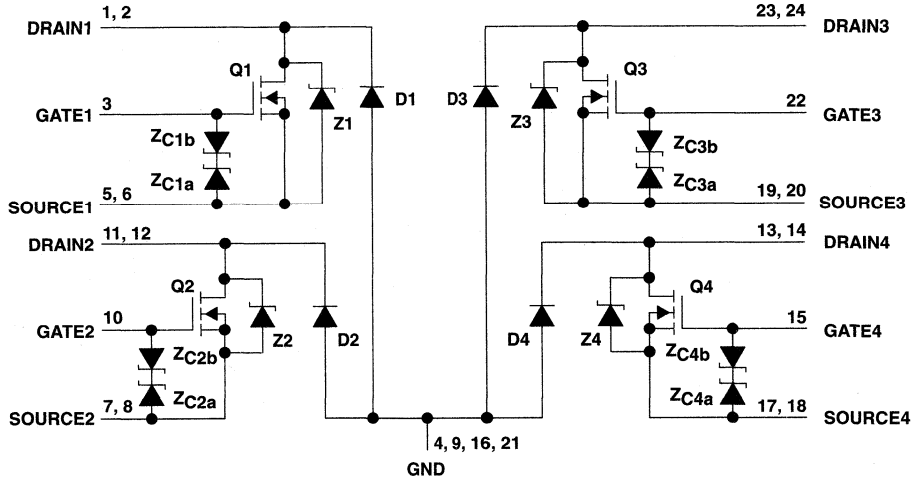


description

The TPIC5403 is a monolithic gate-protected power DMOS array that consists of four independent electrically isolated N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5403 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	2.25 A
Continuous source-to-drain diode current, T_C = 25°C	2.25 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	11.25 A
Continuous gate-to-source zener diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	17.2 mJ
Continuous total power dissipation, T_C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3, and D4)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2.25 A, See Notes 2 and 3	V_{GS} = 10 V,		0.5	0.62	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2.25 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2.25 A (D1, D2, D3, D4), See Notes 2 and 3			2.5		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 15 V,	V_{DS} = 0		20	200	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2.25 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.23	0.27	Ω
			T_C = 125°C		0.35	0.4	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 1.125 A,	1.6	2.1		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		200	250	pF
C_{oss}	Short-circuit output capacitance, common source				100	175	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				60	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1.125 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1, Z2, Z3, and Z4		80		ns
				D1, D2, D3, and D4		160		
Q_{RR}	Total diode charge			Z1, Z2, Z3, and Z4		0.12		µC
				D1, D2, D3, and D4		0.5		

resistive-load switching characteristics, T_C = 25°C

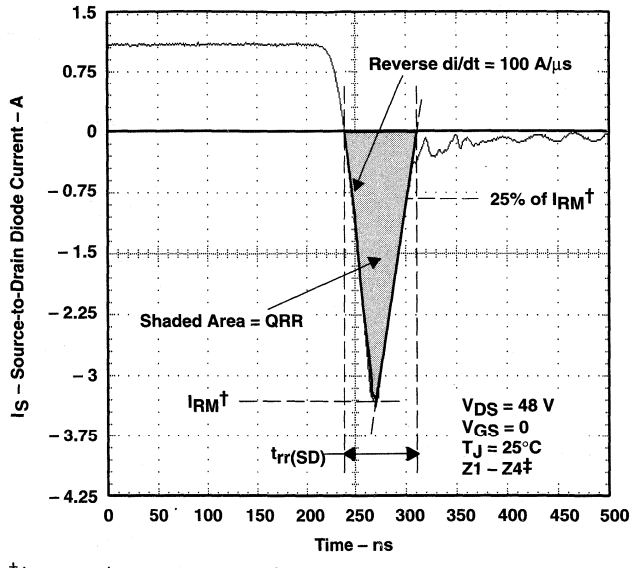
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 20 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		32	55	ns
$t_{d(off)}$	Turn-off delay time			27	50	
t_{r2}	Rise time			14	30	
t_{f2}	Fall time			7	15	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1.125 A, V_{GS} = 10 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.6	0.7	
Q_{gd}	Gate-to-drain charge			2.8	3.2	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		49		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		°C/W

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink
5. Package mounted on a 24 inch^2, 4-layer FR4 printed-circuit board
6. Package mounted in intimate contact with infinite heatsink
7. All outputs with equal power

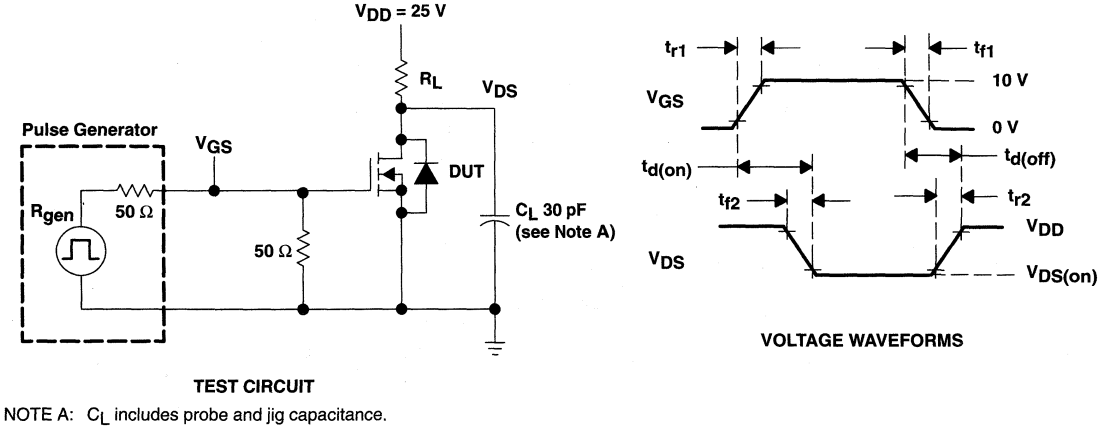
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

‡ The above waveform is representative of D1, D2, D3, and D4 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

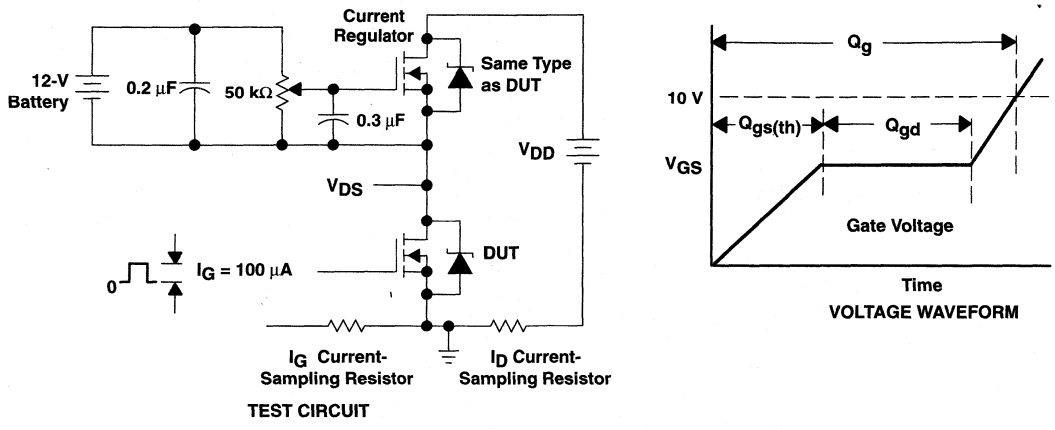
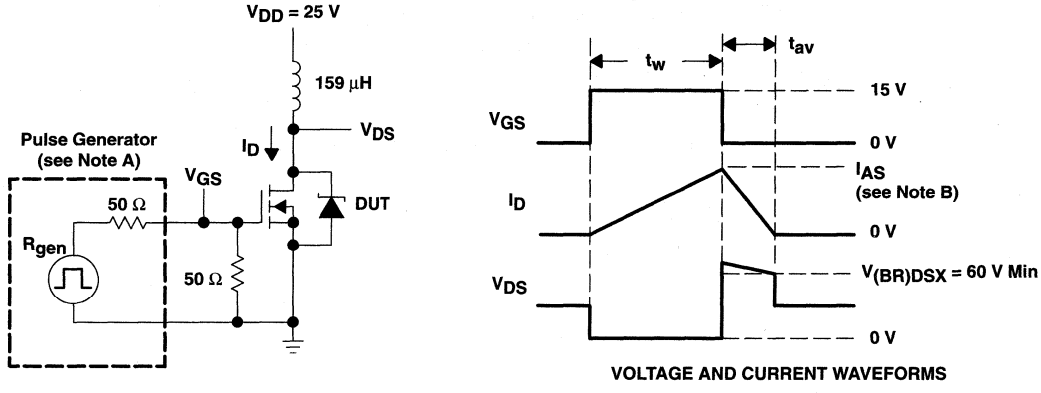


Figure 3. Gate-Charge Test Circuit and Voltage Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 11.25$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 17.2$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

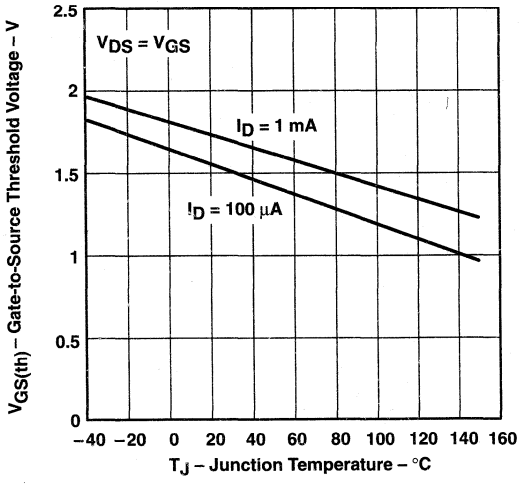


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

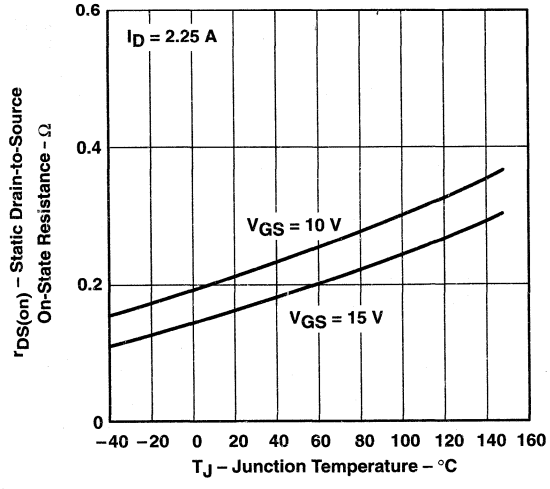


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

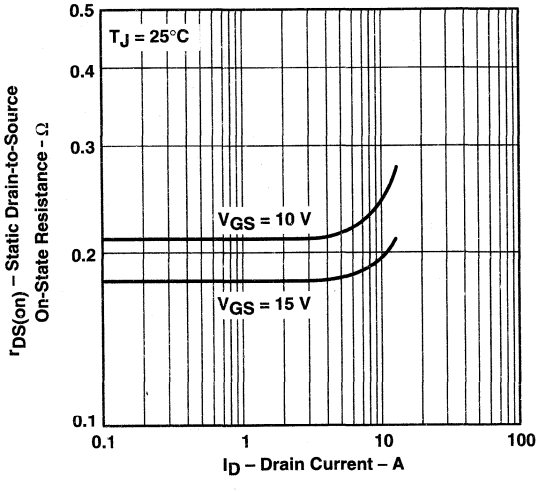


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

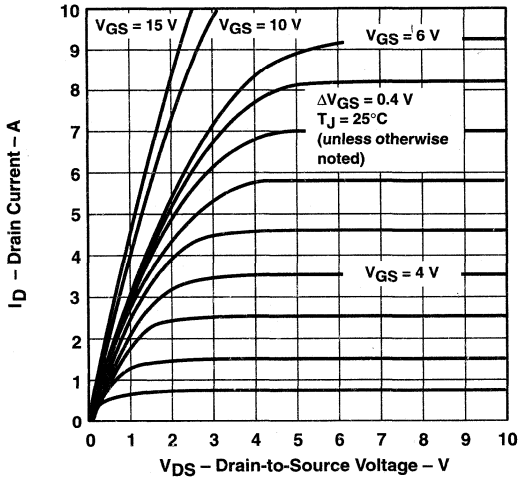


Figure 8

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

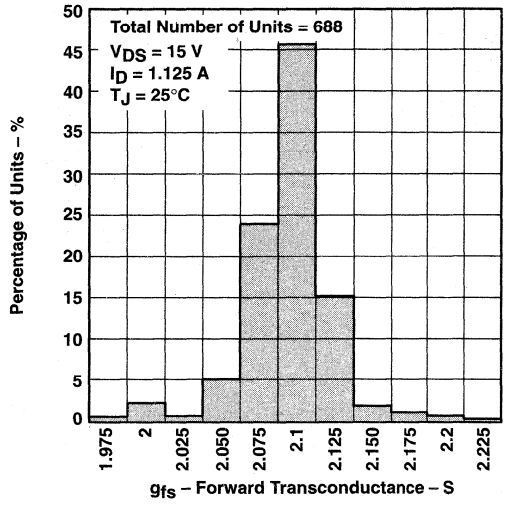


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

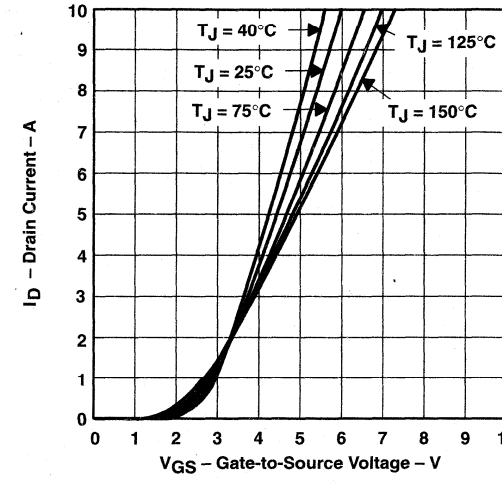


Figure 10

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

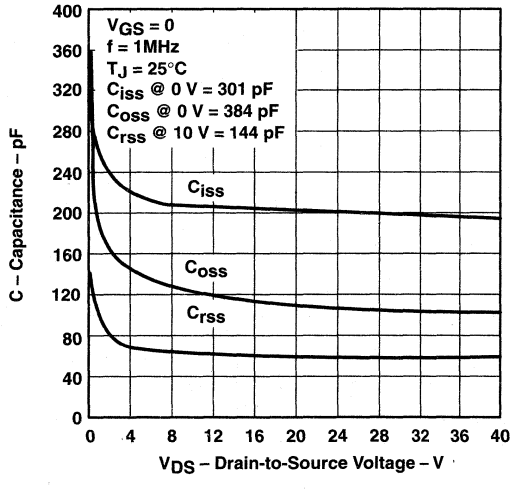


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

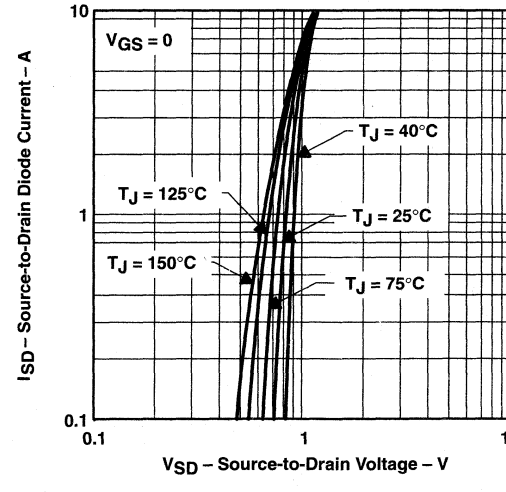


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

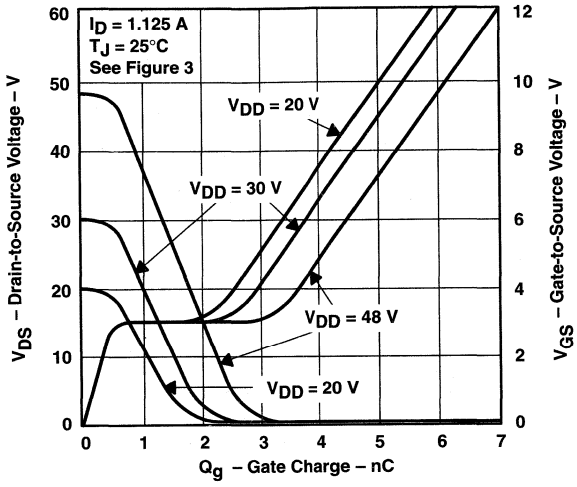


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

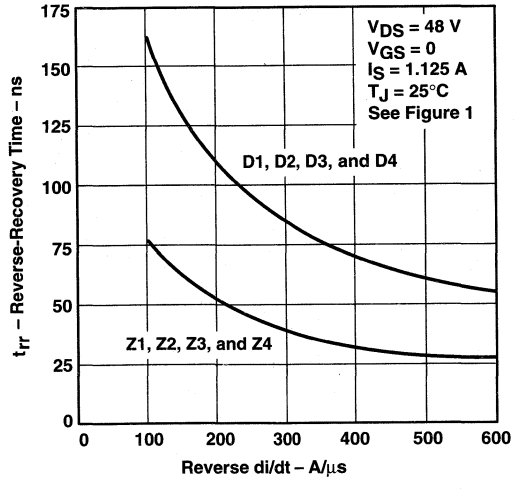
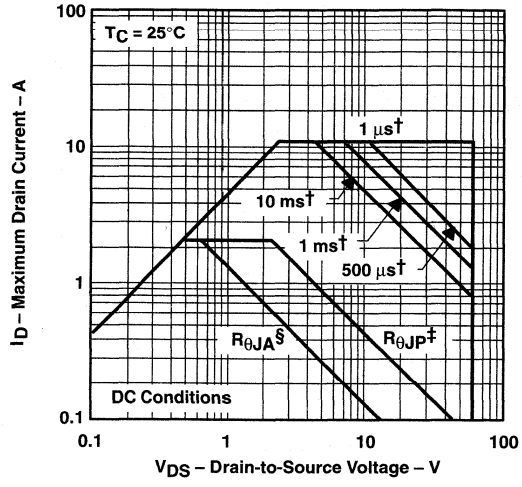


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle
‡ Device mounted in intimate contact with infinite heatsink.
§ Device mounted on FR4 printed circuit board with no heatsink.

Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

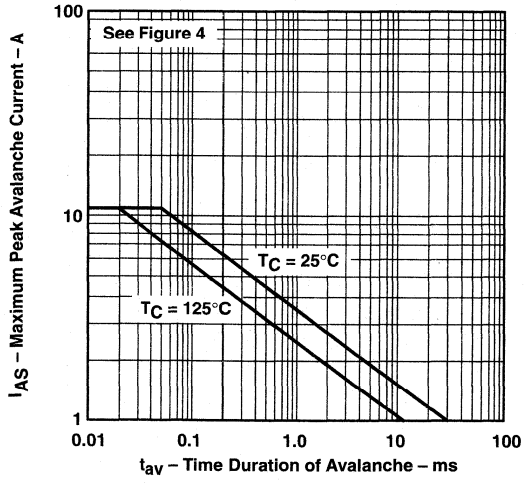
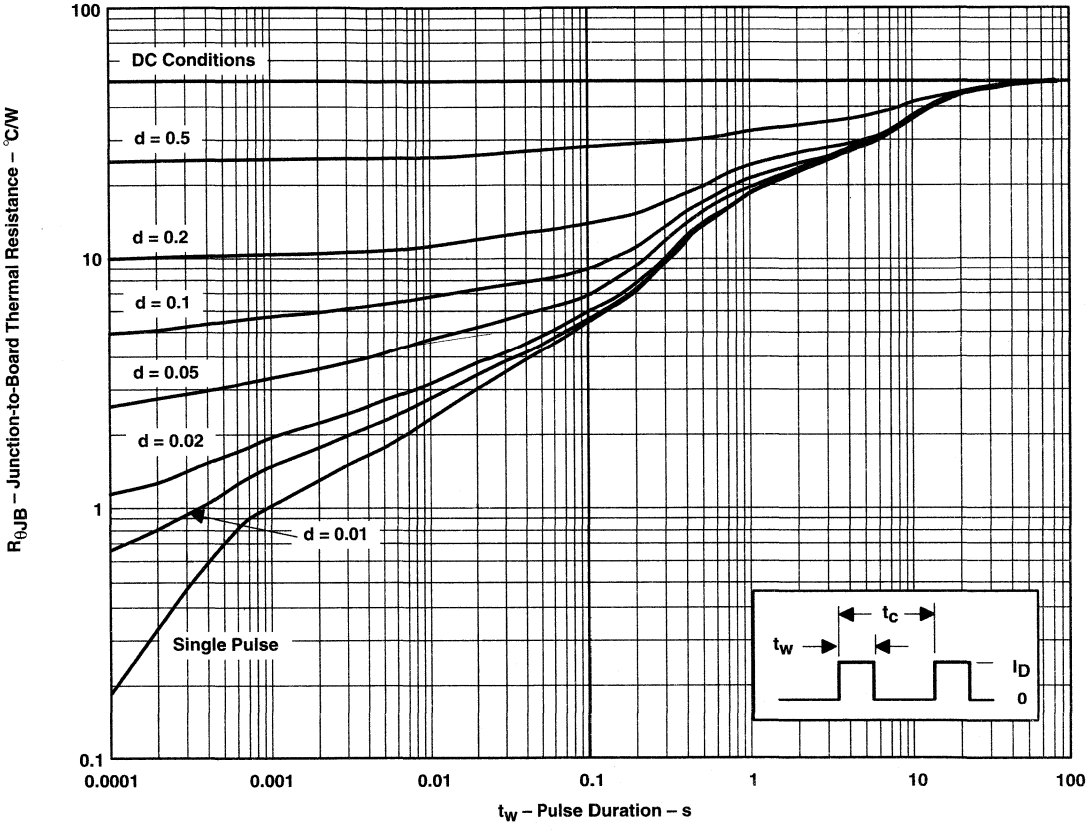


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta JB}(t) = r(t)\ R_{\theta JB}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 17

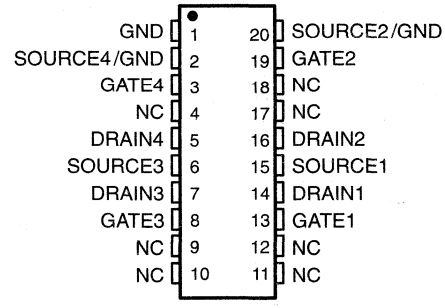
- **Low $r_{DS(on)}$ . . . 0.3 Ω Typ**
- **High-Voltage Output . . . 60 V**
- **Pulsed Current . . . 10 A Per Channel**
- **Fast Commutation Speed**

description

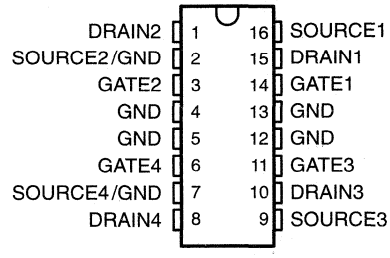
The TPIC5404 is a monolithic power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

The TPIC5404 is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5404 is characterized for operation over the case temperature range of –40°C to 125°C.

DW PACKAGE
(TOP VIEW)

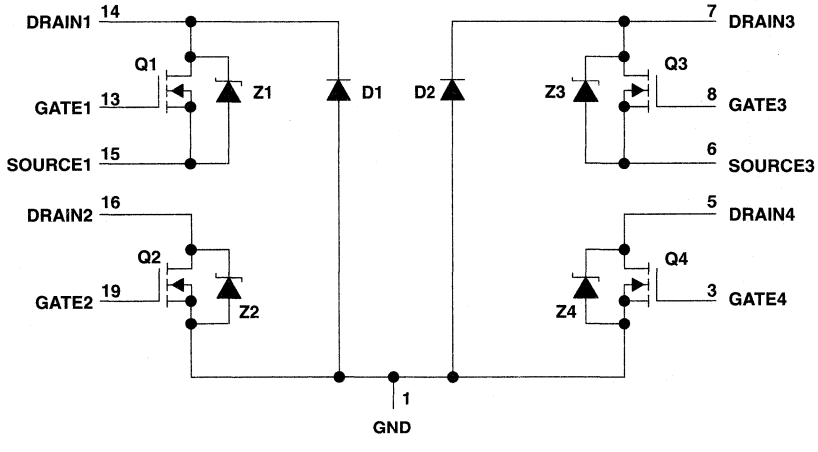


NE PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



NOTE A: Pin numbers shown are for the DW package.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	±20
Continuous drain current, each output, T_C = 25°C: DW package	1.7 A
NE package	2 A
Continuous source-to-drain diode current (NE package)	2 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 15)	10 A
Single-pulse avalanche energy, T_C = 25°C (see Figures 4 and 16)	21 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, V_{GS} = 10 V, See Notes 2 and 3			0.6	0.7	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2 A (D1, D2), See Notes 2 and 3			7.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3			1	1.2	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.41	0.5	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 1 A, See Notes 2 and 3		1.6	1.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz			220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤ 5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z1 and Z3), See Figure 1		120		ns
Q_{RR}	Total diode charge			0.12		µC
$t_{rr(SD)}$	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z2 and Z4), See Figure 1		280		ns
Q_{RR}	Total diode charge			0.9		µC

GND-to-drain diode characteristics, T_C = 25°C (see schematic, D1 and D2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 1 A, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		260		ns
Q_{RR}	Total diode charge			2.2		µC

resistive-load switching characteristics, T_C = 25°C

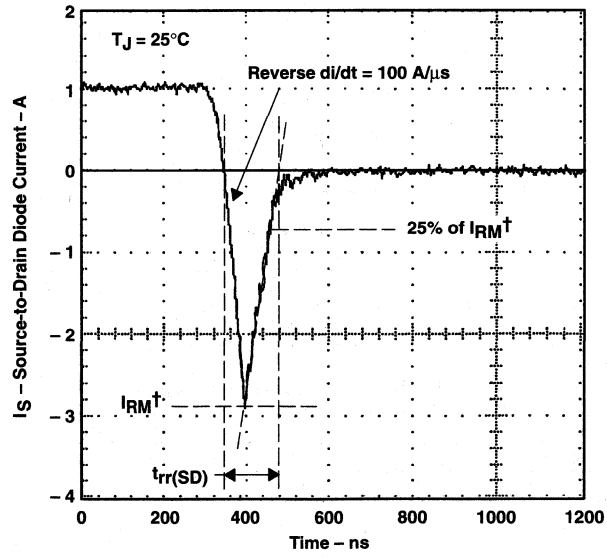
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		32	65	ns
$t_{d(off)}$	Turn-off delay time			40	80	
t_{r2}	Rise time			15	30	
t_{f2}	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.8	1	
Q_{gd}	Gate-to-drain charge			2.6	3.2	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package	All outputs with equal power, See Note 4		90		°C/W
		NE package			60		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package			30		°C/W
		NE package			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

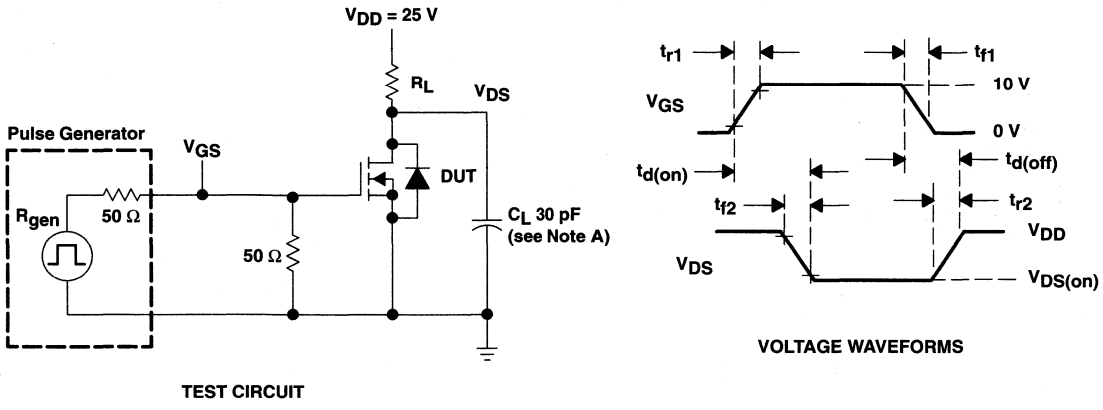
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

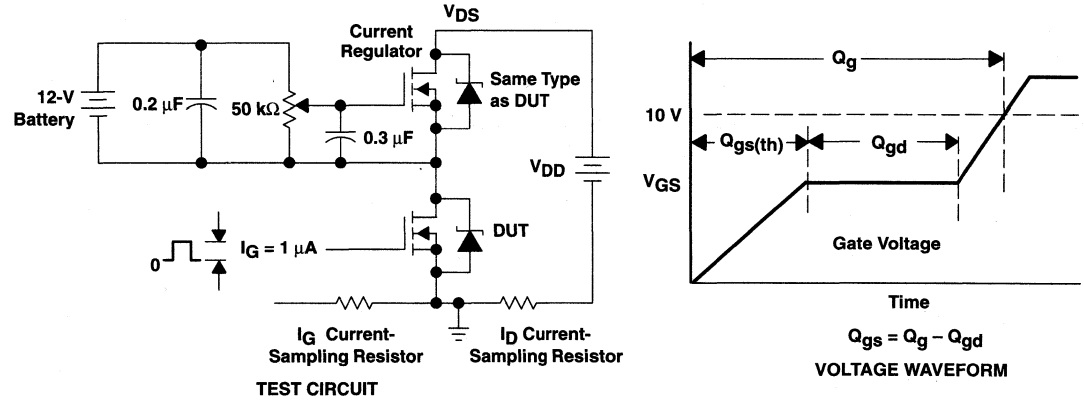
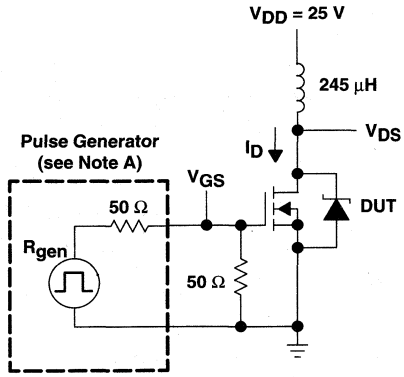
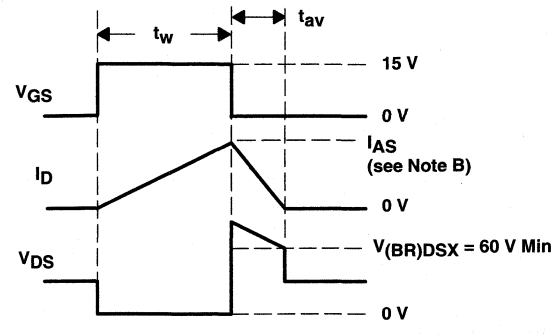


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current I_{AS} = 10 A, where t_{av} = avalanche time.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21$ mJ

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

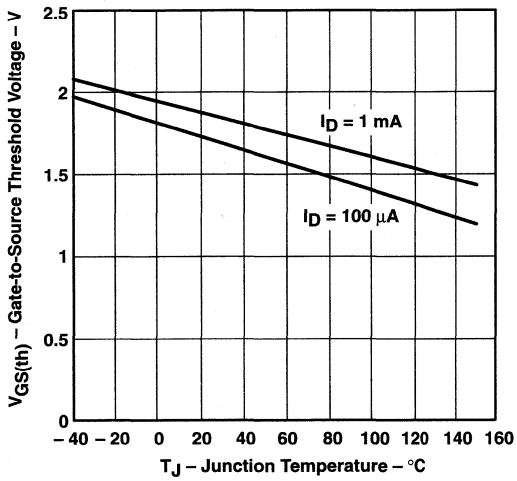


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

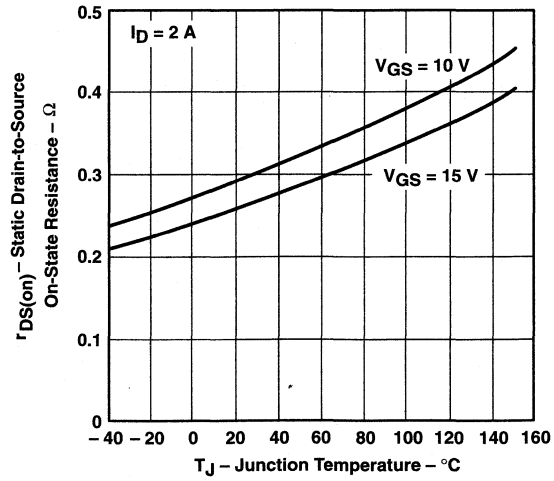


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

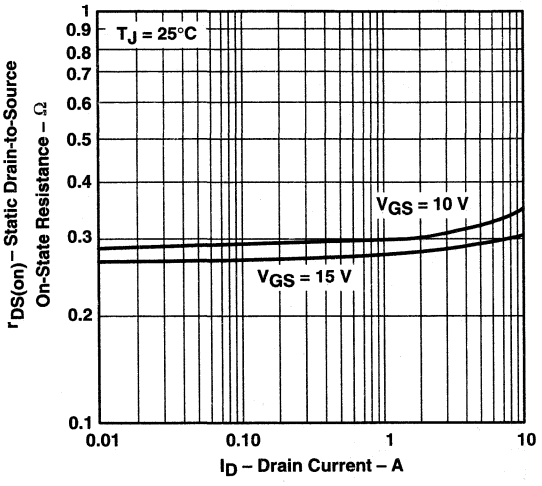


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

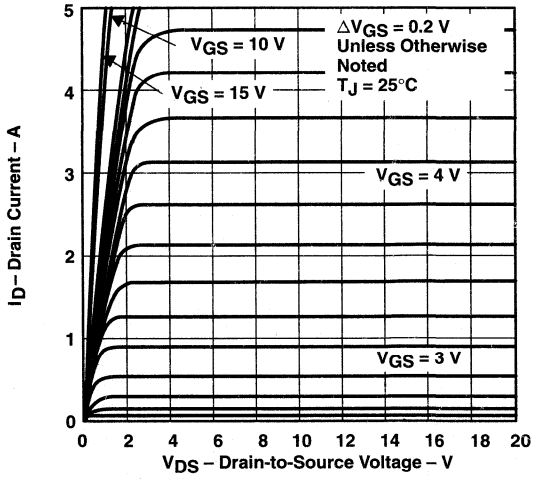


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

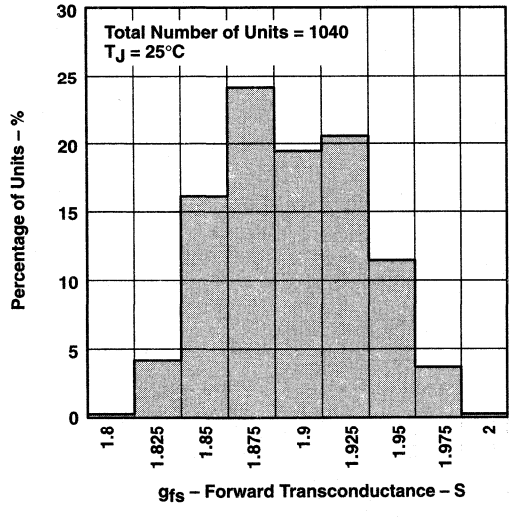


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

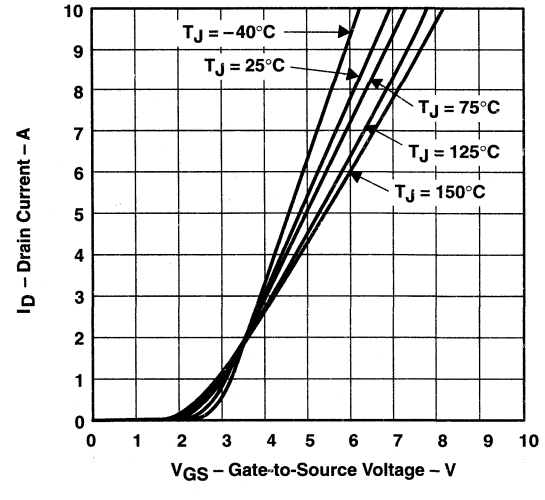


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

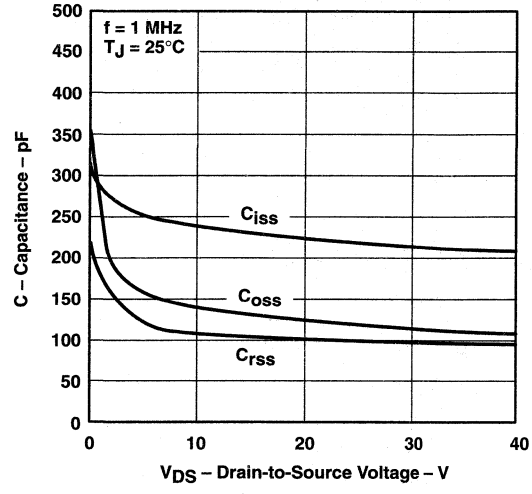


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

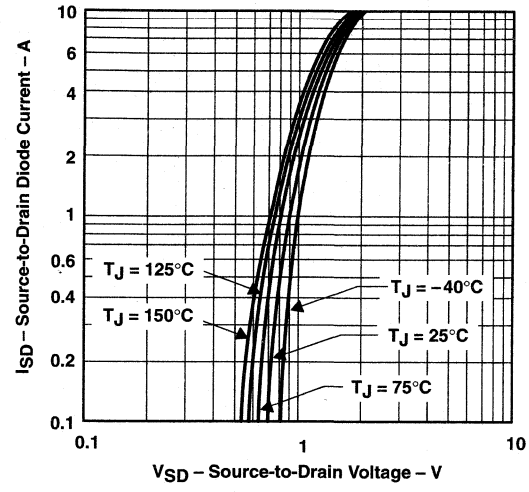


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

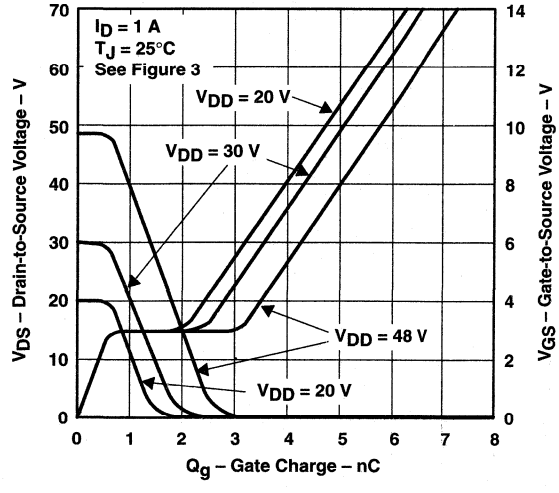


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

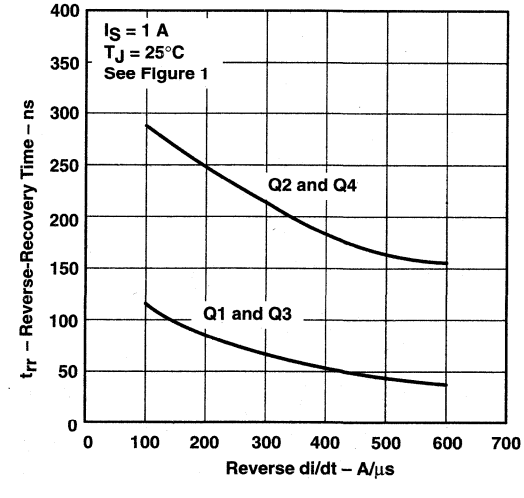
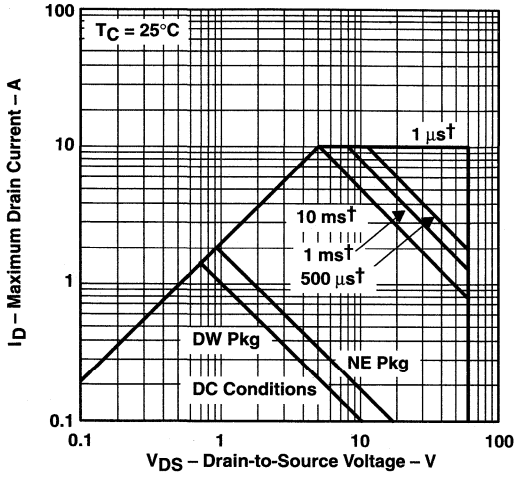


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

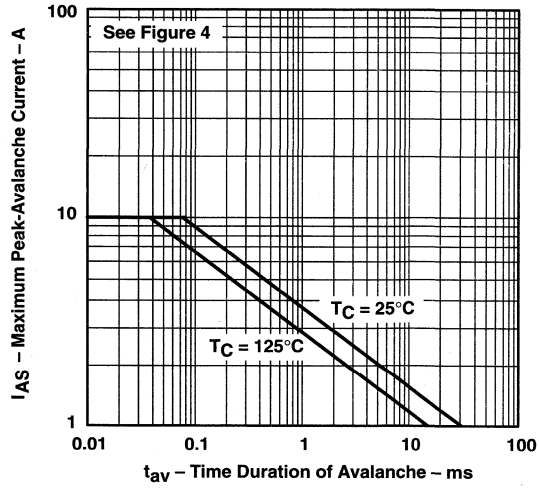
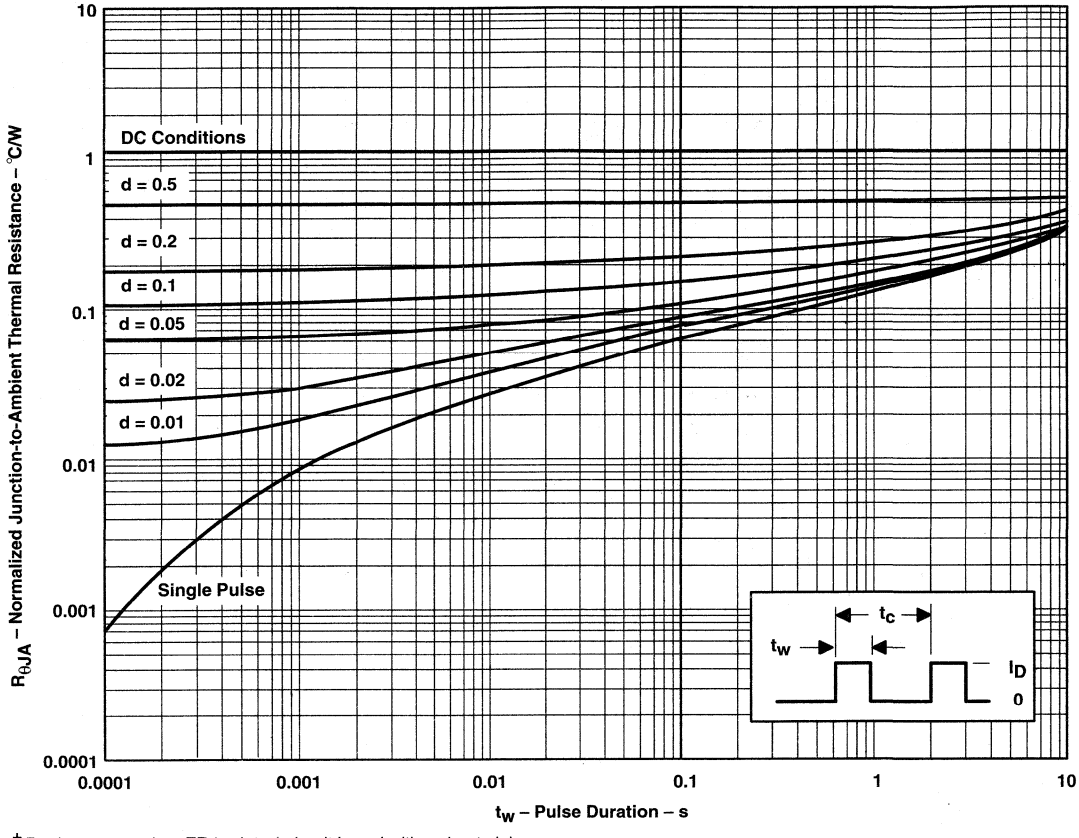


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



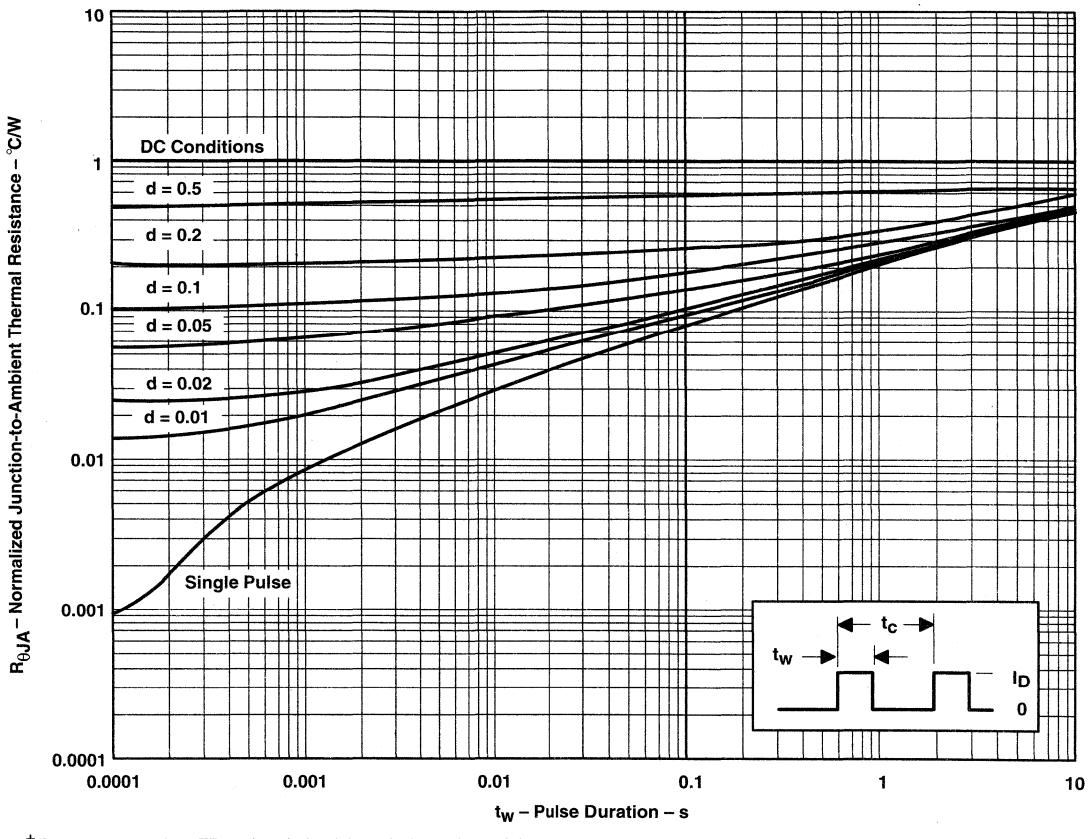
† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 17

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



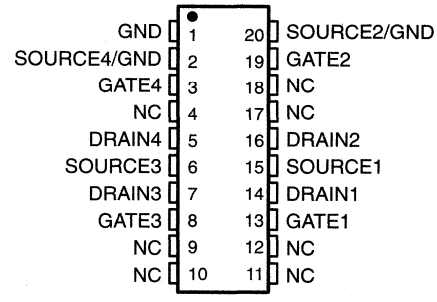
† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

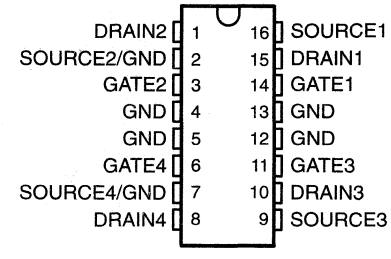
Figure 18

- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)



NE PACKAGE
(TOP VIEW)



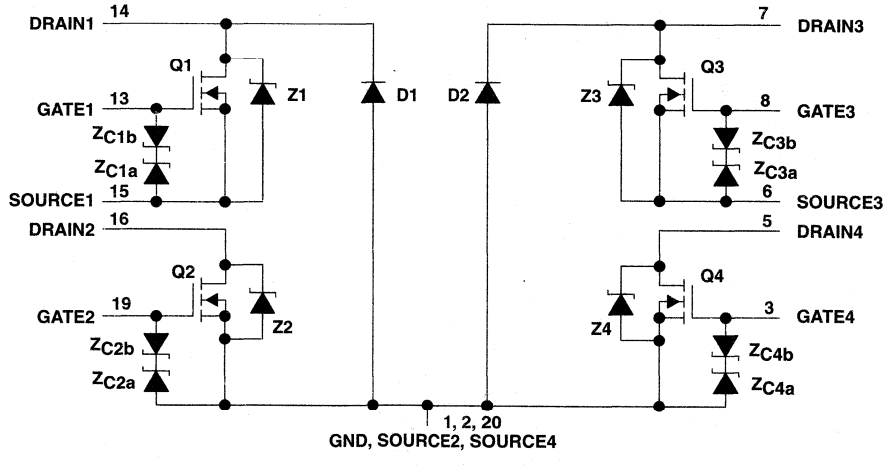
NC – No internal connection

description

The TPIC5421L is a monolithic gate-protected logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5421L is offered in a 20-pin wide-body surface-mount (DW) package and a 16-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.
Pin numbers shown are for the DW package.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C: NE package	1.5 A
DW package	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	180 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.4	0.475	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.475	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		1.25	1.4		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0, See Figure 11			220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, See Figures 1 and 14 V_{DS} = 48 V, di/dt = 100 A/µs,	Z1 and Z3		55		ns
			Z2 and Z4		150		
			D1 and D2		200		
Q_{RR}	Total diode charge		Z1 and Z3		0.06		µC
			Z2 and Z4		0.3		
			D1 and D2		0.7		

resistive-load switching characteristics, T_C = 25°C

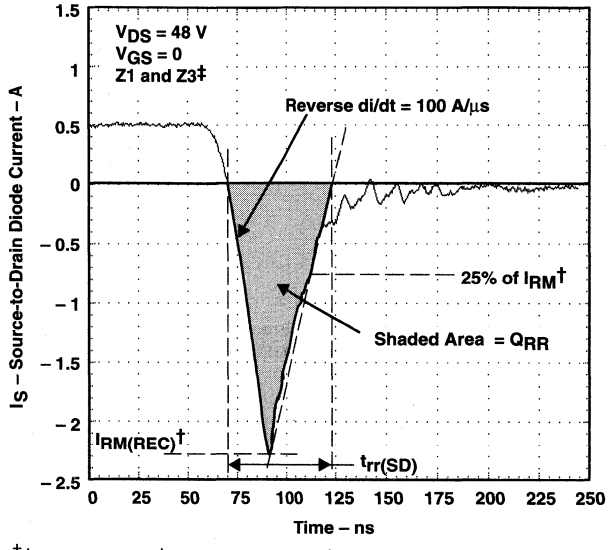
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_{r2}	Rise time			21	42	
t_{f2}	Fall time			9	18	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 5 V, See Figure 3		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.55	0.8	
Q_{gd}	Gate-to-drain charge			2.5	3.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package	See Notes 4 and 6		90		°C/W
		NE package			60		
$R_{\theta JB}$	Junction-to-board thermal resistance	DW package	See Notes 4 and 6		53		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package	See Notes 5 and 6		30		
		NE package			25		

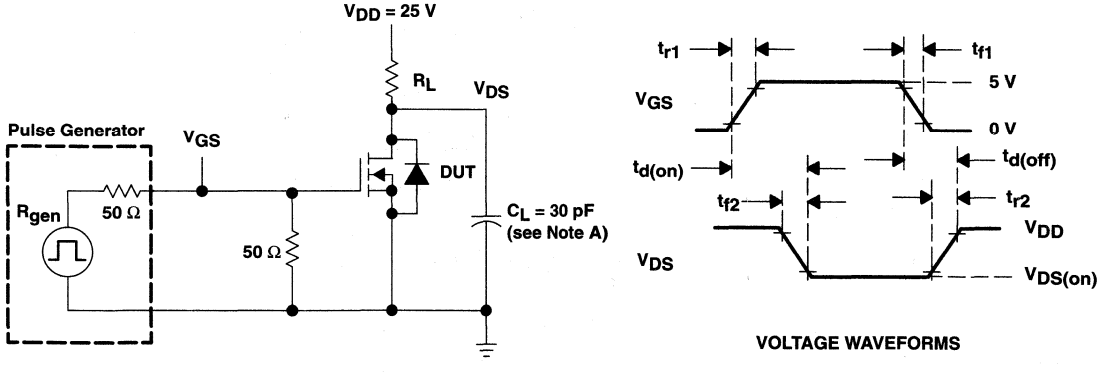
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted in intimate contact with infinite heatsink.
6. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† $I_{RM(REC)}$ = maximum recovery current
‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveforms of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

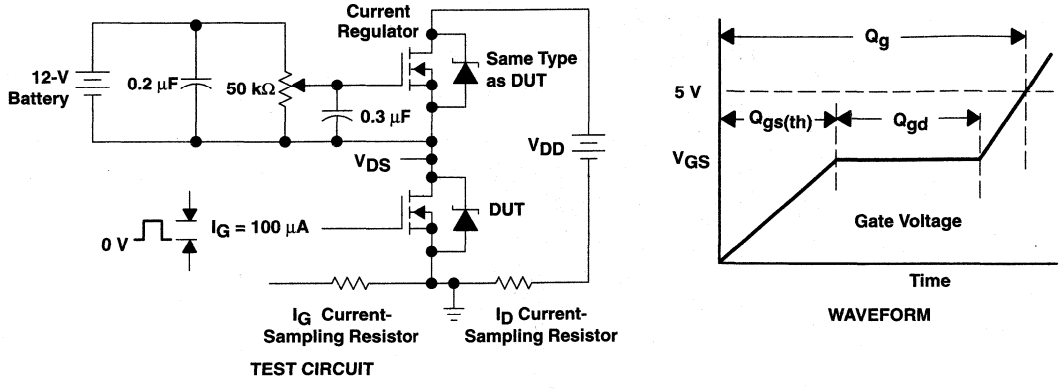
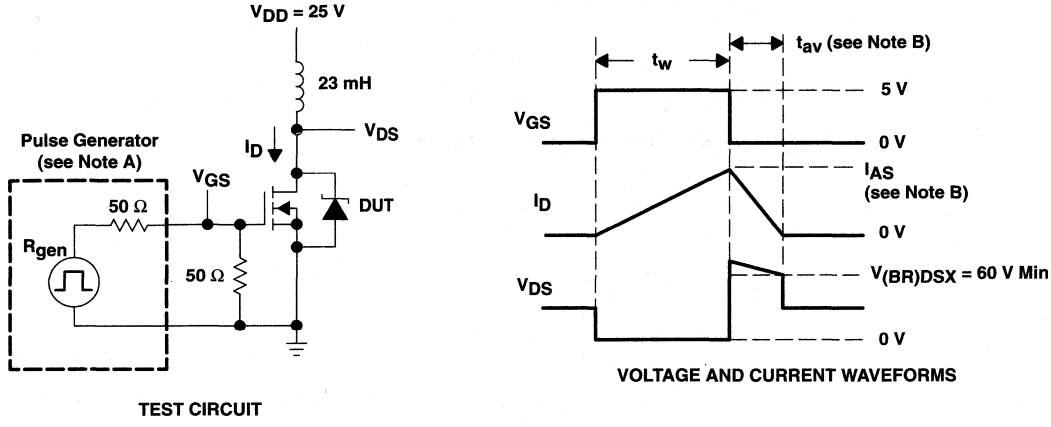


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180$ mJ,
where t_{av} = avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

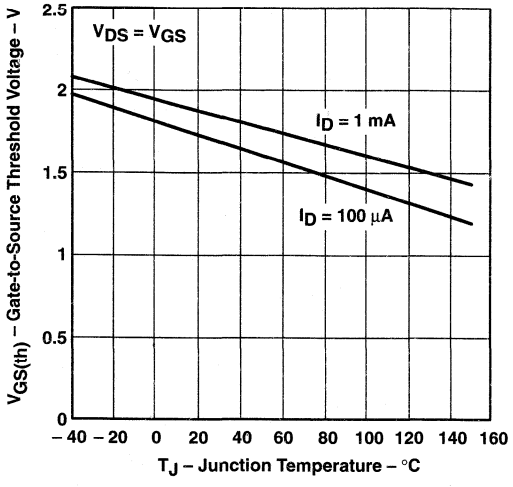


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

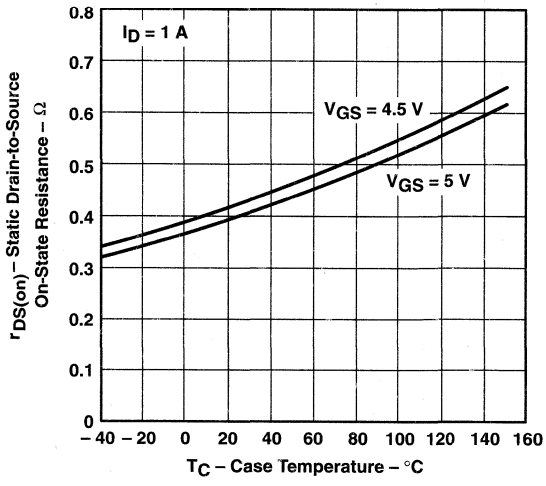


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

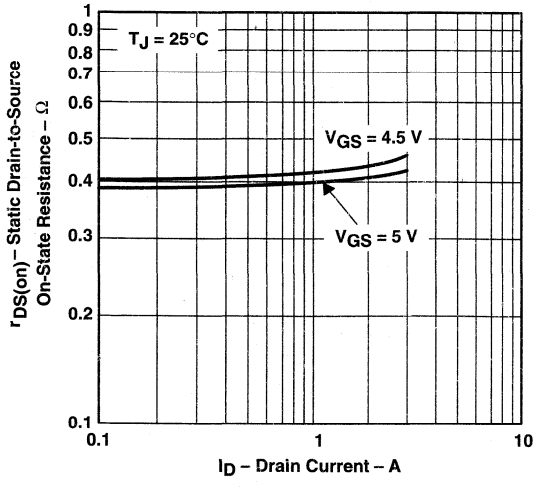


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

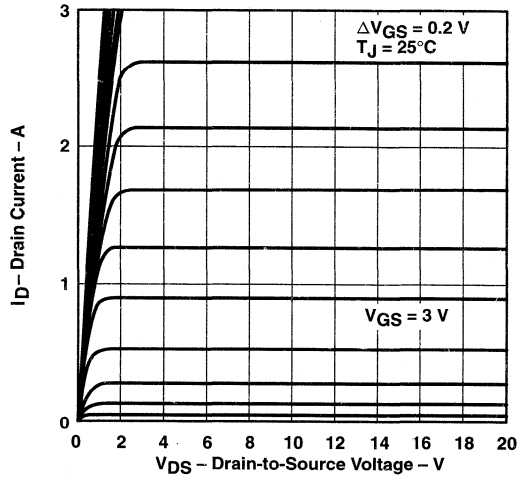


Figure 8

TYPICAL CHARACTERISTICS

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

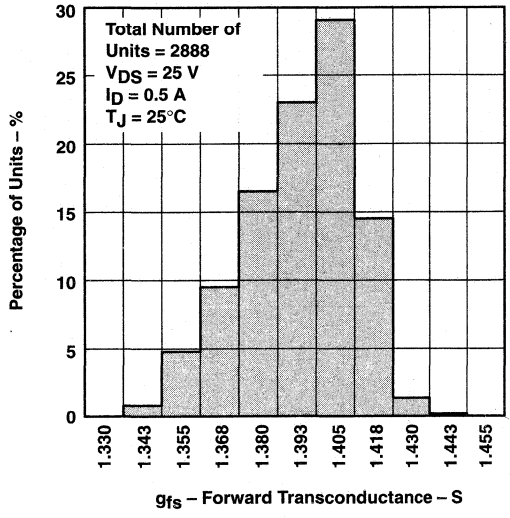


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

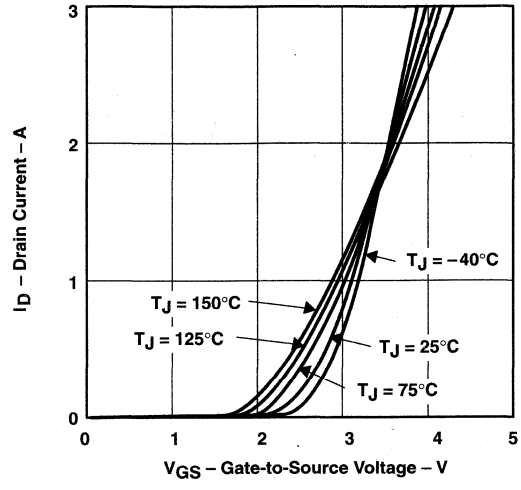


Figure 10

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

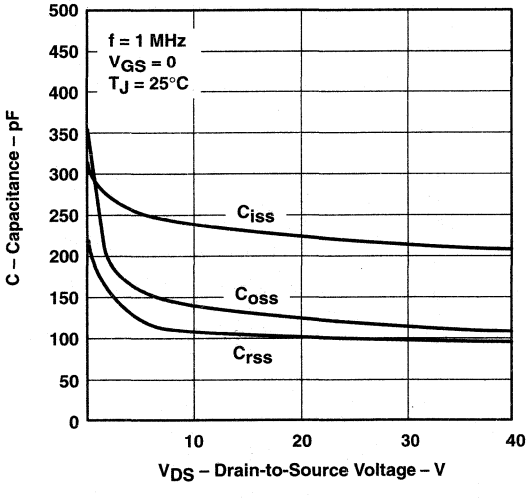


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

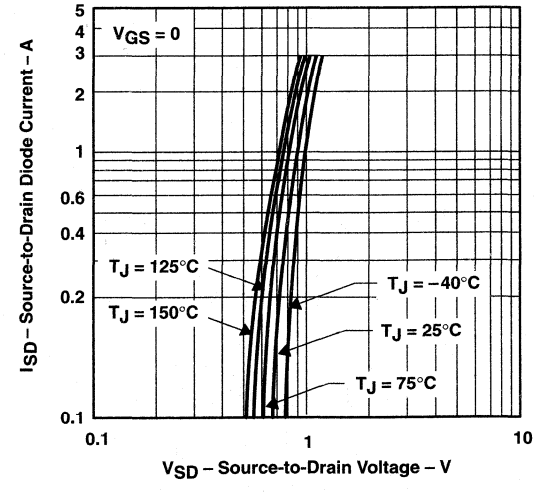


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

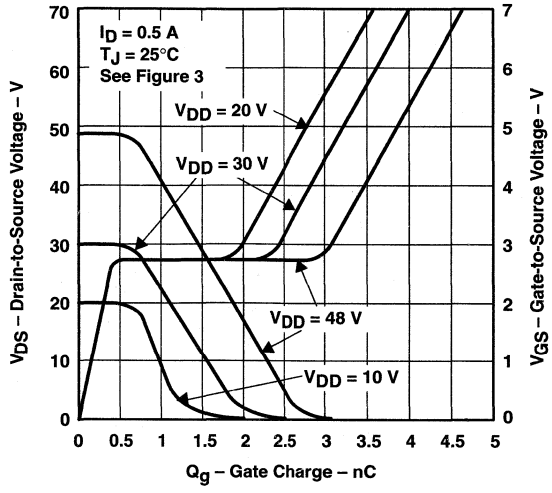


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

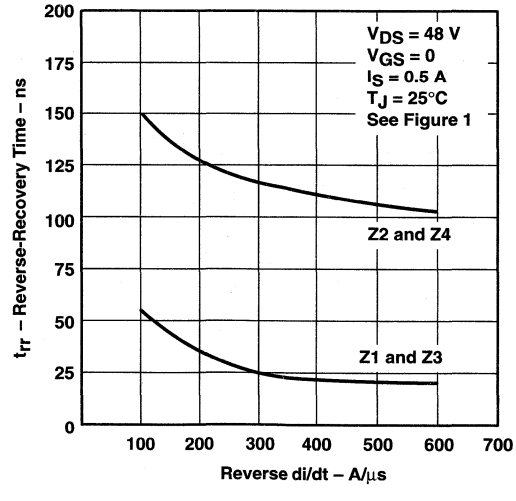
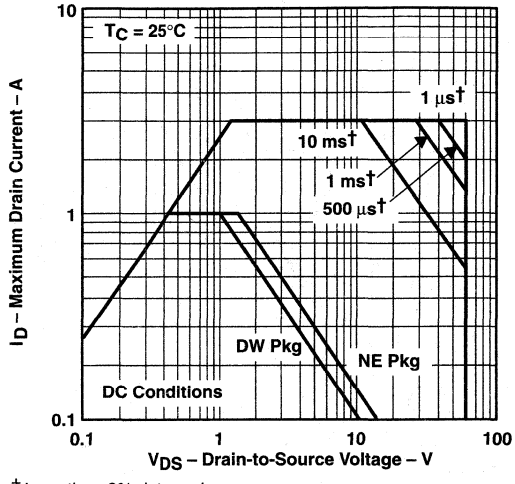


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle

Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

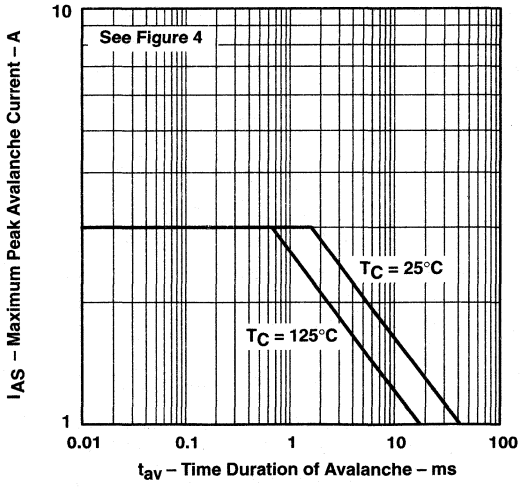
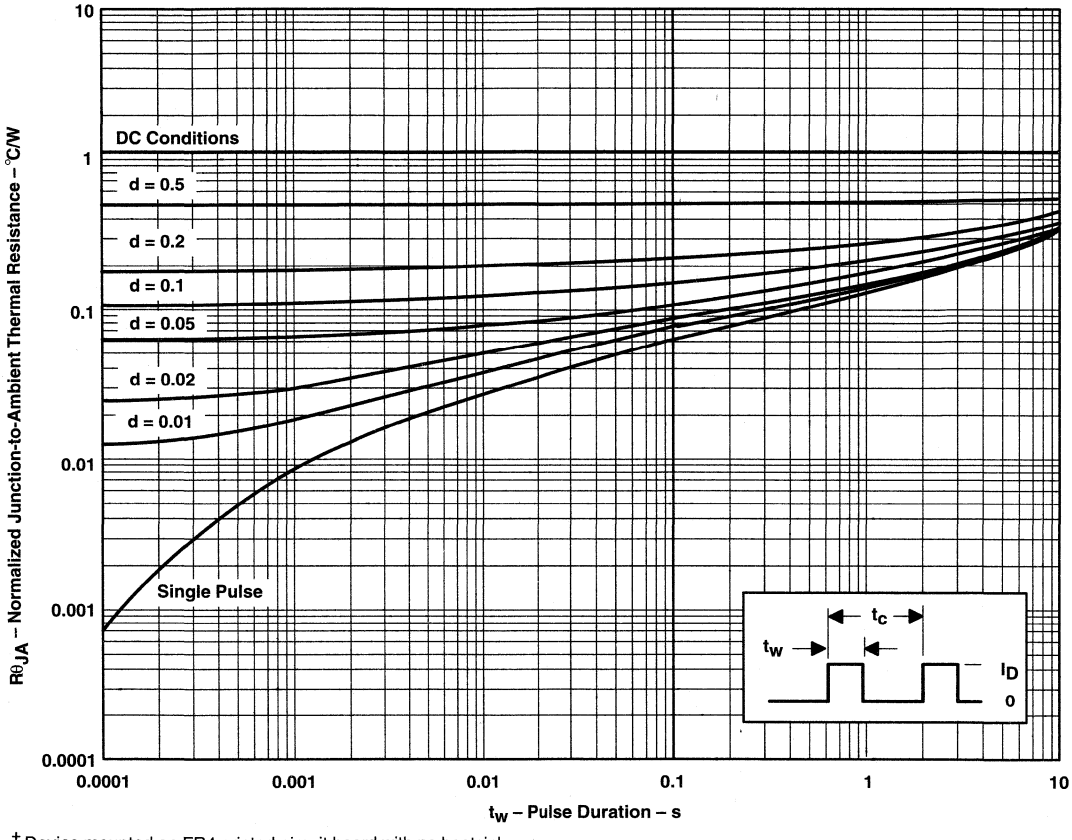


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



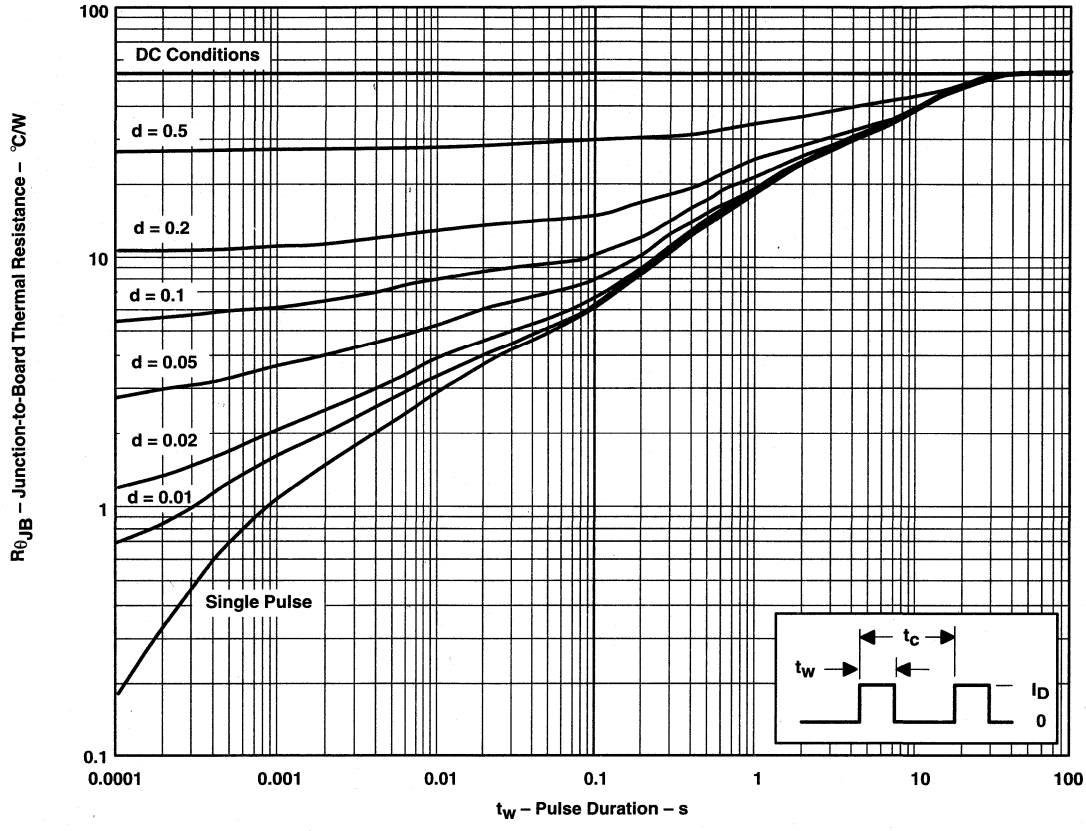
† Device mounted on FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JA}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



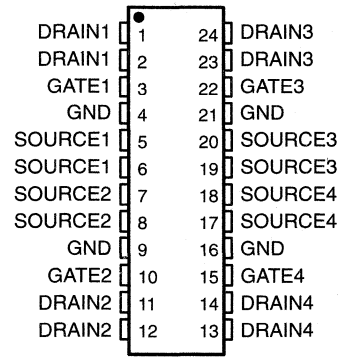
† Device mounted on a 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JB}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 18

- **Low $r_{DS(on)}$ . . . 0.32 Ω Typ**
- **Voltage Output . . . 60 V**
- **Input Protection Circuitry . . . 18 V**
- **Pulsed Current . . . 4 A Per Channel**
- **Extended ESD Capability . . . 4000 V**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)

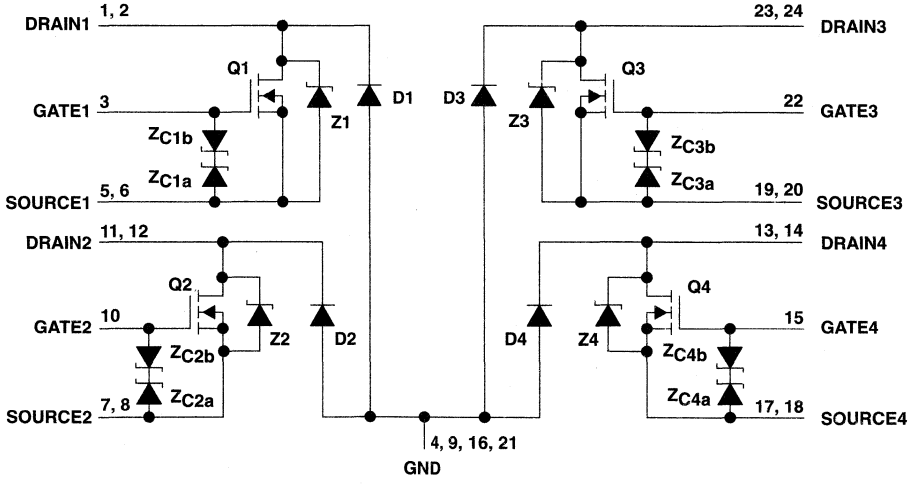


description

The TPIC5423L is a monolithic gate-protected logic-level power DMOS array that consists of four electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5423L is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature of –40°C to 125°C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1.25 A
Continuous source-to-drain diode current, T_C = 25°C	1.25 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	4 A
Continuous gate-to-source zener-diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4 and 16)	96 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	1.39 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.25 A, See Notes 2 and 3	V_{GS} = 5 V,		0.4	0.47	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.25 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.25 A (D1, D2, D3, D4), See Notes 2 and 3			2		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V,	V_{DS} = 0		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1.25 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.32	0.375	Ω
			T_C = 125°C		0.44	0.55	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 0.625 A,	1.25	1.63		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		200	250	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				60	75	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.625 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs, Z1, Z2, Z3, and Z4		80		ns
			D1, D2, D3, and D4		130		
Q_{RR}	Total diode charge		Z1, Z2, Z3, and Z4		0.8		µC
			D1, D2, D3, and D4		0.66		

resistive-load switching characteristics, T_C = 25°C

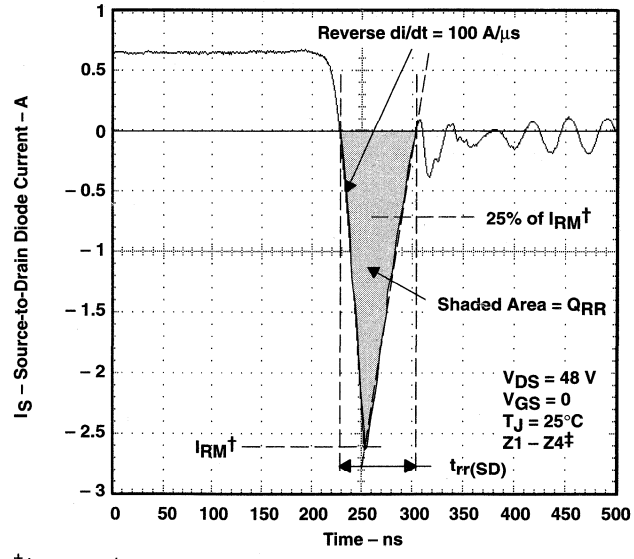
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 40 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		34	70	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_r	Rise time			28	55	
t_f	Fall time			15	30	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.625 A, V_{GS} = 5 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			2.6	3.2	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		49		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		28		

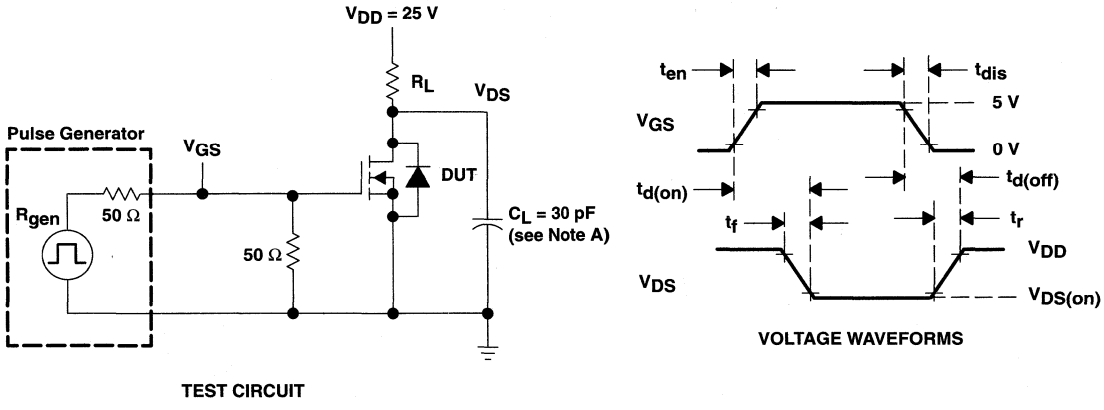
NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
6. Package mounted in intimate contact with infinite heatsink.
7. All outputs with equal power.

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1, D2, D3, and D4 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

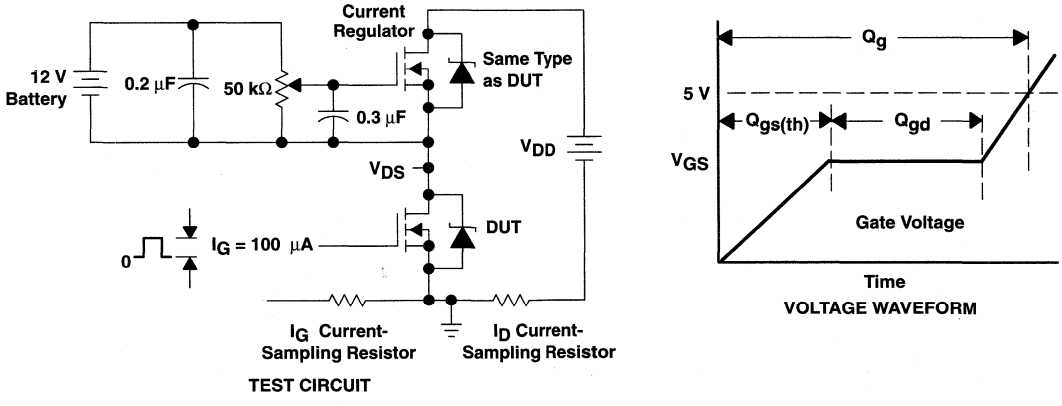
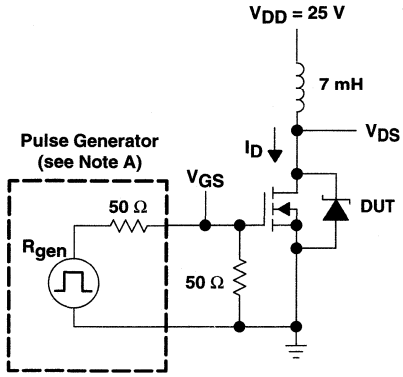
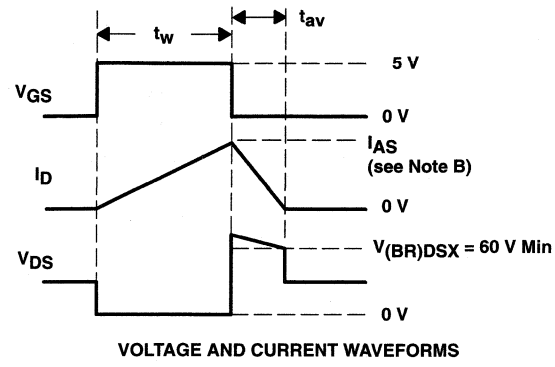


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 4$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 96$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

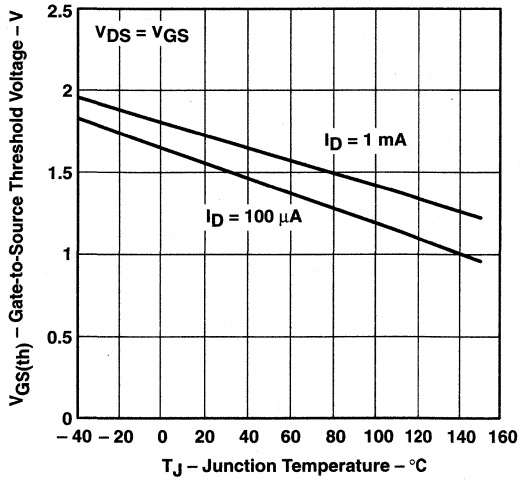


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

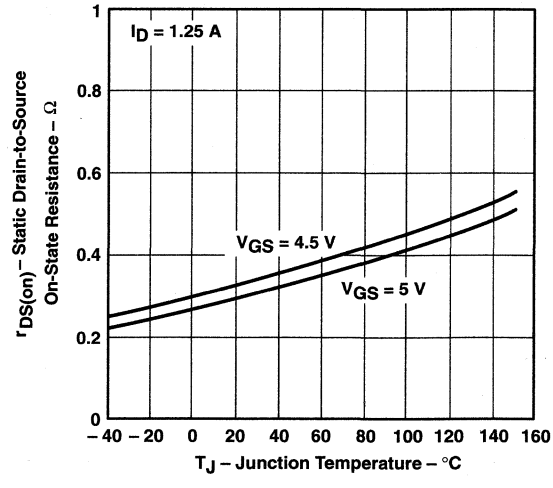


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

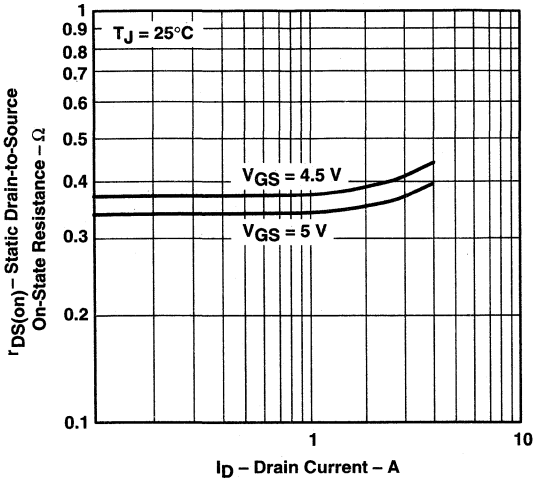


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

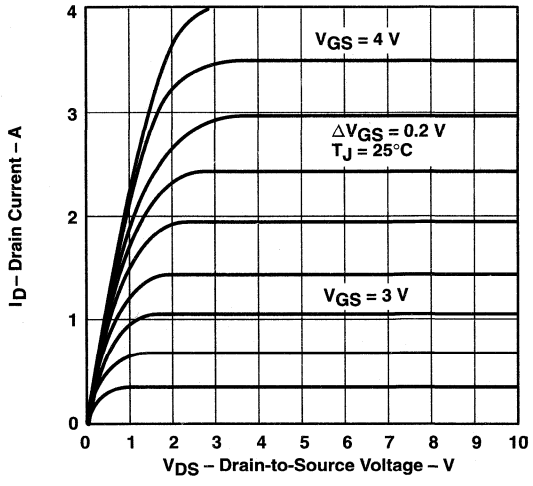


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

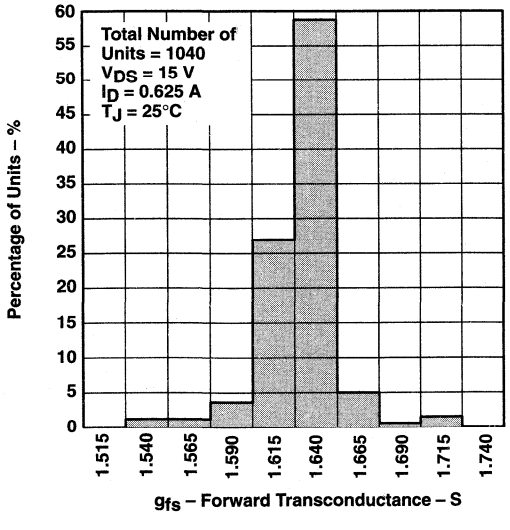


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

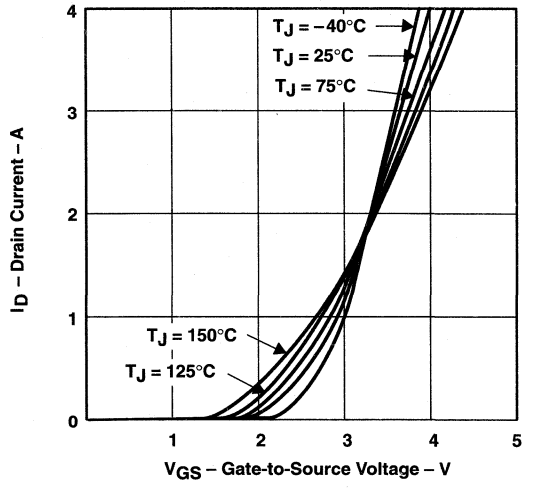


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

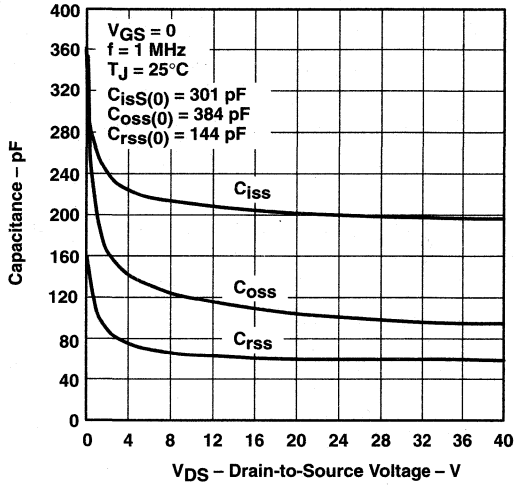


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

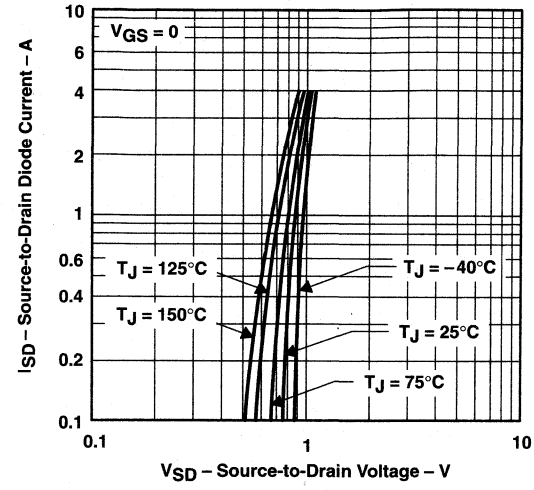


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

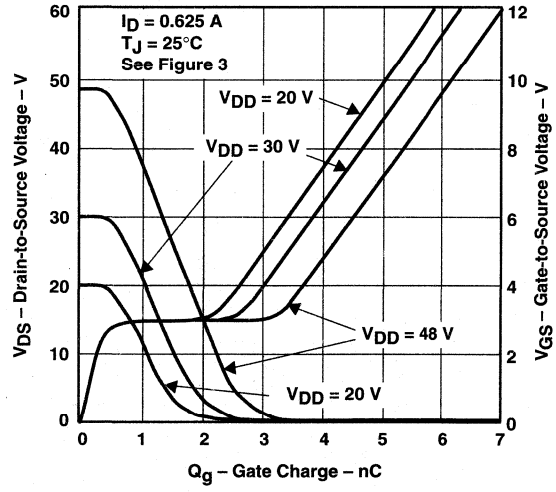


Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

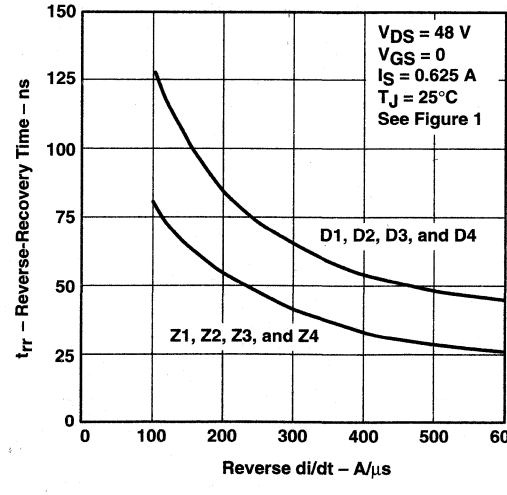
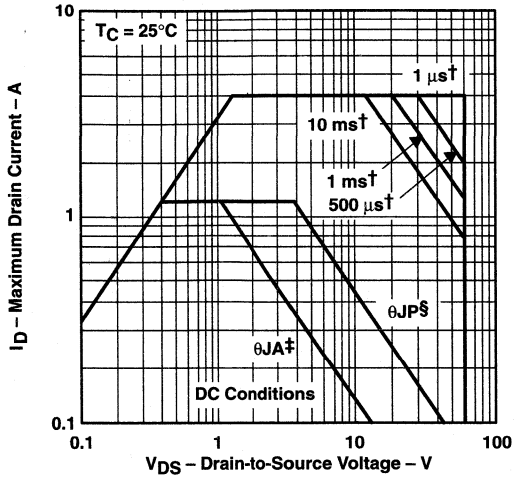


Figure 14

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle
‡ Device mounted on FR4 printed-circuit board with no heatsink.
§ Device mounted in intimate contact with infinite heatsink.

Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

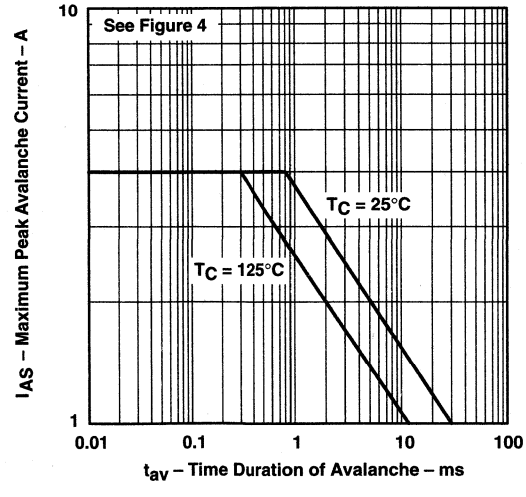
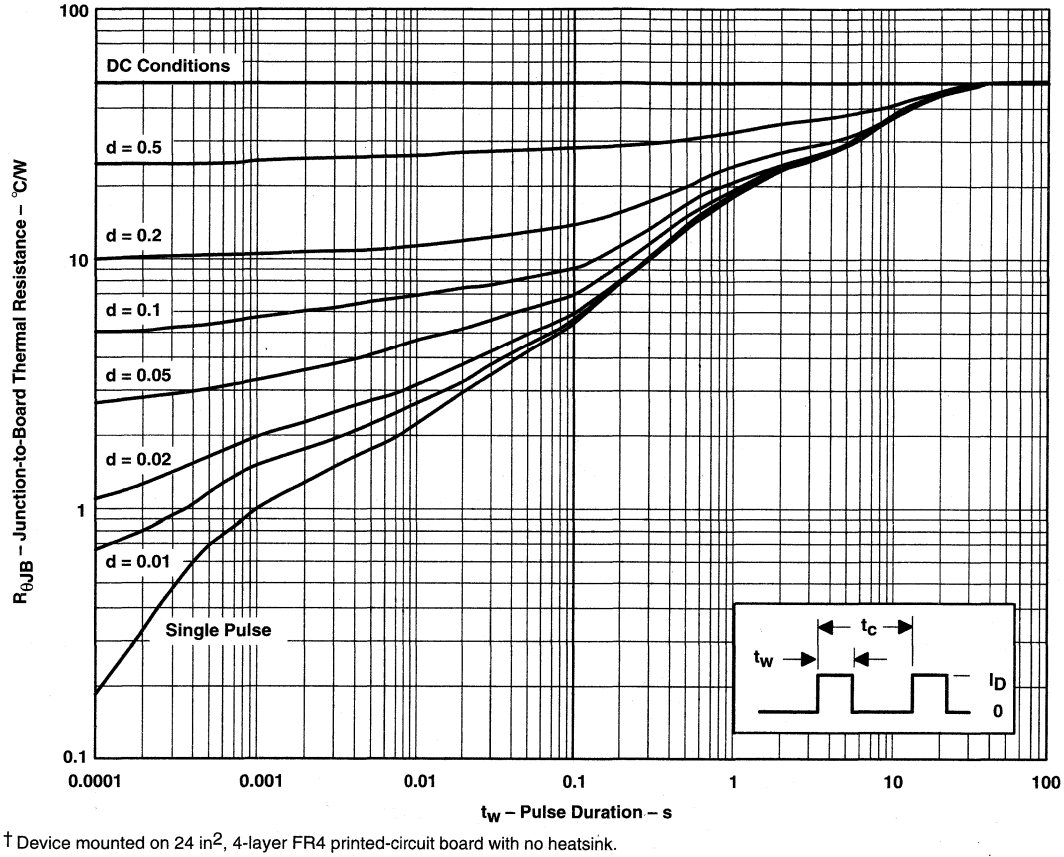


Figure 16

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in^2, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W / t_c

Figure 17

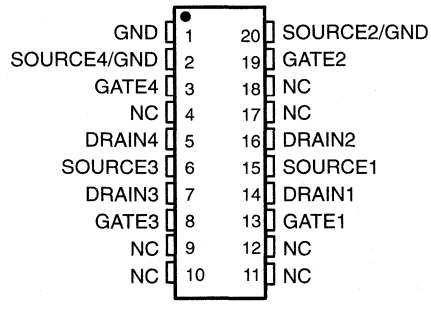
- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Output . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

description

The TPIC5424L is a monolithic logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

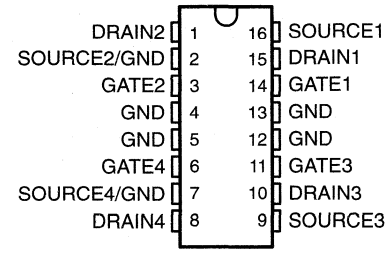
The TPIC5424L is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5424L is characterized for operation over the case temperature range of –40°C to 125°C.

DW PACKAGE
(TOP VIEW)

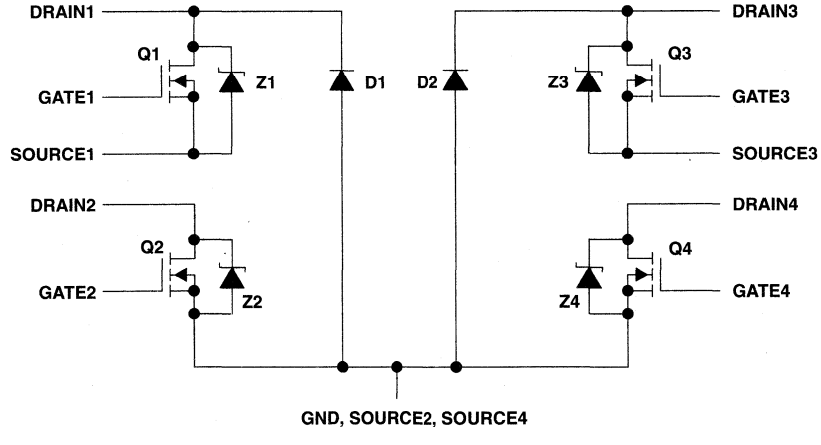


NC – No internal connection

NE PACKAGE
(TOP VIEW)



schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	180 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	V_{DS} = V_{GS},	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, See Notes 2 and 3	V_{GS} = 5 V,		0.4	0.48	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 5 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V (D1, D2)	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.48	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 0.5 A,	1.25	1.39		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S =0.5 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1 and Z3		55		ns
				Z2 and Z4		150		
				D1 and D2		200		
Q_{RR}	Total diode charge			Z1 and Z3		0.06		µC
				Z2 and Z4		0.3		
				D1 and D2		0.7		

resistive-load switching characteristics, T_C = 25°C

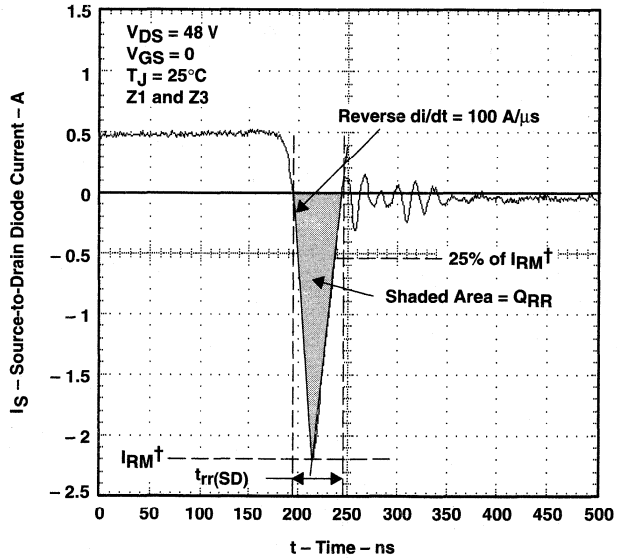
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		34	68	ns
$t_{d(off)}$	Turn-off delay time			40	82	
t_r	Rise time			21	42	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.55	0.8	
Q_{gd}	Gate-to-drain charge			2.5	3.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	DW package	All outputs with equal power		90		°C/W
		NE package			60		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package			30		°C/W
		NE package			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION

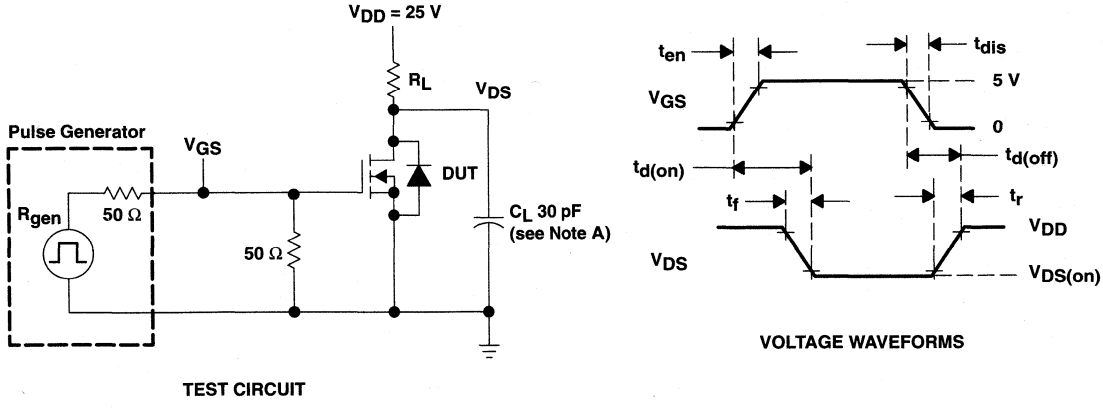


† I_{RM} = maximum recovery current

NOTE A. The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

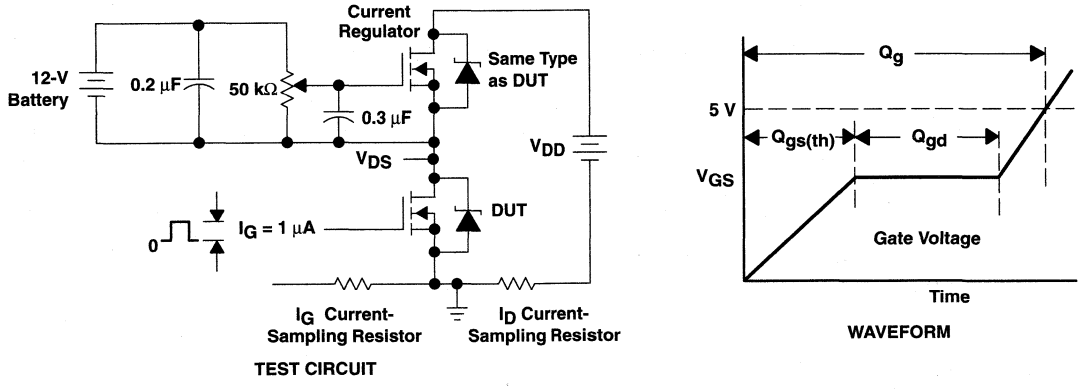
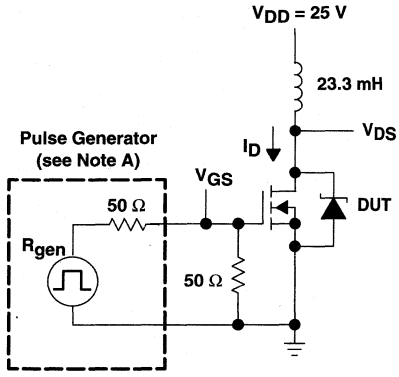
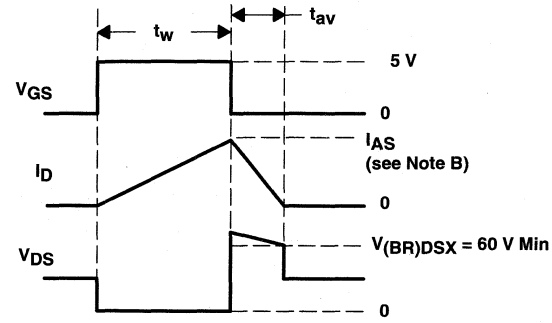


Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current I_{AS} = 3 A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

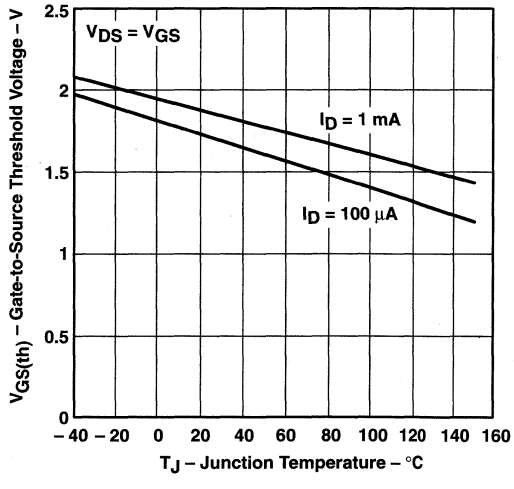


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

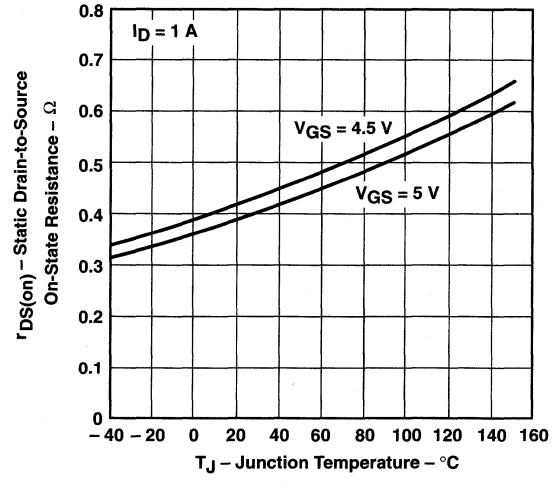


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

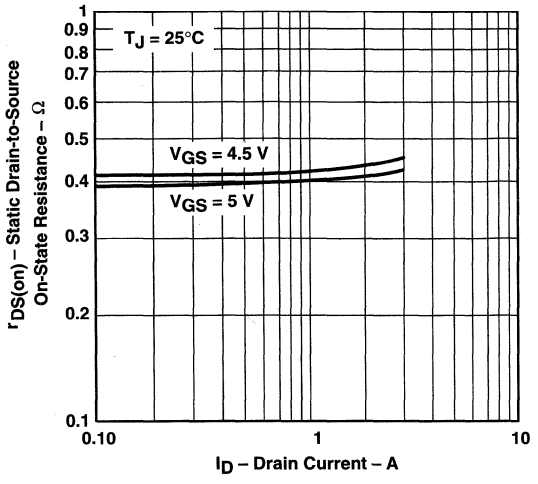


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

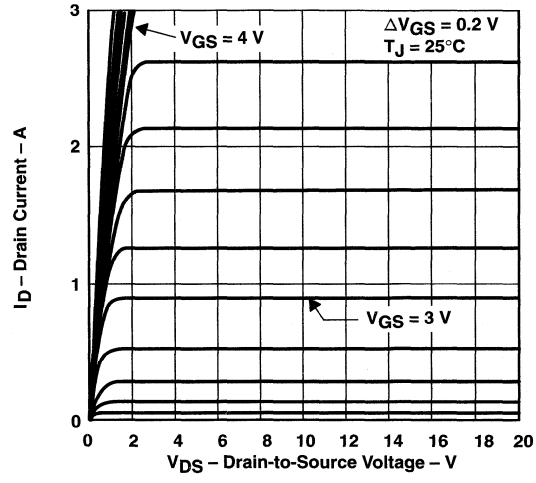


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

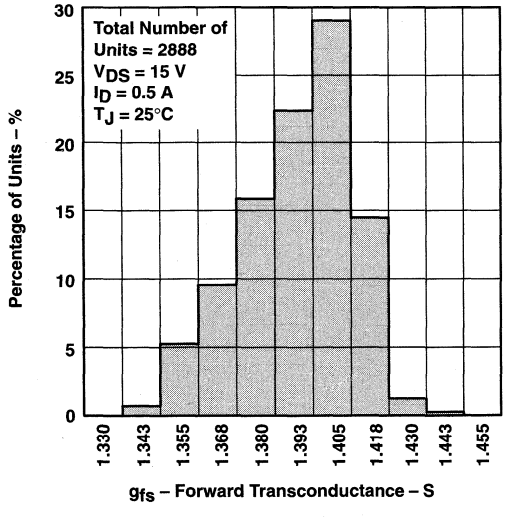


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

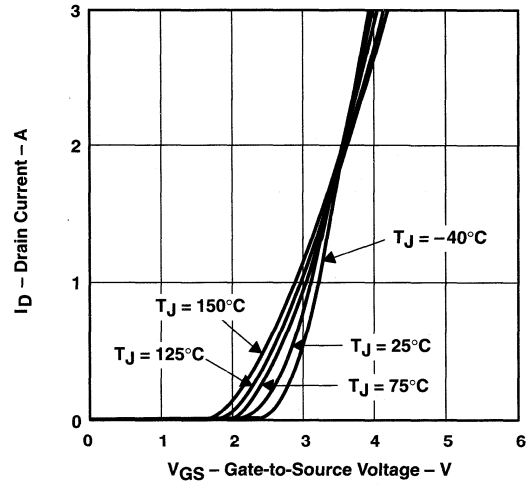


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

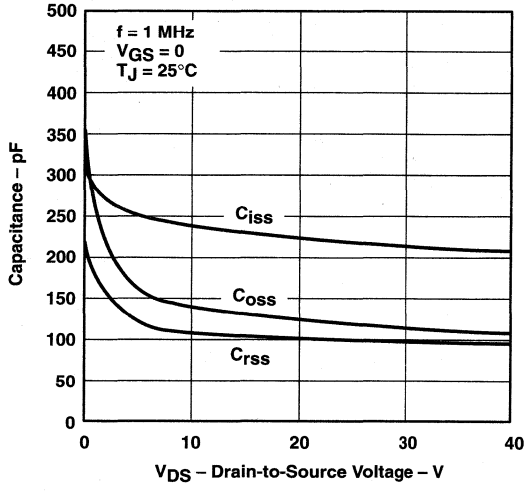


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

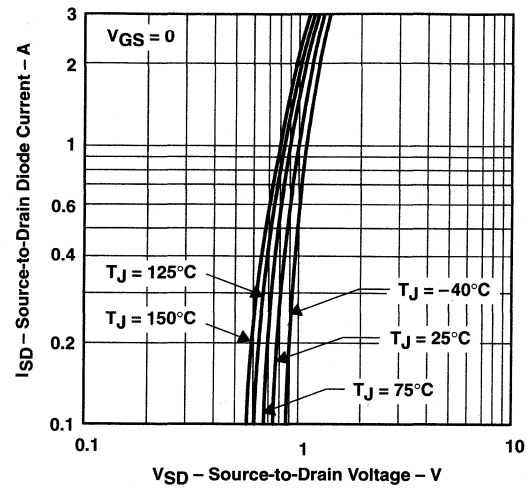


Figure 12

GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

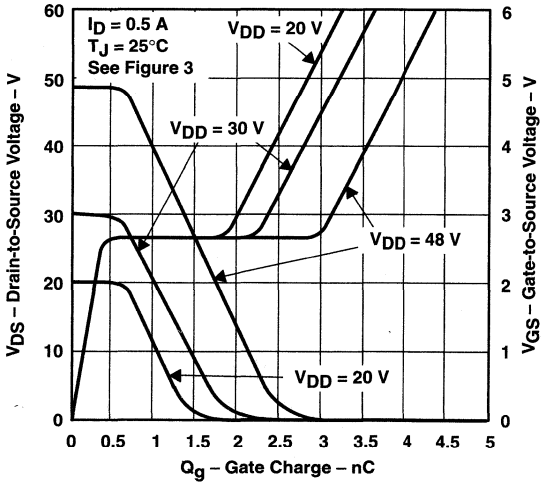


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

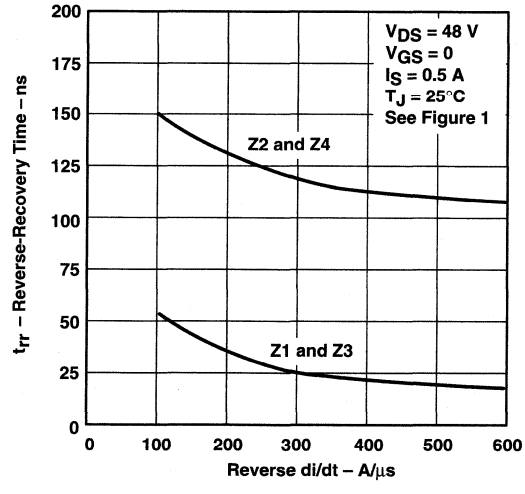
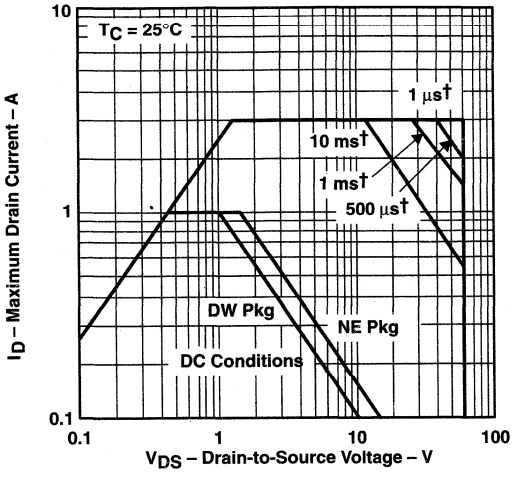


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

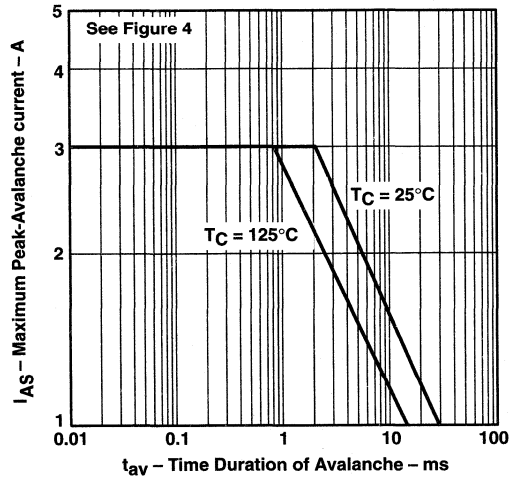
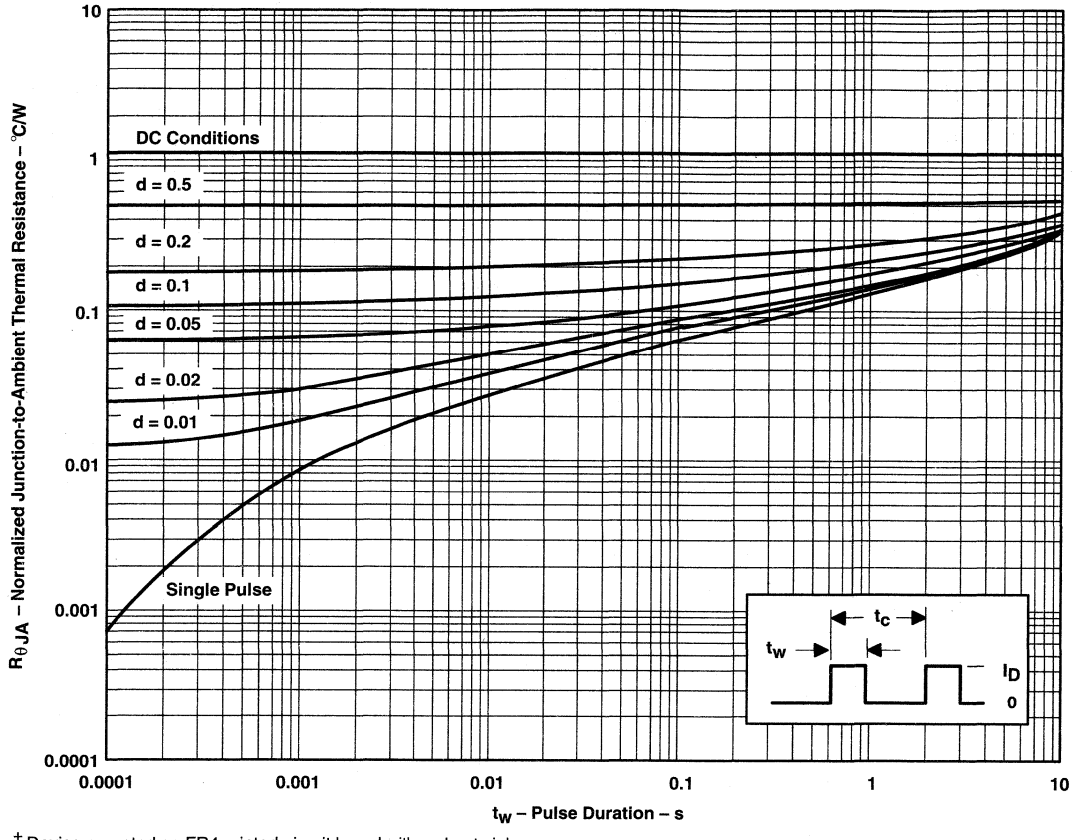


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

TEXAS INSTRUMENTS
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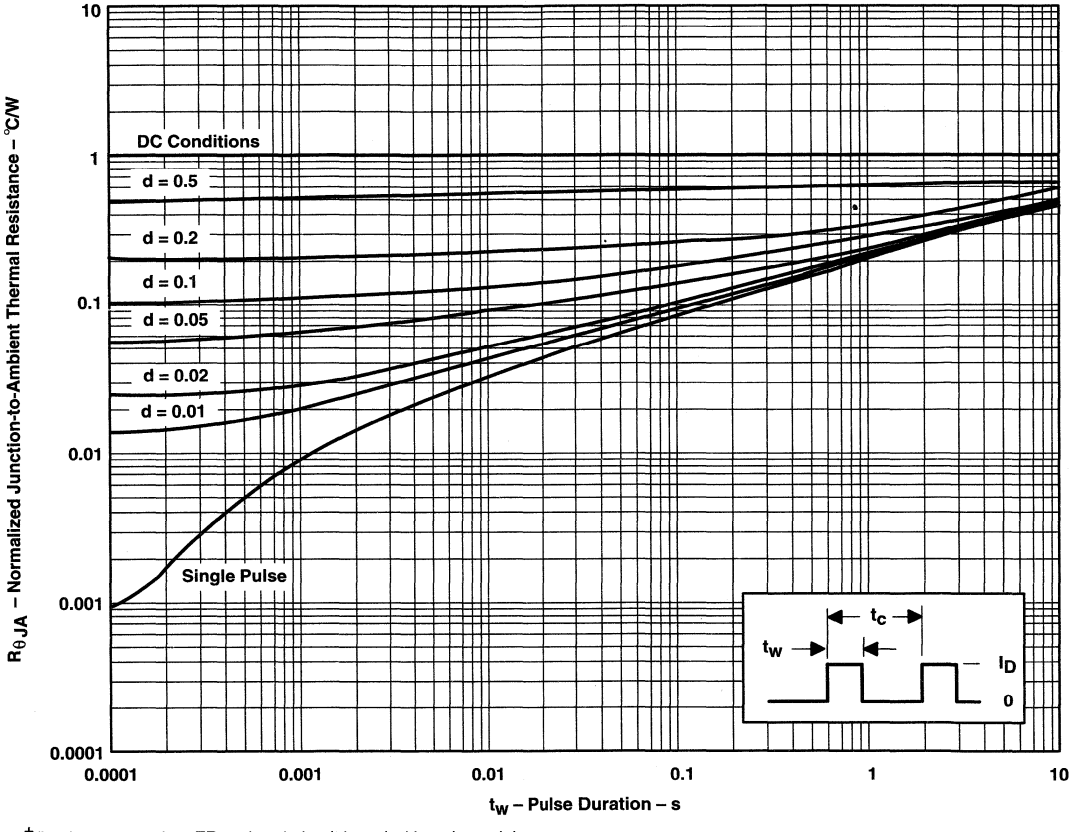
THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



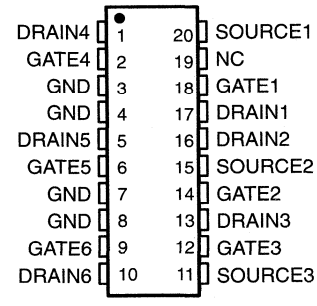
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 18

- **Low $r_{DS(on)}$ . . . 0.3 Ω Typ**
- **High-Voltage Output . . . 60 V**
- **Pulsed Current . . . 8 A Per Channel**
- **Fast Commutation Speed**

DW PACKAGE
(TOP VIEW)



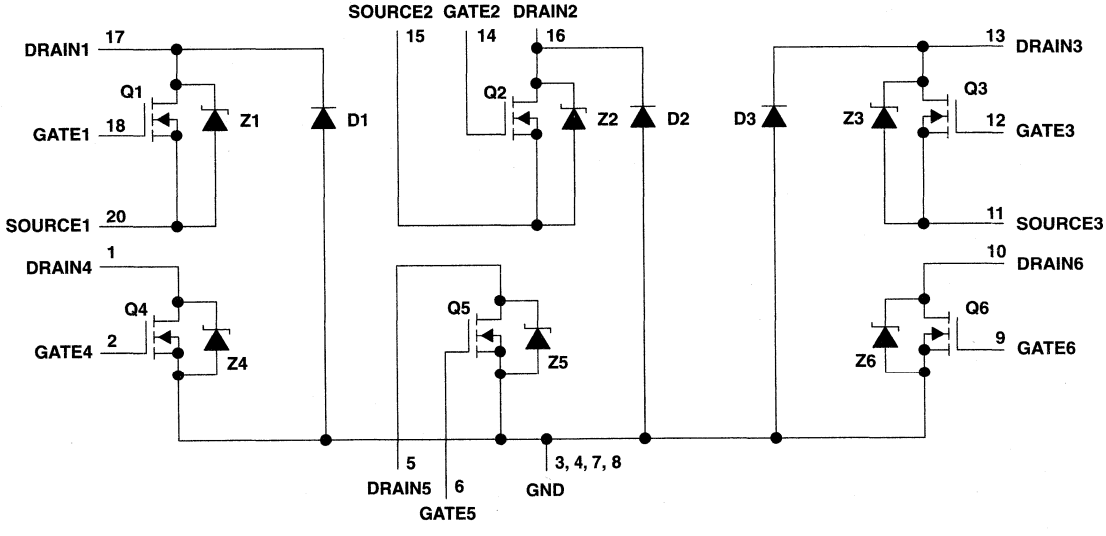
NC – No internal connection

description

The TPIC5601 is a monolithic power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors, three of which are configured with a common source. The TPIC5601 is offered in a 20-pin wide-body surface-mount (DW) package.

The TPIC5601 is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q4, Q5, and Q6)	60 V
Gate-to-source voltage range, V_{GS}	±20 V
Continuous drain current, each output, T_C = 25°C	1.7 A
Continuous source-to-drain diode current	1.7 A
Pulsed drain current, I_D, each output, T_C = 25°C (see Note 1 and Figure 15)	8 A
Single-pulse avalanche energy, E_A, T_C = 25°C (see Figures 4 and 16)	36 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.7 A, V_{GS} = 10 V, See Notes 2 and 3			0.51	0.6	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.7 A (D1, D2, D3), See Notes 2 and 3			7.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.7 A, V_{GS} = 0 (Z1, Z2, Z3, Z4, Z5, Z6), See Notes 2 and 3			1	1.2	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1.7 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.41	0.5	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3	I_D = 1 A,	1.2	1.75		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz	V_{GS} = 0,		190	240	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z1, Z2, Z3), See Figure 1		65		ns
Q_{RR}	Total diode charge			0.12		µC
$t_{rr(SD)}$	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z4, Z5, Z6), See Figure 1		240		ns
Q_{RR}	Total diode charge			0.9		µC

GND-to-drain diode characteristics, T_C = 25°C (see schematic, D1, D2, and D3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 1 A, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		260		ns
Q_{RR}	Total diode charge			2.2		µC

resistive-load switching characteristics, T_C = 25°C

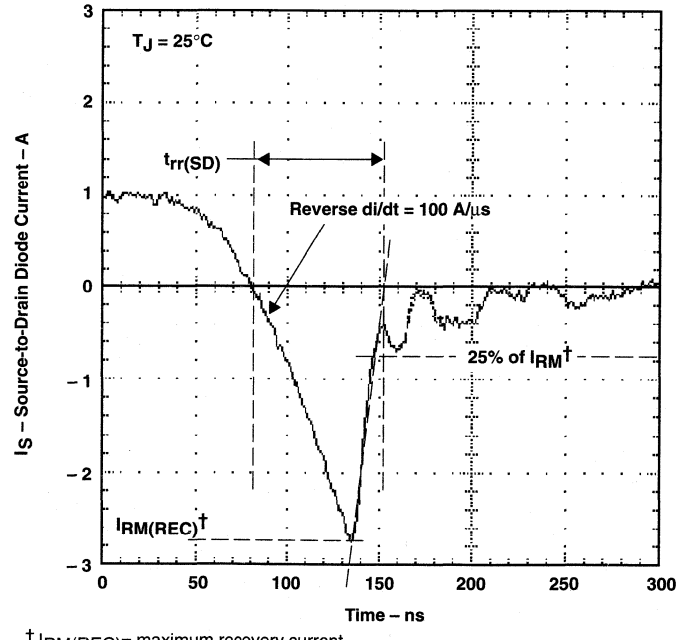
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		32	65	ns
$t_{d(off)}$	Turn-off delay time			40	80	
t_{r2}	Rise time			15	30	
t_{f2}	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		5	6	nC
Q_{GS}	Threshold gate-to-source charge			0.5	0.6	
Q_{GD}	Gate-to-drain charge			1.9	2.3	
$L_{(drain)}$	Internal drain inductance			5		nH
$L_{(source)}$	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		90		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			27		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink.

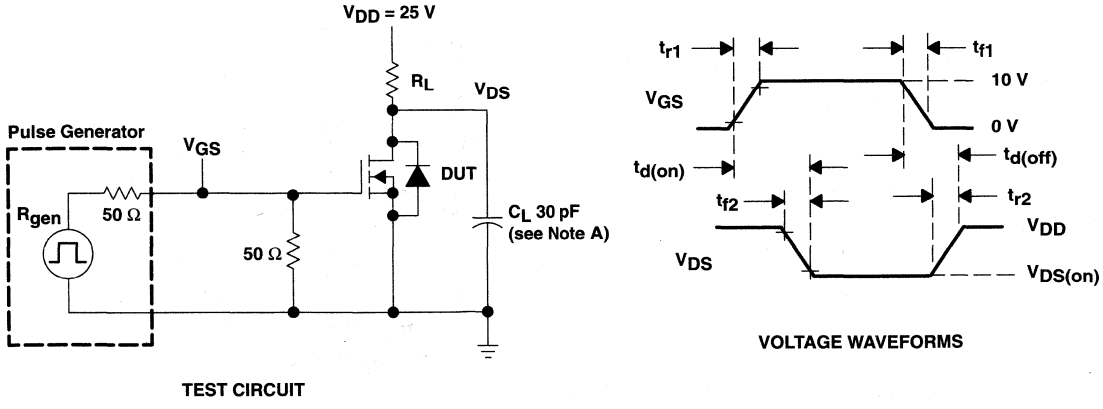
PARAMETER MEASUREMENT INFORMATION



† $I_{RM(REC)}$= maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

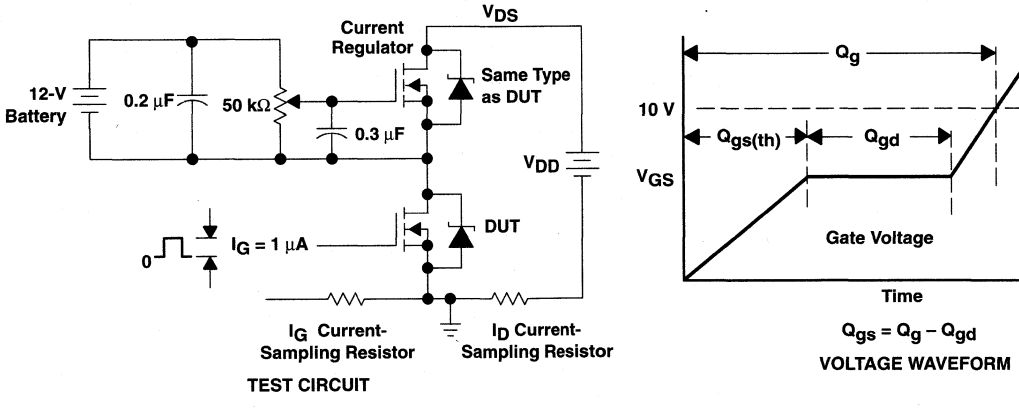
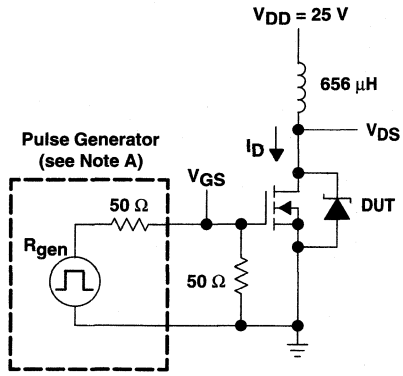
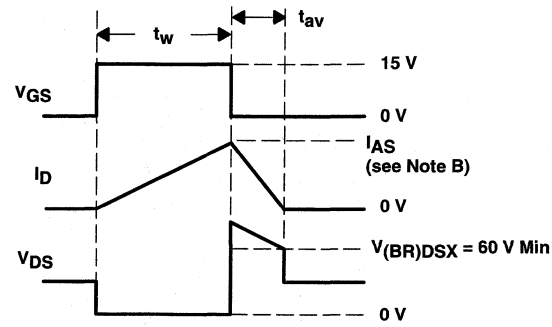


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 8$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 36$ mJ, where

tav = Avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

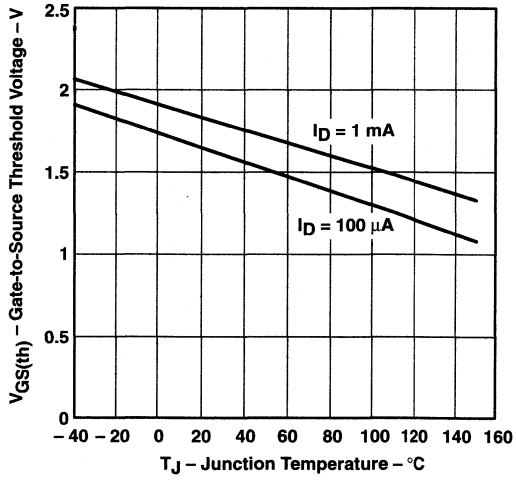


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

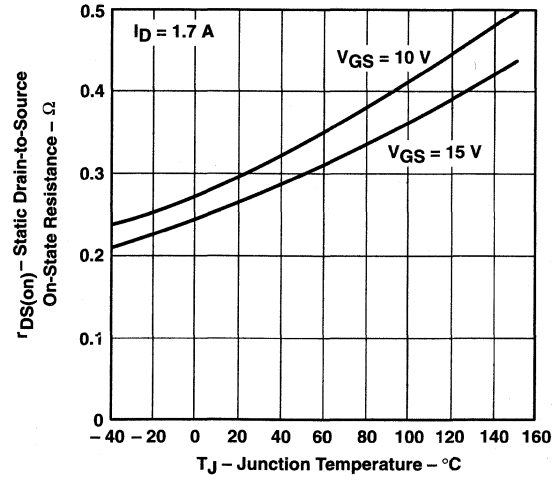


Figure 6

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

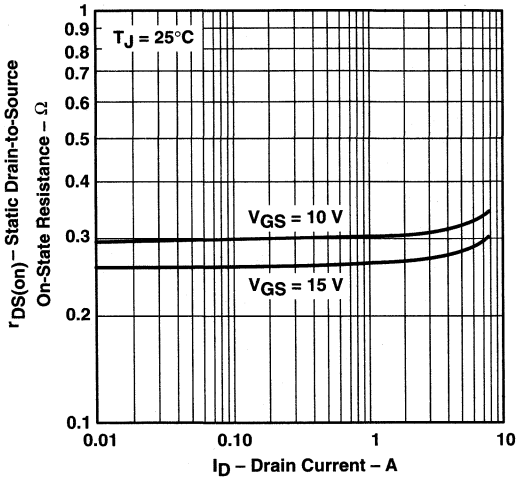


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

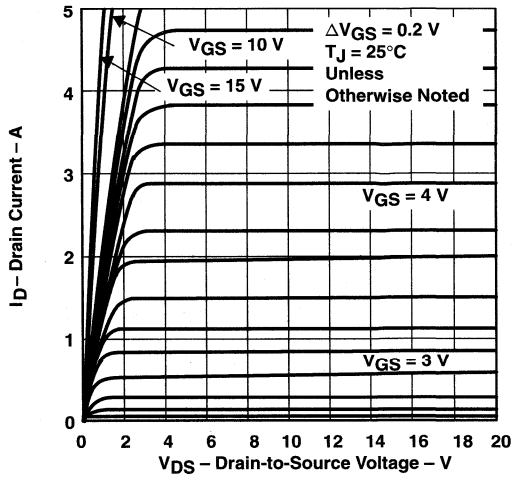


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

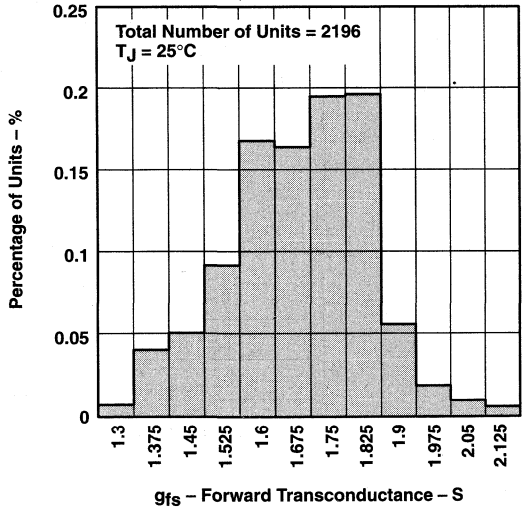


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

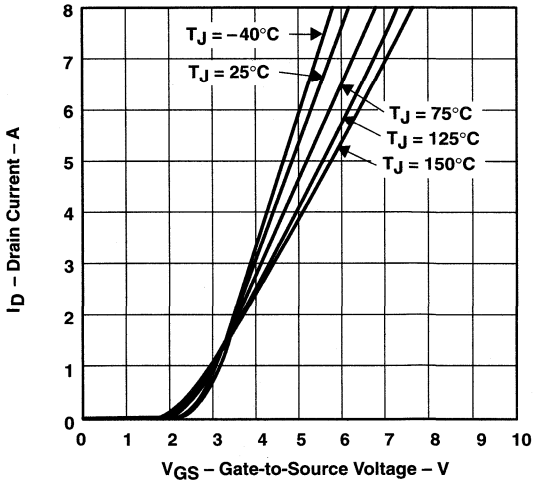


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

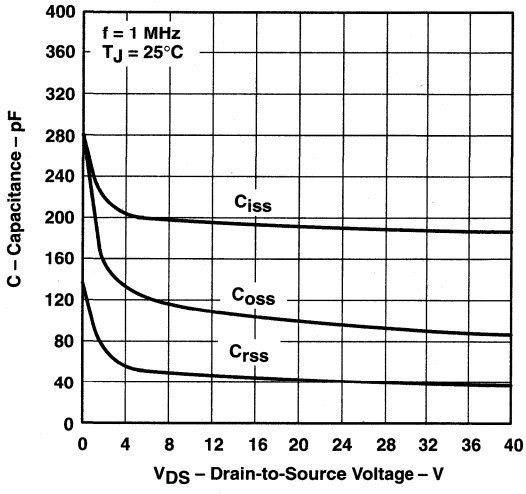


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

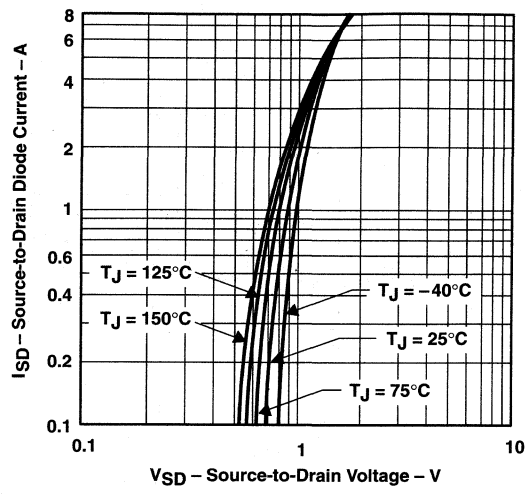


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

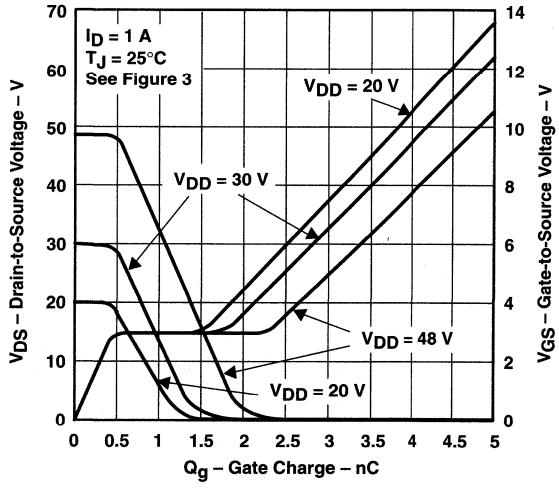


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

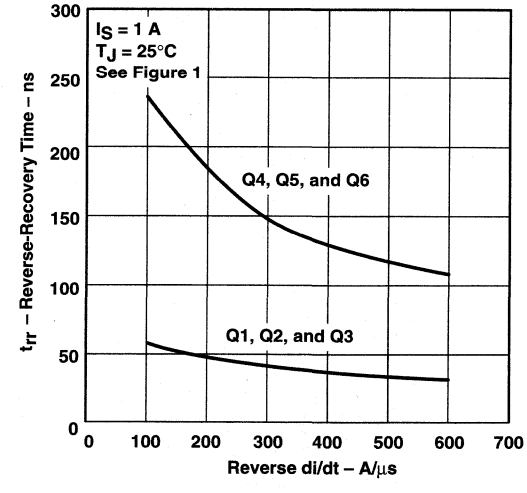
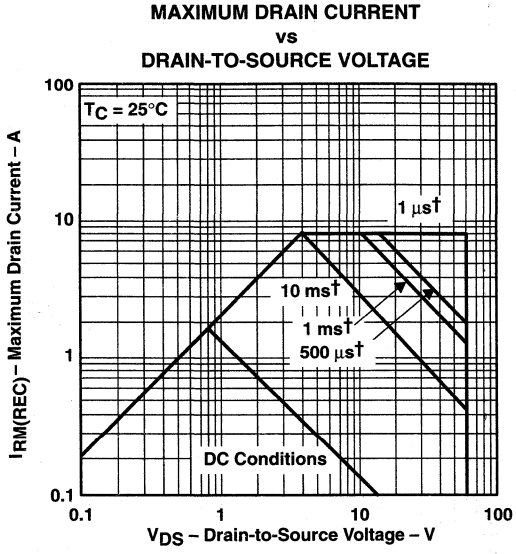


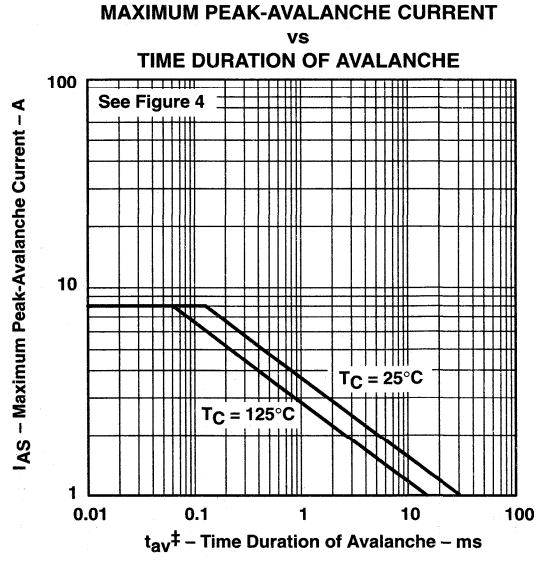
Figure 14

THERMAL INFORMATION



† Less than 0.1 duty cycle

Figure 15

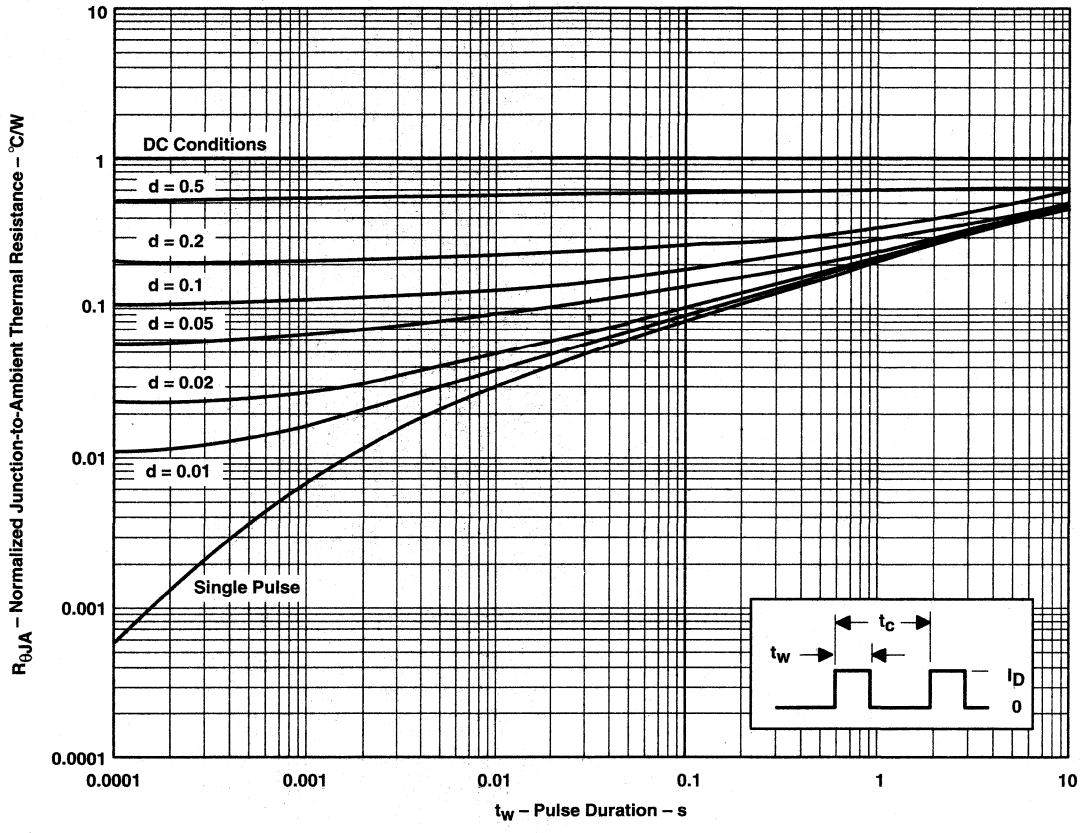


‡ Non-JEDEC symbol for avalanche time.

Figure 16

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



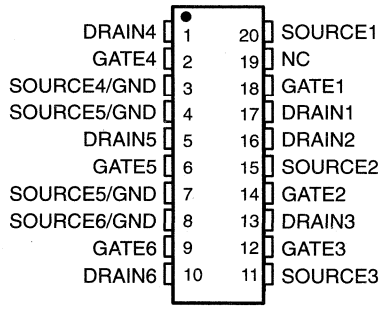
† Device mounted on FR4 printed-circuit board with no heatsink

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_w = pulse duration
t_c = cycle time
d = duty cycle = t_w/t_c

Figure 17

- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Output . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)



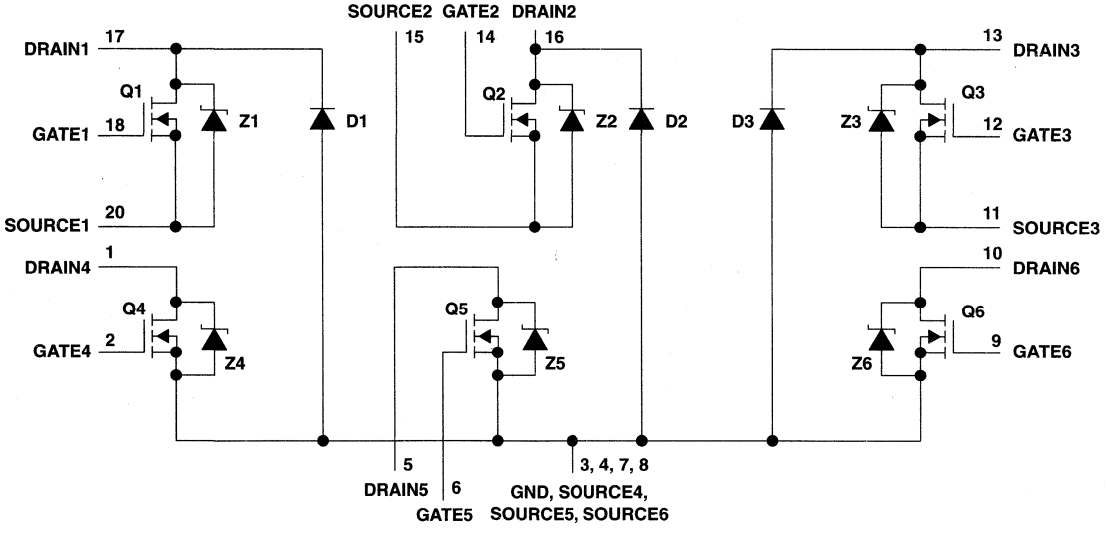
NC – No internal connection

description

The TPIC5621L is a monolithic logic-level power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors, three of which are configured with a common source.

The TPIC5621L is offered in a 20-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q4, Q5, and Q6)	60 V
Gate-to-source voltage range, V_{GS}	±20 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, I_{max}, T_C = 25°C (each output, see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15 and 16)	162 mJ
Continuous total dissipation (see Figure 15)	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, V_{GS} = 5 V, See Notes 2 and 3			0.4	0.48	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4, Z5, Z6), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2, D3), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V (D1, D2, D3)	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.48	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figure 9		1	1.29	1.45	S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			190	240	pF
C_{oss}	Short-circuit output capacitance, common source				100	125	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	50	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 0.5 A, V_{DS} = 48 V, V_{GS} = 0, di/dt = 100 A/µs, See Figures 1 and 14	Z1, Z2, Z3		65		ns
			Z4, Z5, Z6		150		
			D1, D2, D3		200		
Q_{RR}	Total diode charge		Z1, Z2, Z3		0.06		µC
			Z4, Z5, Z6		0.3		
			D1, D2, D3		0.7		

resistive-load switching characteristics, T_C = 25°C

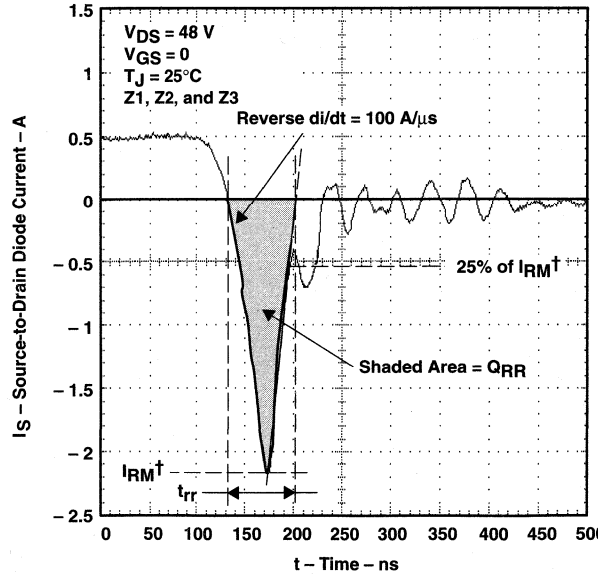
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		34	68	ns
$t_{d(off)}$	Turn-off delay time			41	32	
t_r	Rise time			21	42	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 5 V, See Figure 3		3.1	3.7	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			1.9	2.3	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	All outputs with equal power		90		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			27		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION

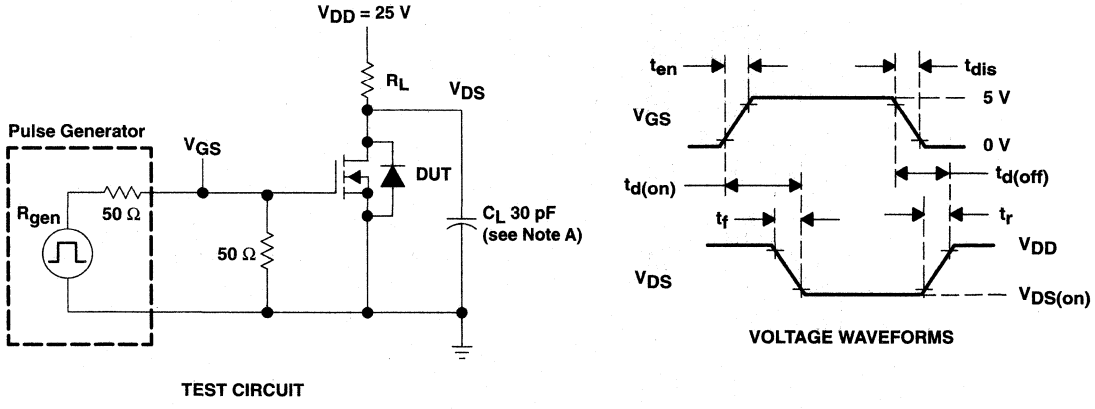


† I_{RM} = maximum recovery current

NOTE A. The above waveform is representative of Z4, Z5, Z6, D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

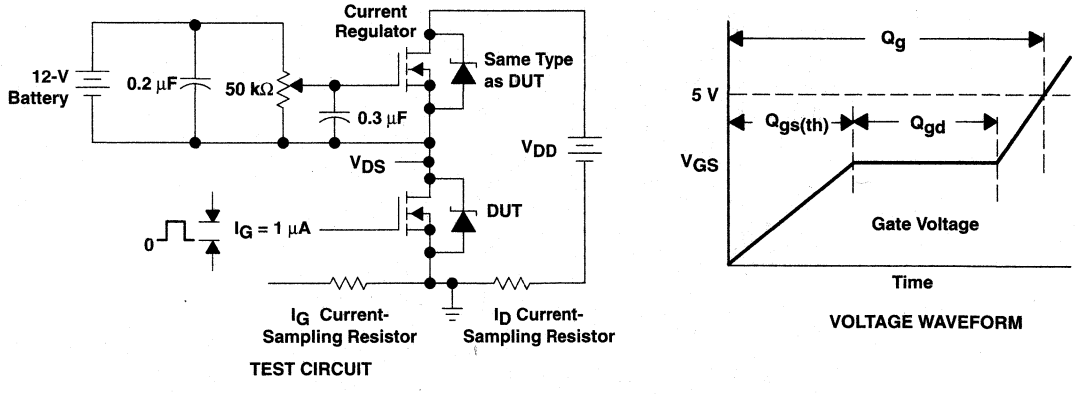
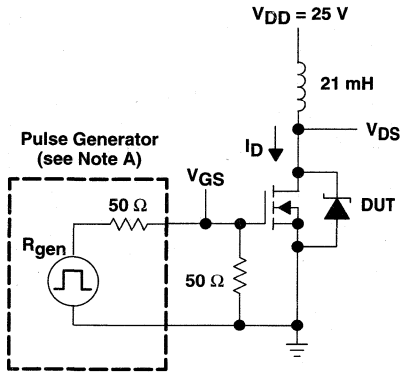
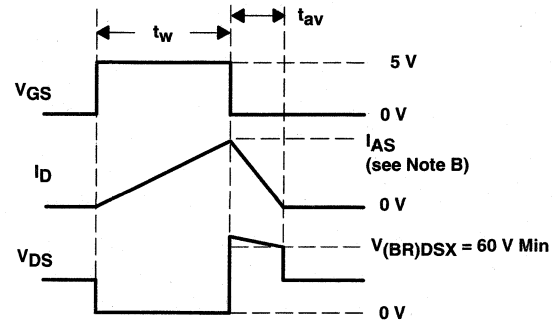


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 162$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

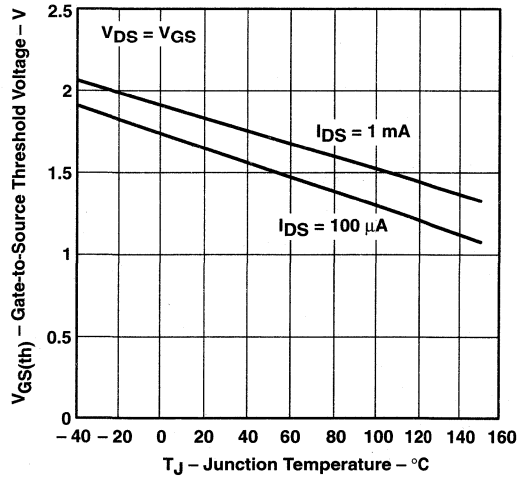


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

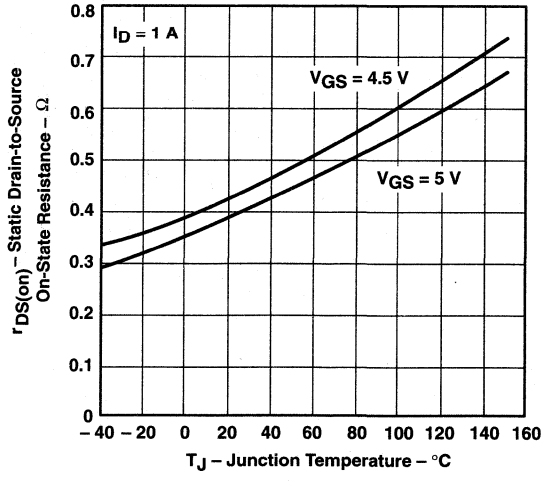


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

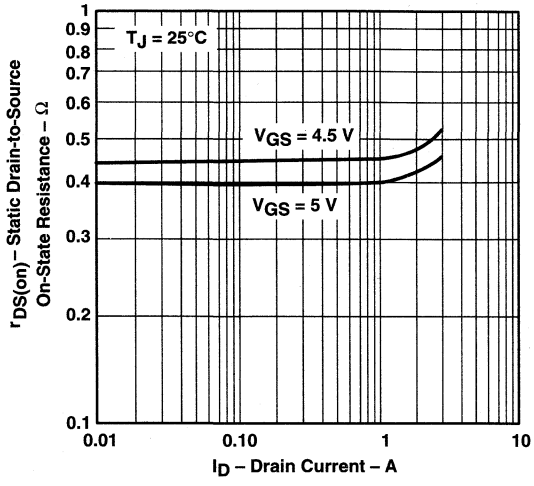


Figure 7

DRAIN-TO-SOURCE CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

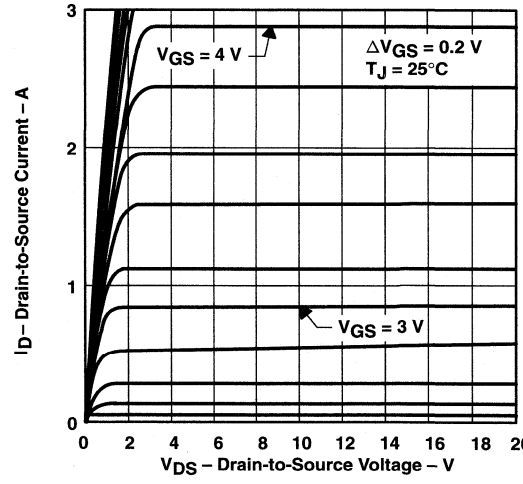


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

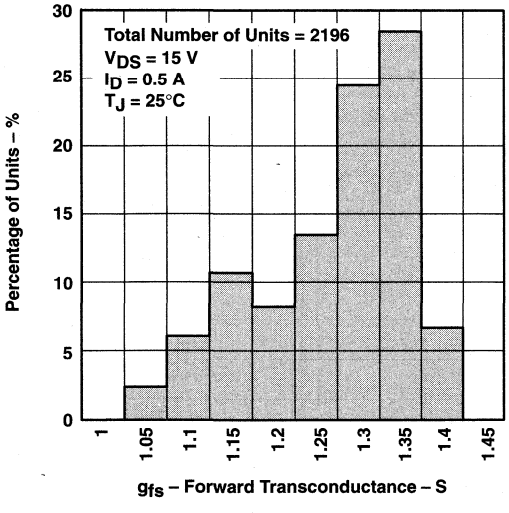


Figure 9

DRAIN-TO-SOURCE CURRENT
vs
GATE-TO-SOURCE VOLTAGE

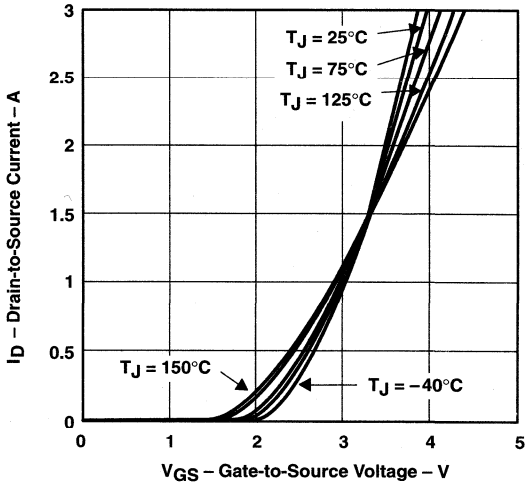


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

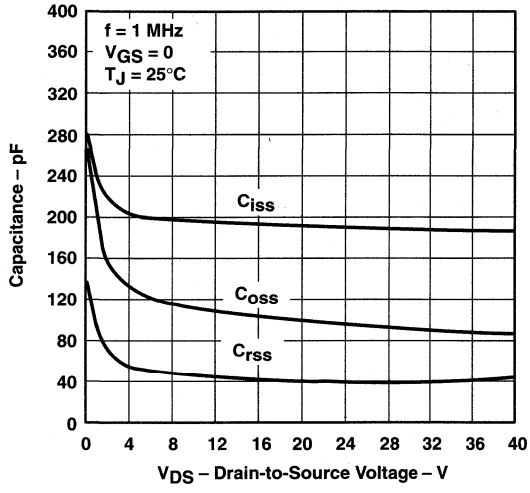


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

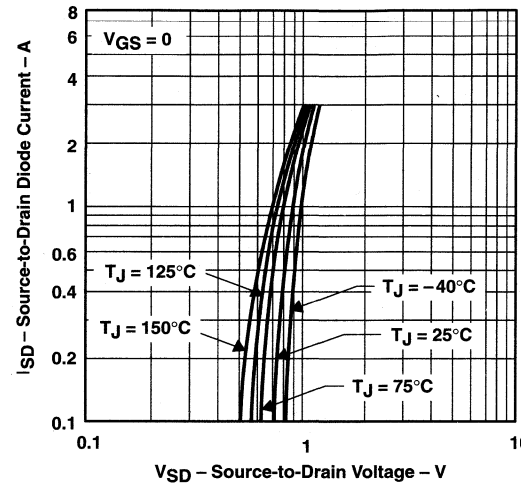


Figure 12

DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

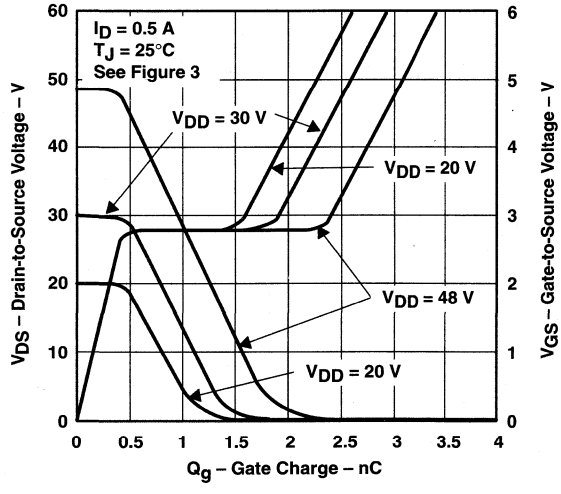


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

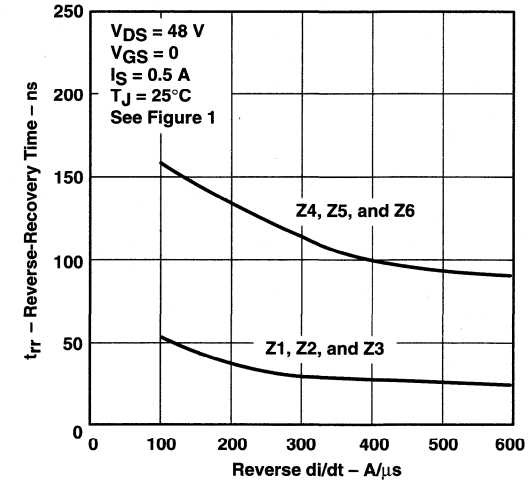
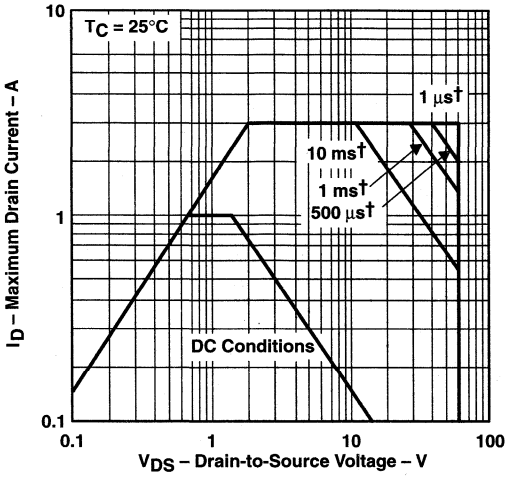


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

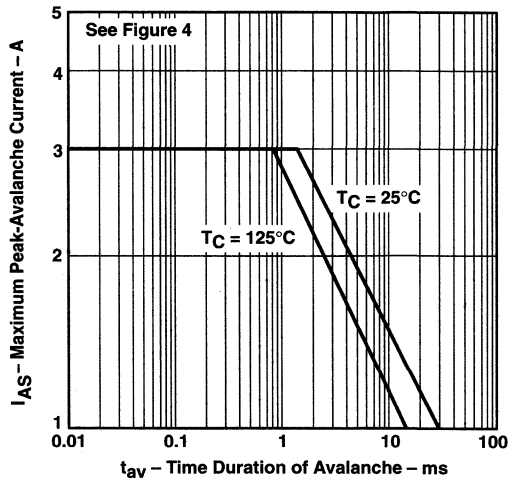
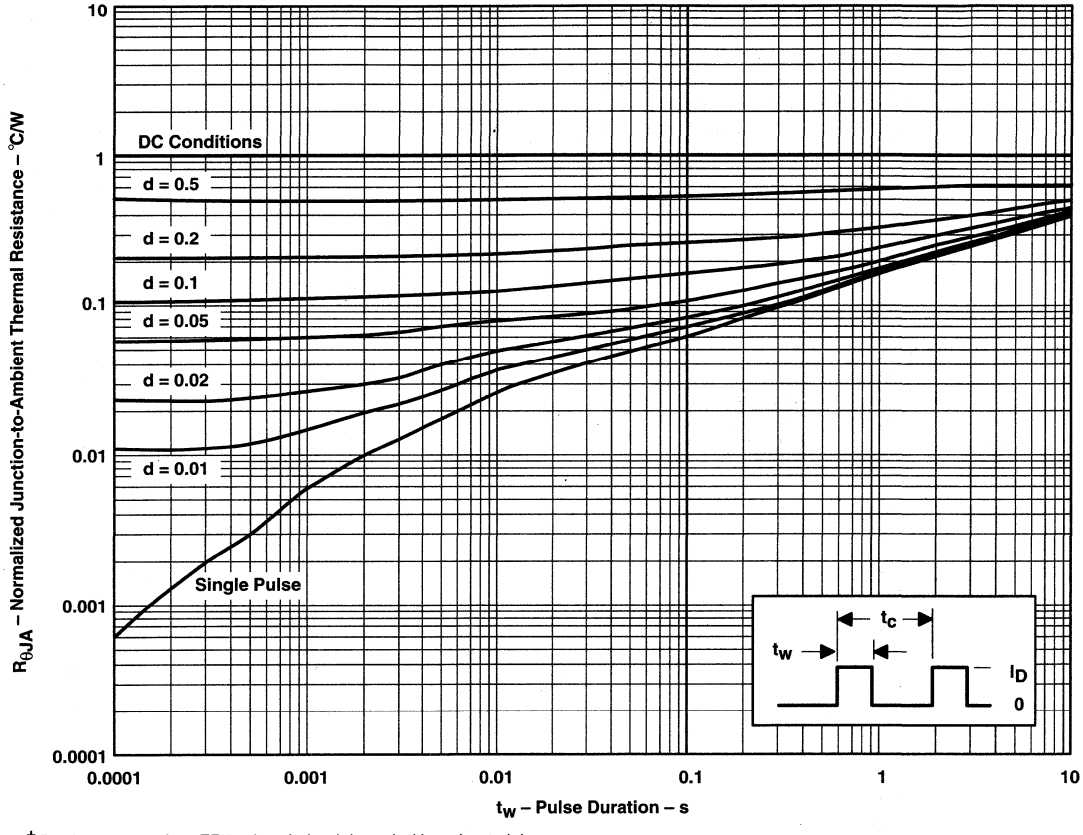


Figure 16

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



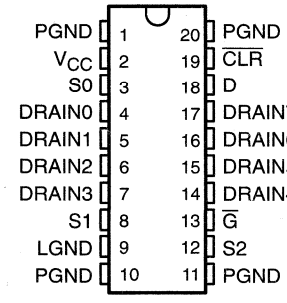
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W / t_C

Figure 17

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Four Distinct Function Modes**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



description

This power logic 8-bit addressable latch controls open-drain DMOS transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of storing single-line data in eight addressable latches with 3-to-8 decoding or demultiplexing mode active-low DMOS outputs.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
CLR	G	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

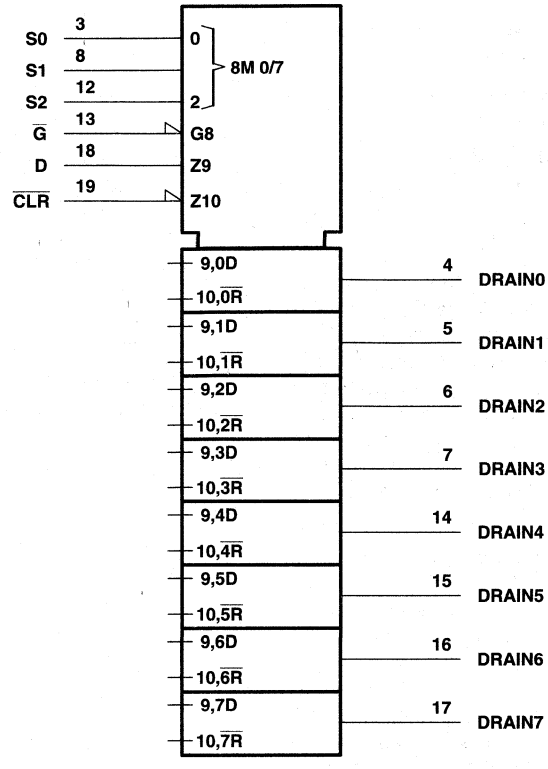
SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 9, logic ground (LGND), and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

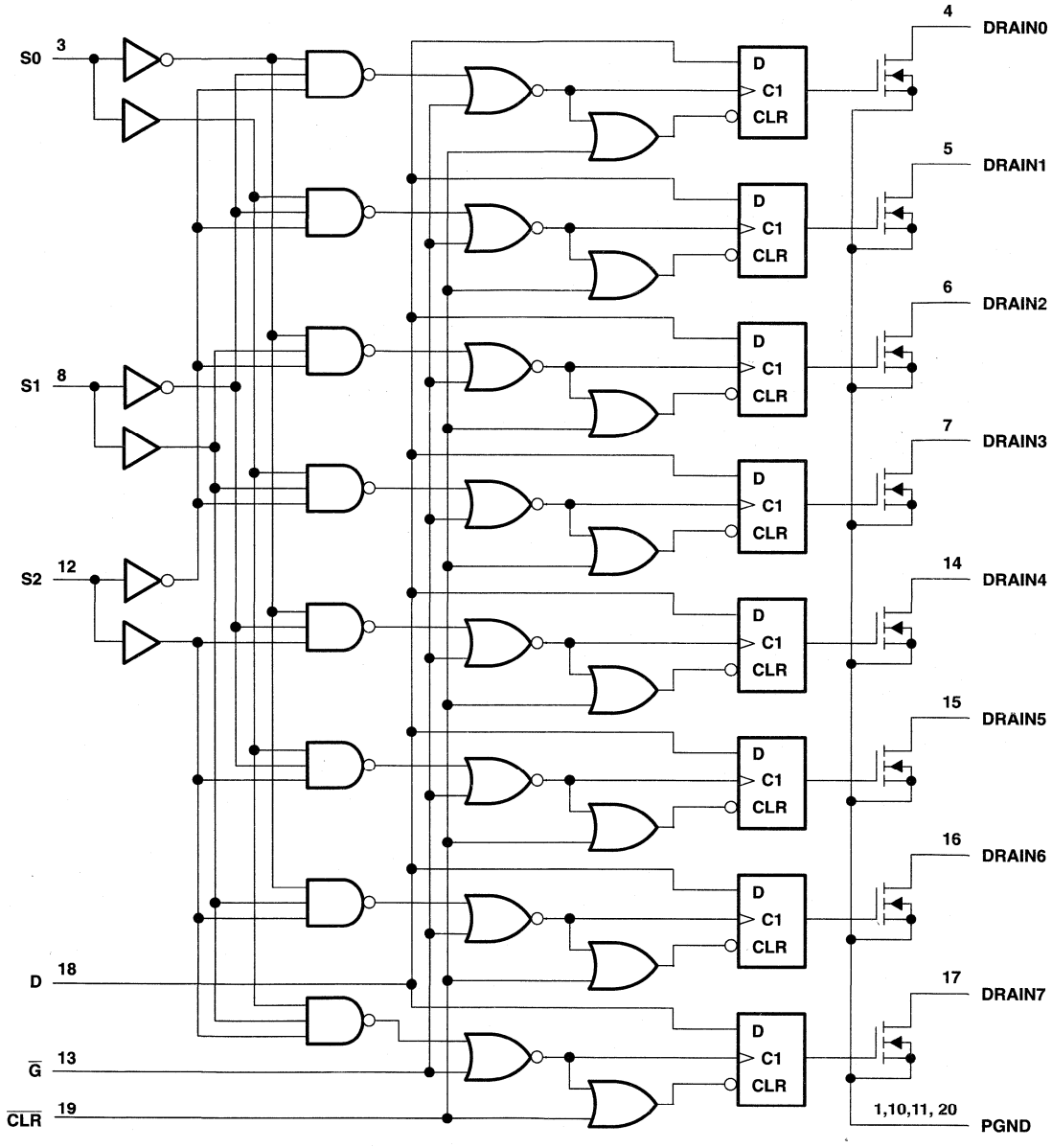
The TPIC6259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

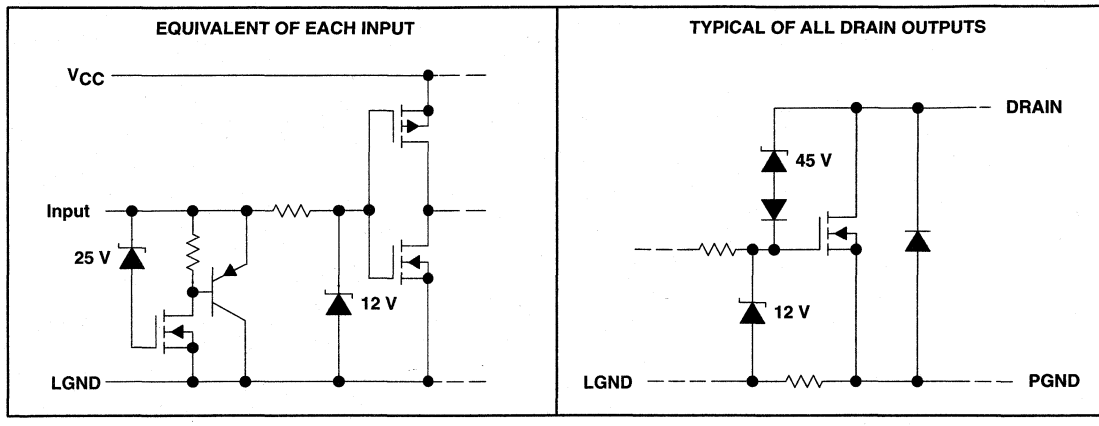


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Note 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature, (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high after $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, $V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, T_C = 85°C, See Notes 5, 6, and 7			250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from D	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 10		625		ns
t_{PHL}	Propagation delay time, high-to-low-level output from D			140		ns
t_r	Rise time, drain output			650		ns
t_f	Fall time, drain output			400		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

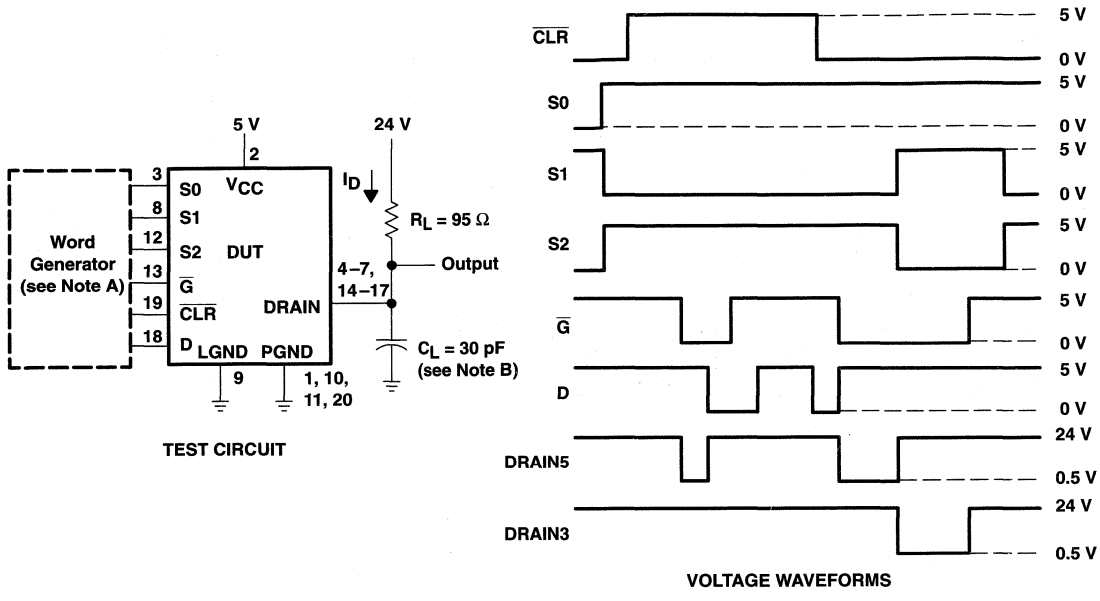


Figure 1. Typical Operation Mode

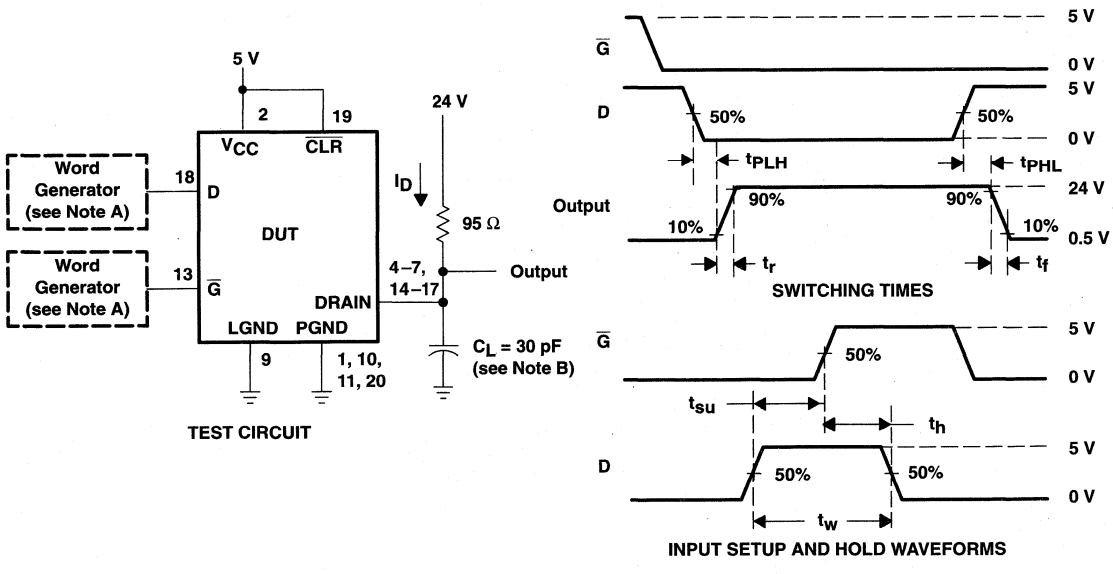
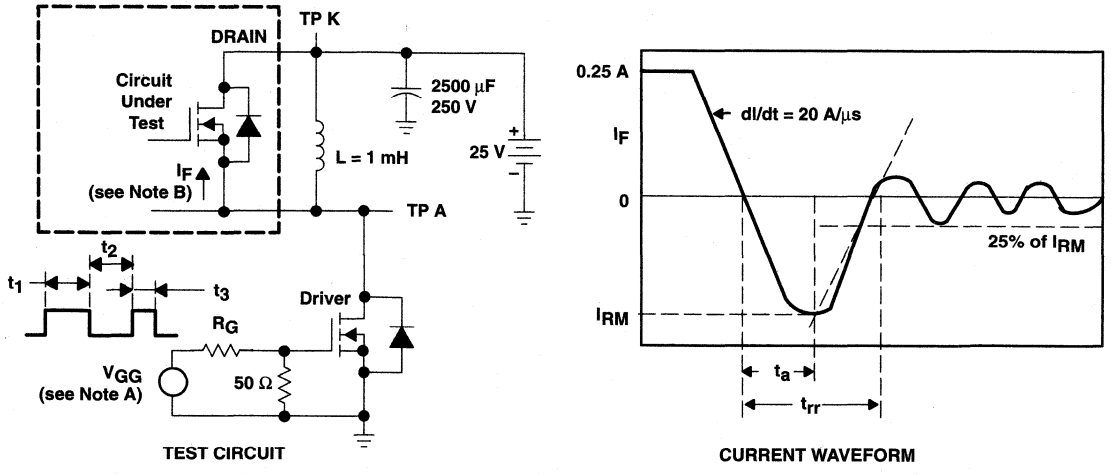


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

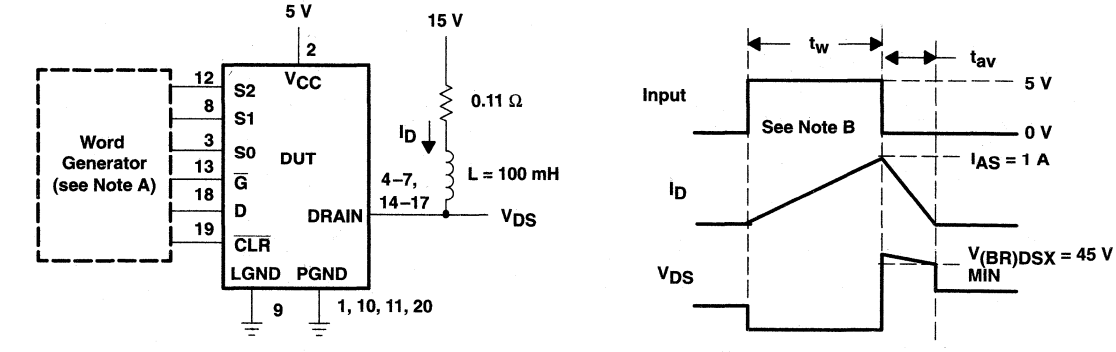
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



TEST CIRCUIT VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

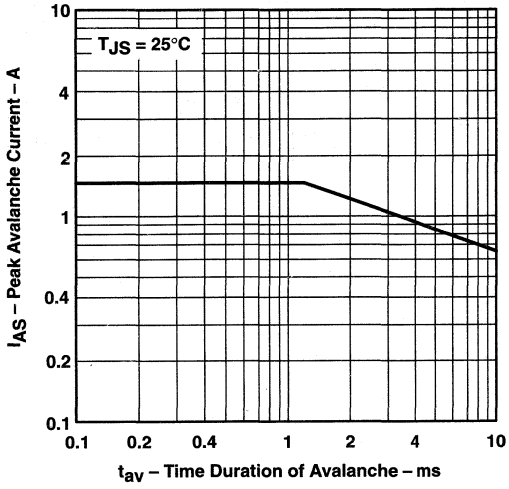


Figure 5

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

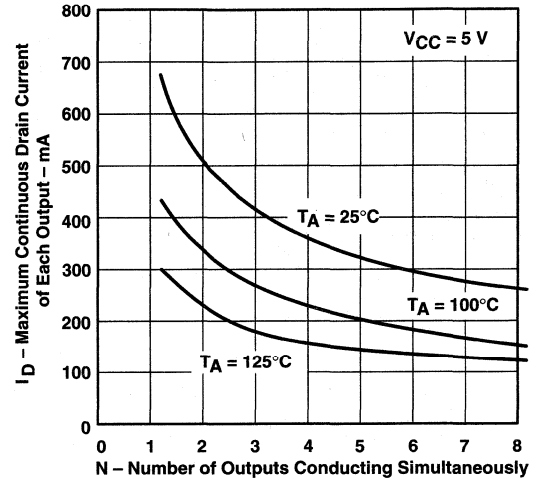


Figure 6

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

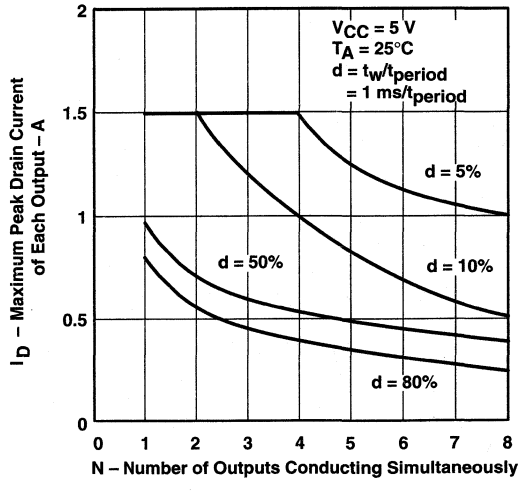


Figure 7

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

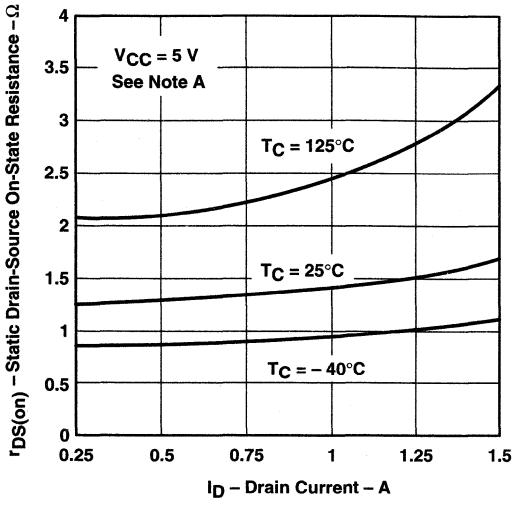


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

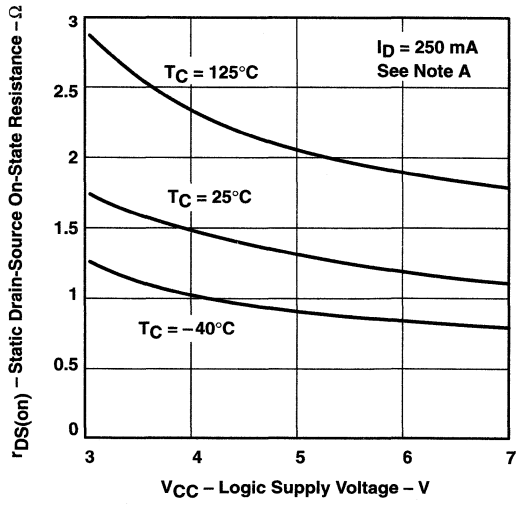


Figure 9

SWITCHING TIME vs FREE-AIR TEMPERATURE

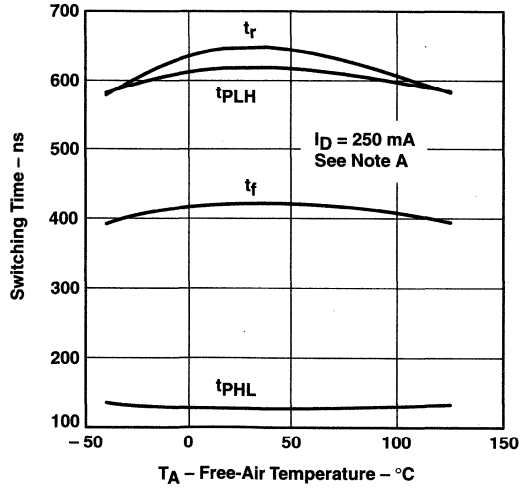


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

- Low $r_{DS(on)}$ . . . 1.3 Ω Typ
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage up to 45 V
- Low Power Consumption

description

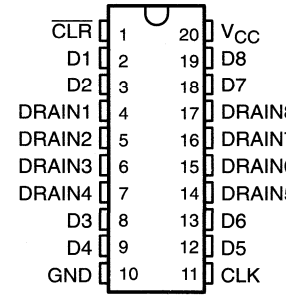
The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

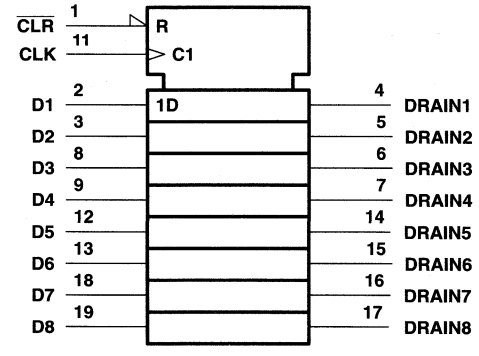
When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of −40°C to 125°C.

DW OR N PACKAGE
(TOP VIEW)



logic symbol†



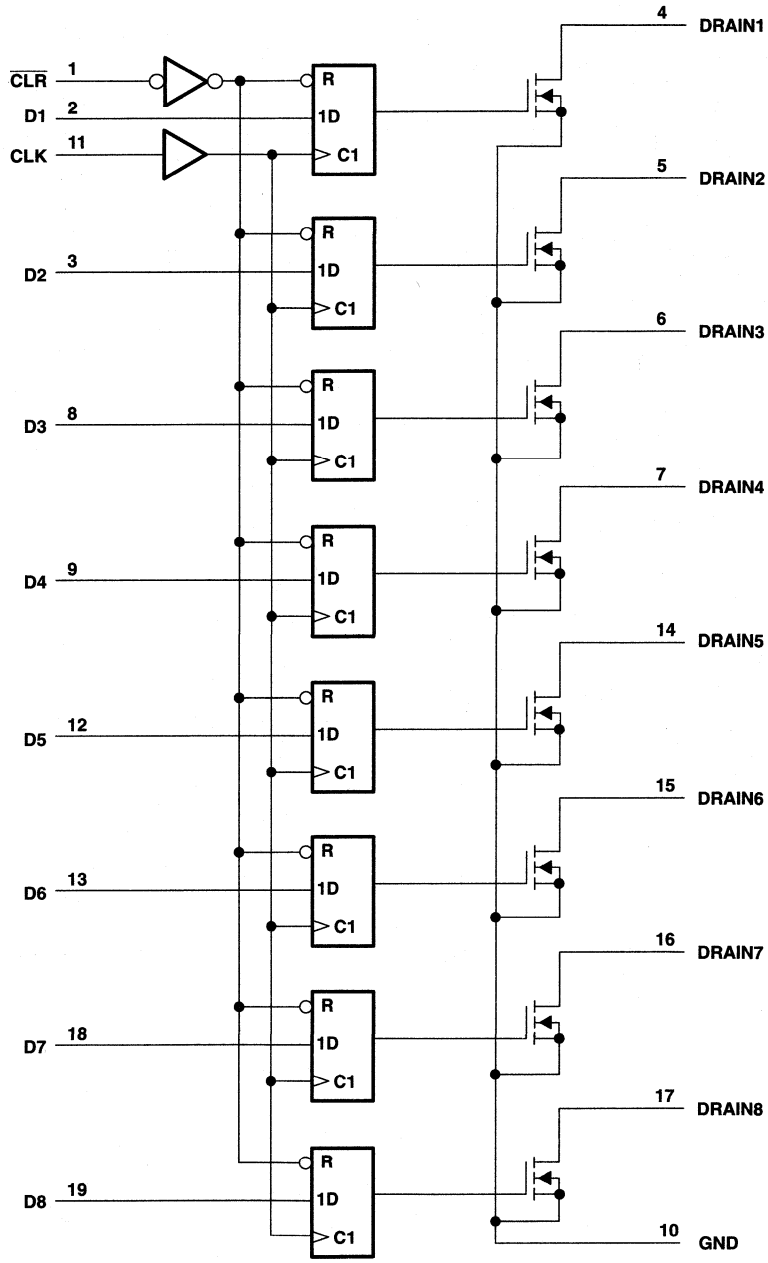
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each channel)

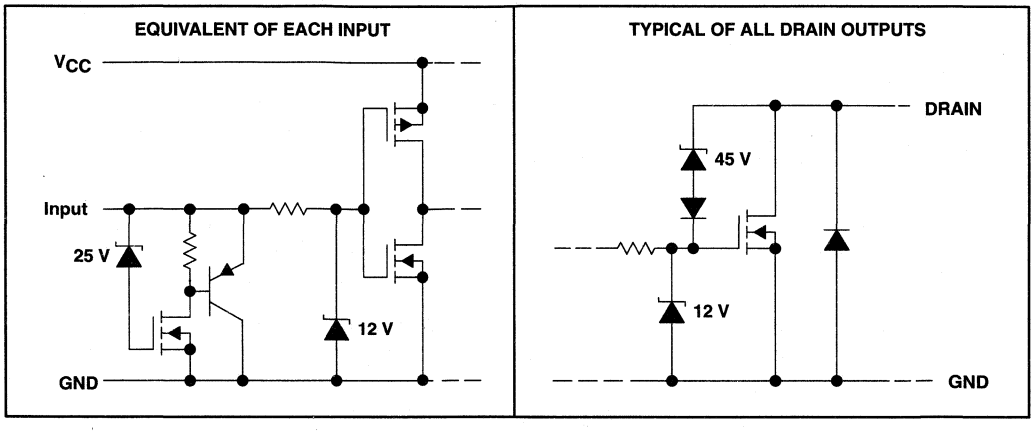
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	DRAIN
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, D high before CLK↑, t_{su} (see Figure 2)	10		ns
Hold time, D high after CLK↑, t_h (see Figure 2)	15		ns
Pulse duration, t_w (see Figure 2)	25		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 10		625		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK			150		ns
t_r	Rise time, drain output			675		ns
t_f	Fall time, drain output			400		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

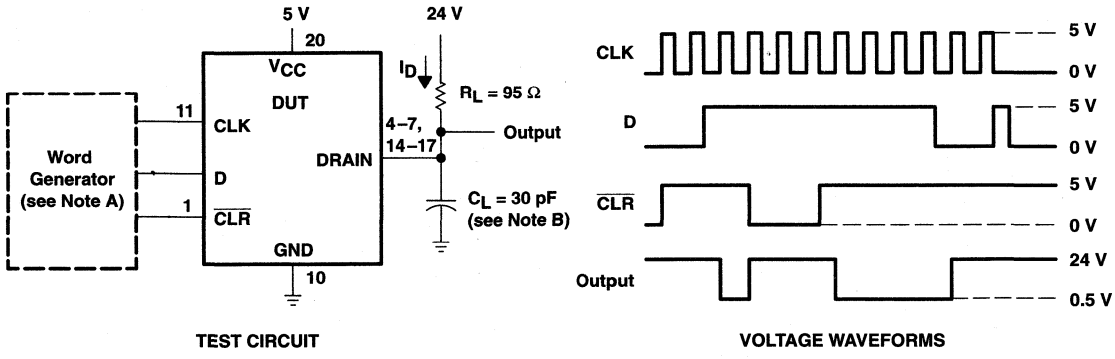


Figure 1. Resistive Load Normal Operation

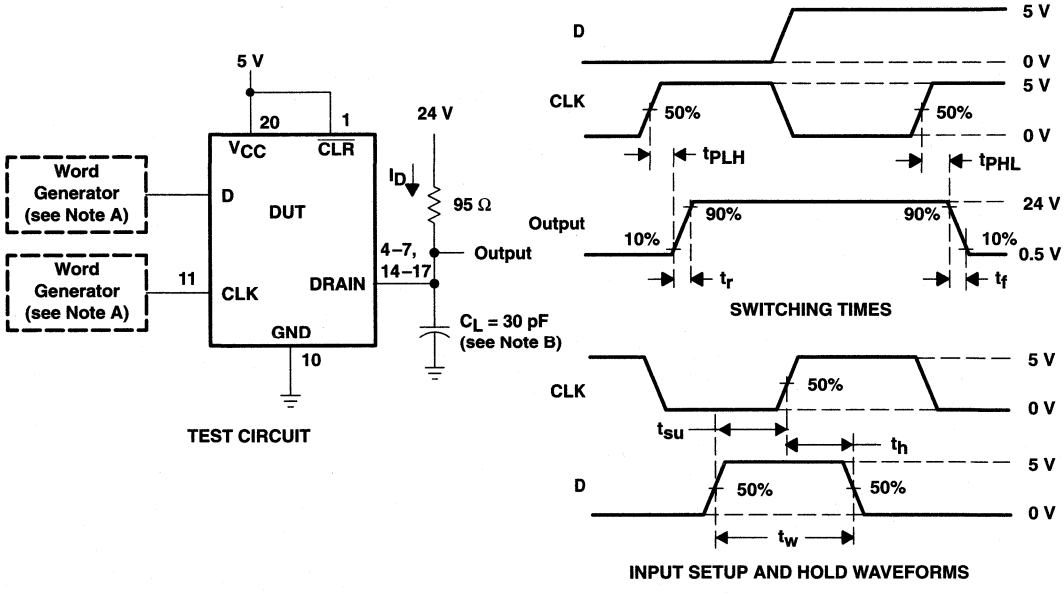
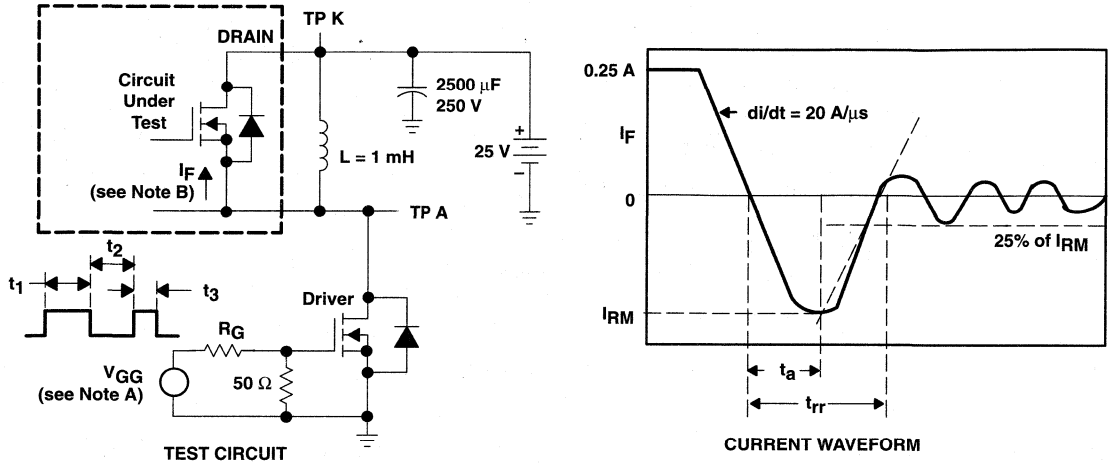


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

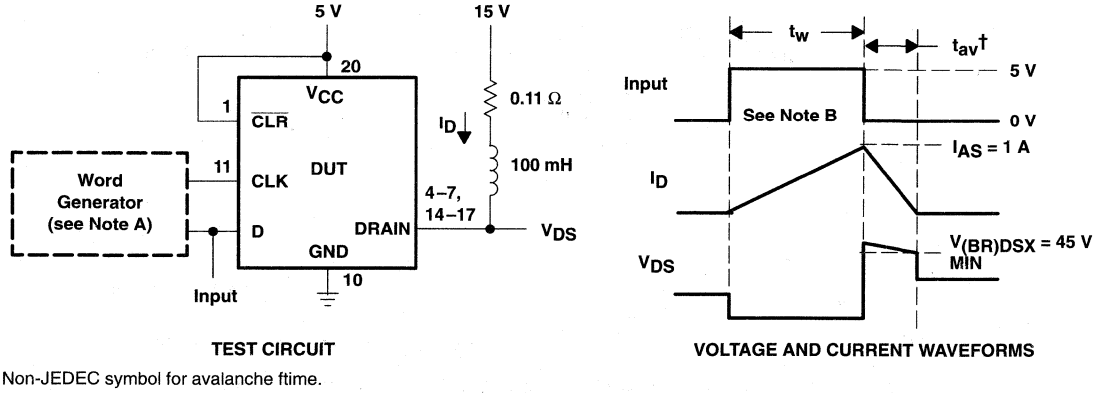
NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 KHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche ftime.

NOTES: A. The word generator A has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

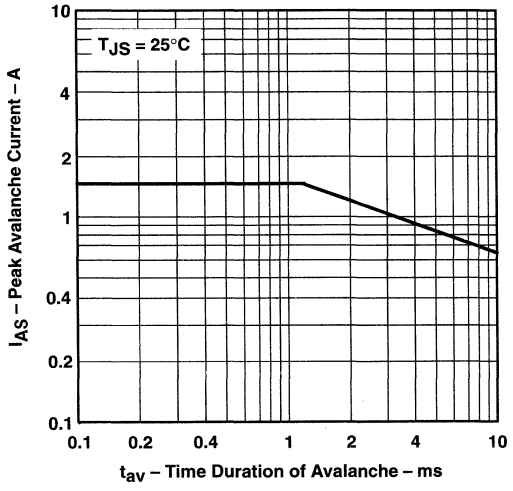


Figure 5

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

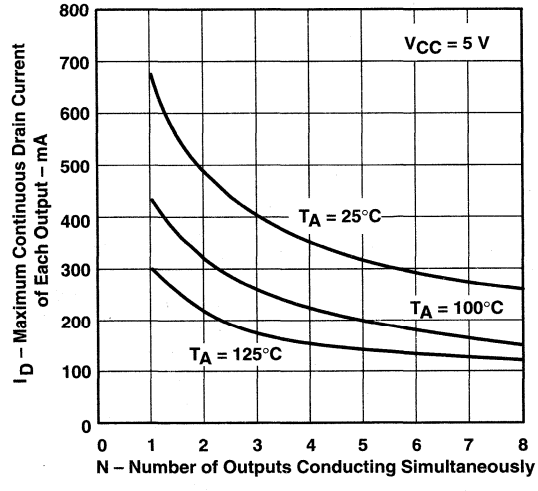


Figure 6

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

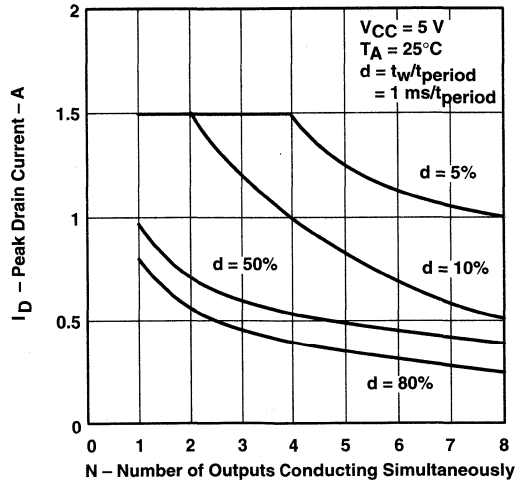


Figure 7

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

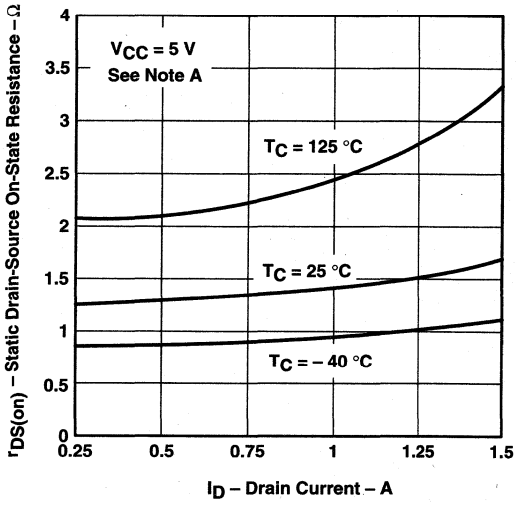


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

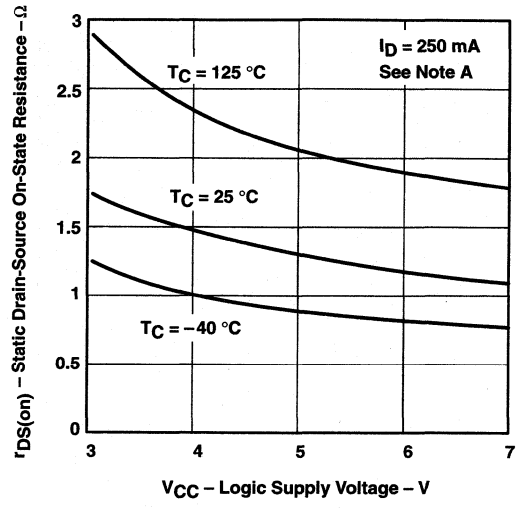


Figure 9

SWITCHING TIME vs FREE-AIR TEMPERATURE

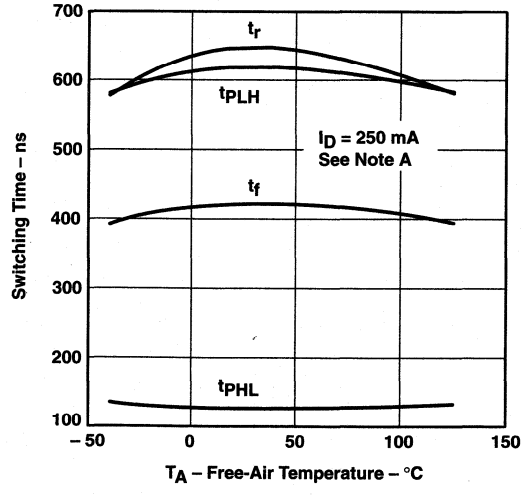
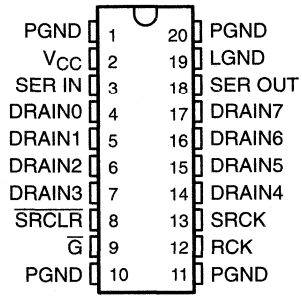


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Devices Are Cascadable**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)

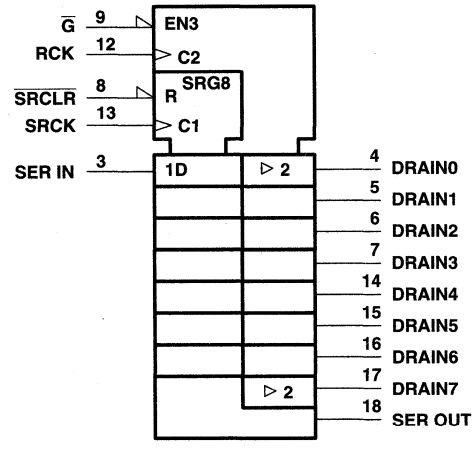


description

The TPIC6595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†



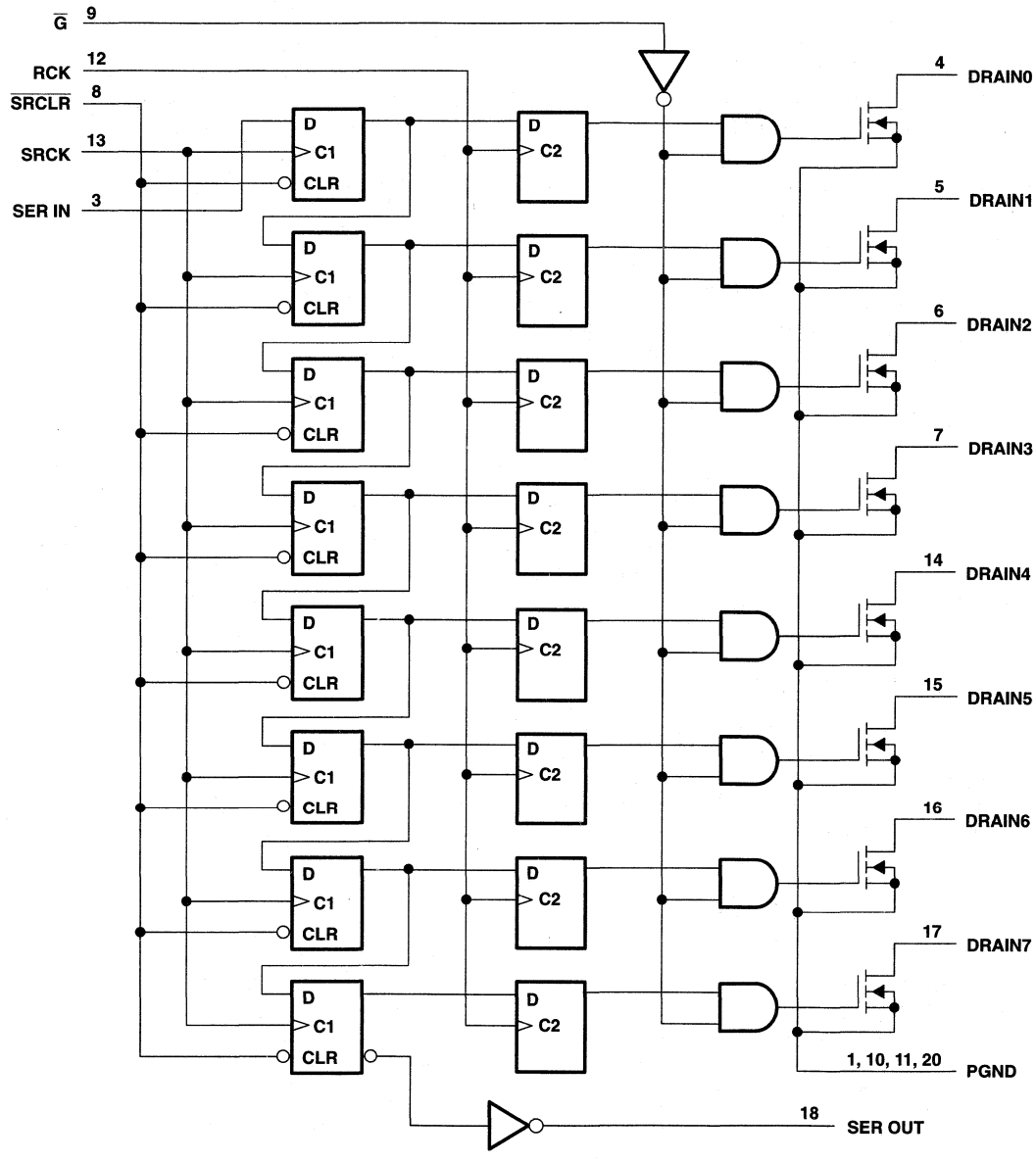
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND) and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



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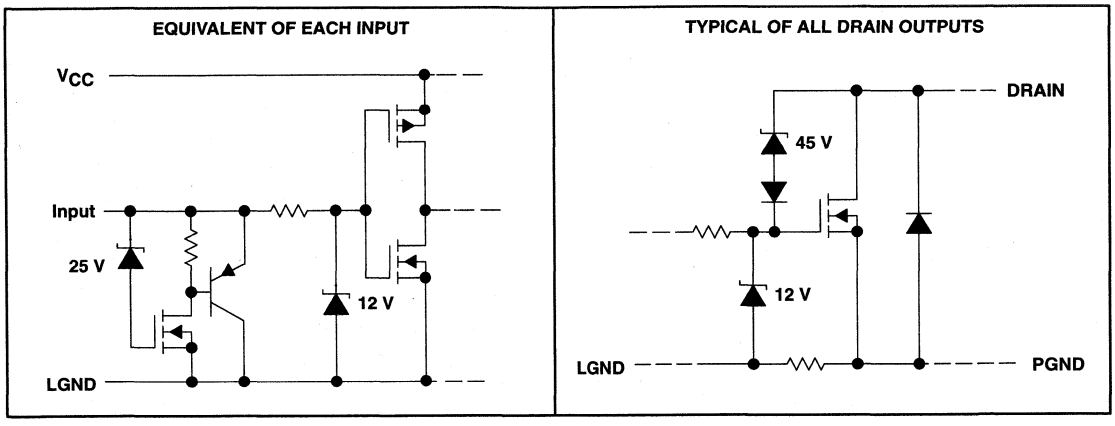
schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %
4. DRAIN supply voltage = 15 V, starting junction temperature, (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 mA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = −4 mA, V_{CC} = 4.5 V		4.1	4.3		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 mA, V_{CC} = 4.5 V			0.002	0.1	V
		I_{OH} = 4 mA, V_{CC} = 4.5 V			0.2	0.4	
hys	Input hysteresis	V_{DS} = 15 V			1.3		V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CCL}	Logic supply current	I_O = 0, All inputs low			15	100	µA
$I_{CC(FRQ)}$	Logic supply current frequency	f_{SRCK} = 5 MHz, I_O = 0, C_L = 30 pF, See Figure 1, Figure 2, and Figure 6			0.6	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 9 and 10		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 250 mA, See Figure 1 and Figure 2		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			150		ns
t_r	Rise time, drain output			750		ns
t_f	Fall time, drain output			425		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

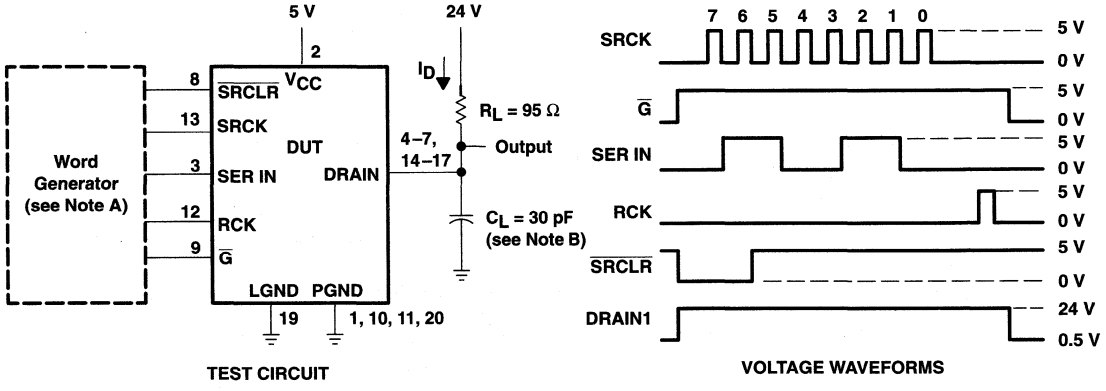


Figure 1. Resistive Load Operation

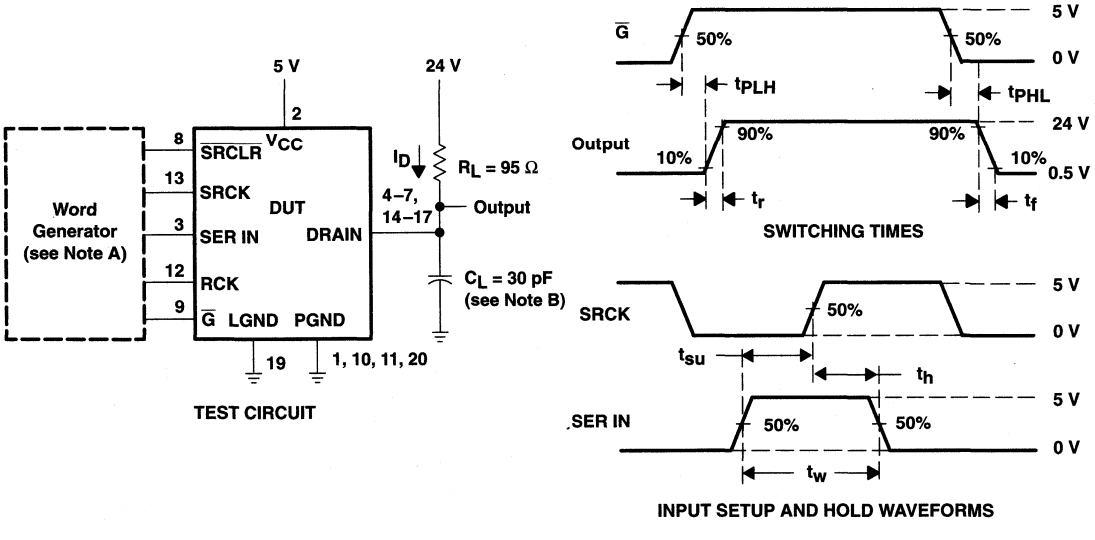
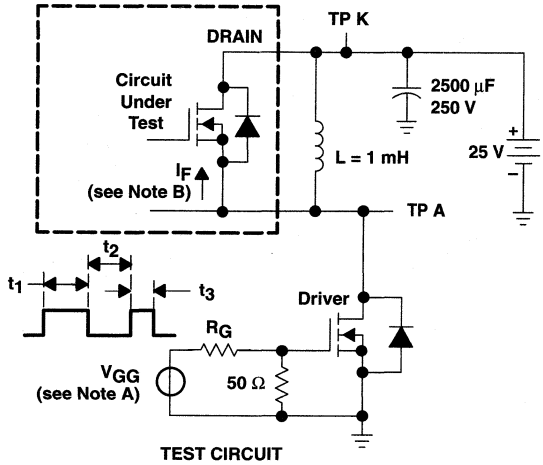


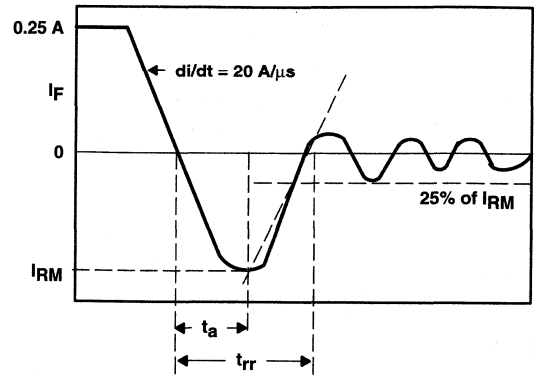
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



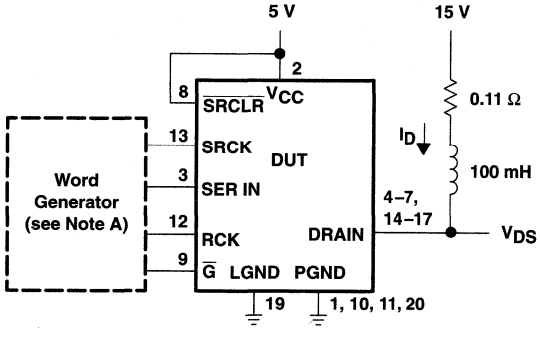
TEST CIRCUIT



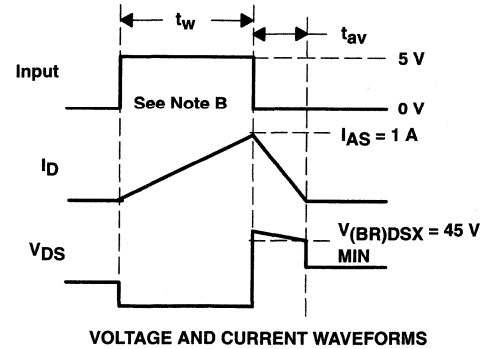
CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

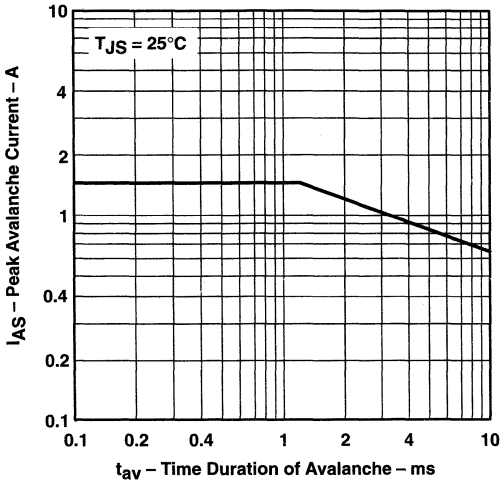


Figure 5

SUPPLY CURRENT
vs
FREQUENCY

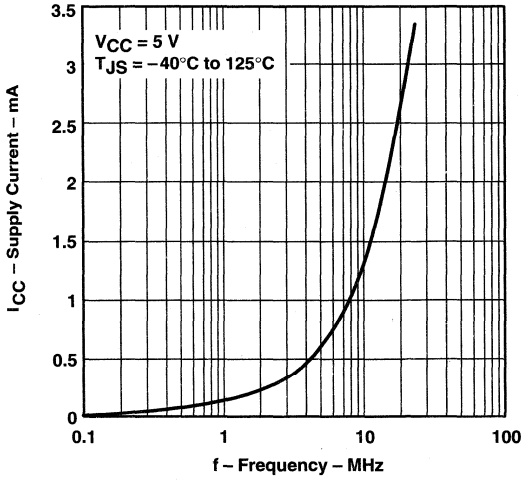


Figure 6

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

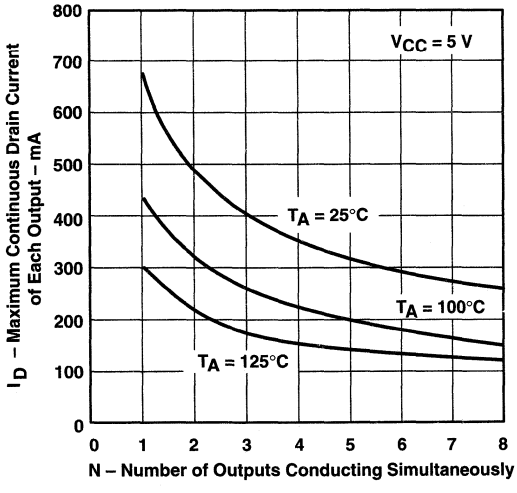


Figure 7

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

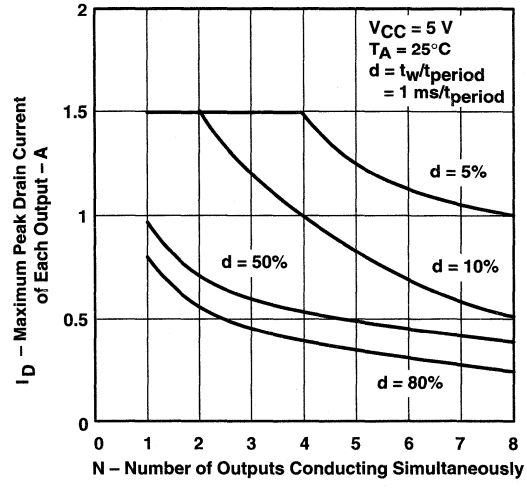


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

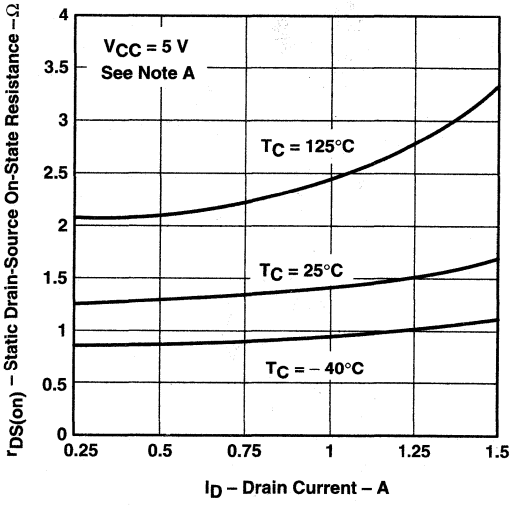


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

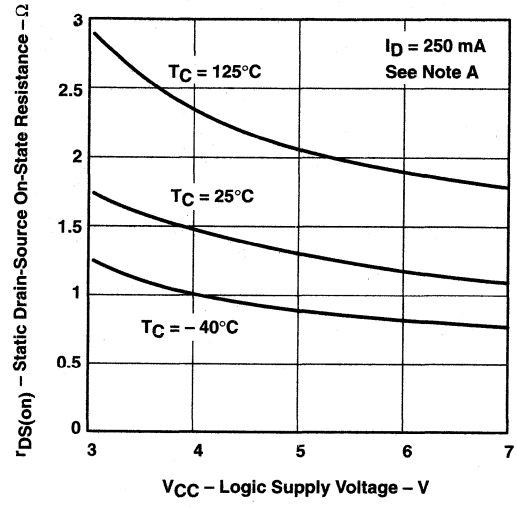


Figure 10

SWITCHING TIME vs FREE-AIR TEMPERATURE

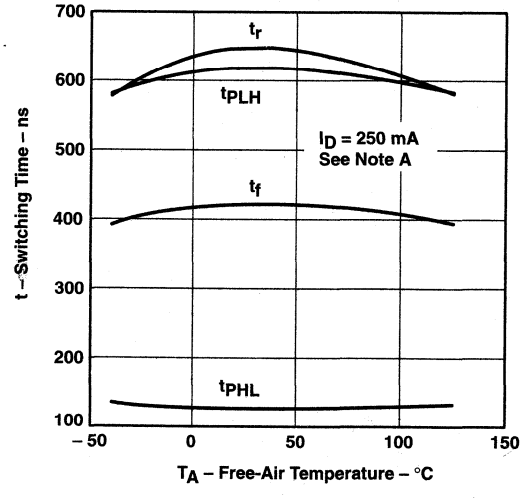
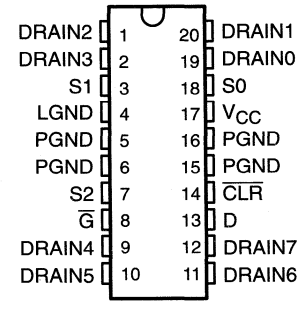


Figure 11

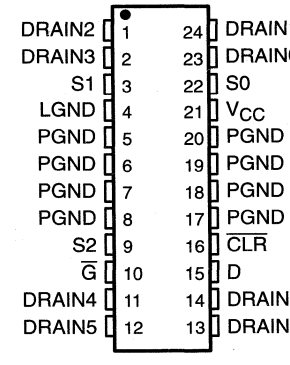
NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Four Distinct Function Modes**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 8-line demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

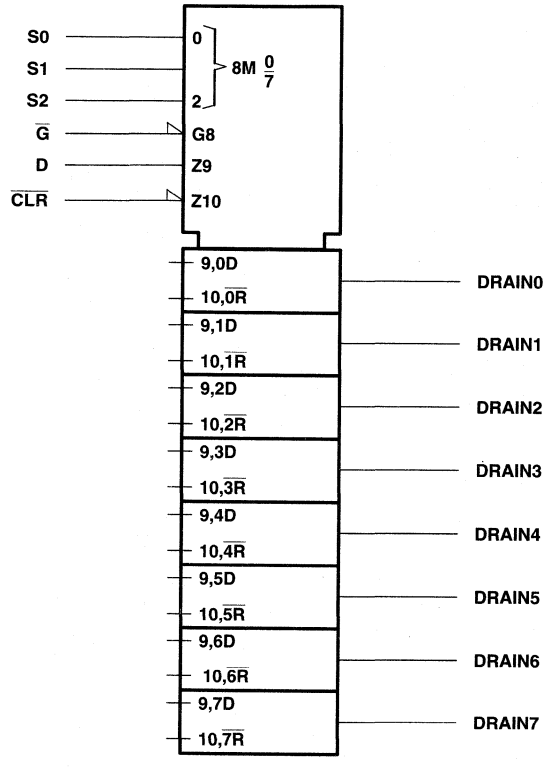
LATCH SELECTION TABLE

SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

description (continued)

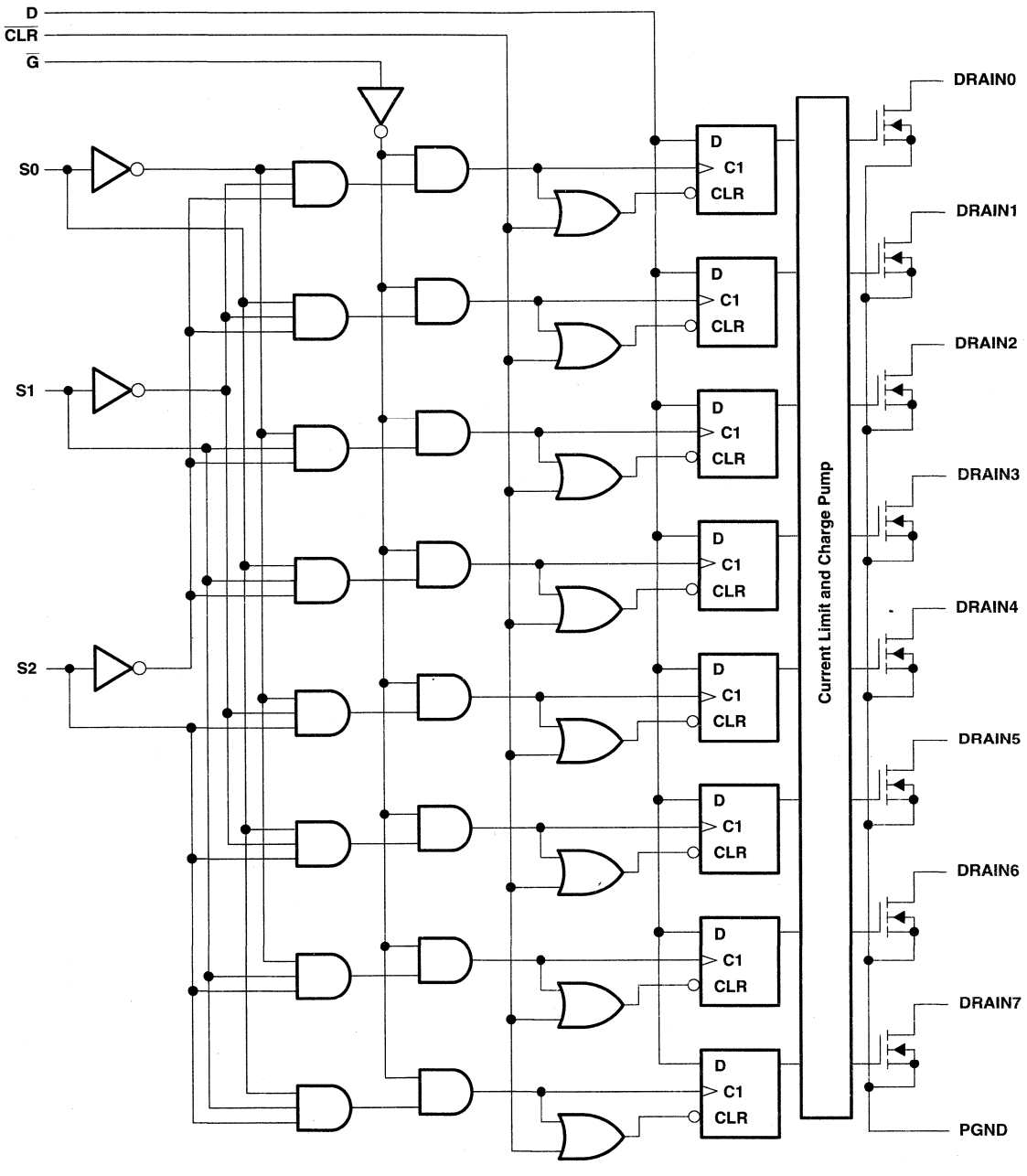
The TPIC6A259 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body, surface-mount (DW) package. The TPIC6A259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

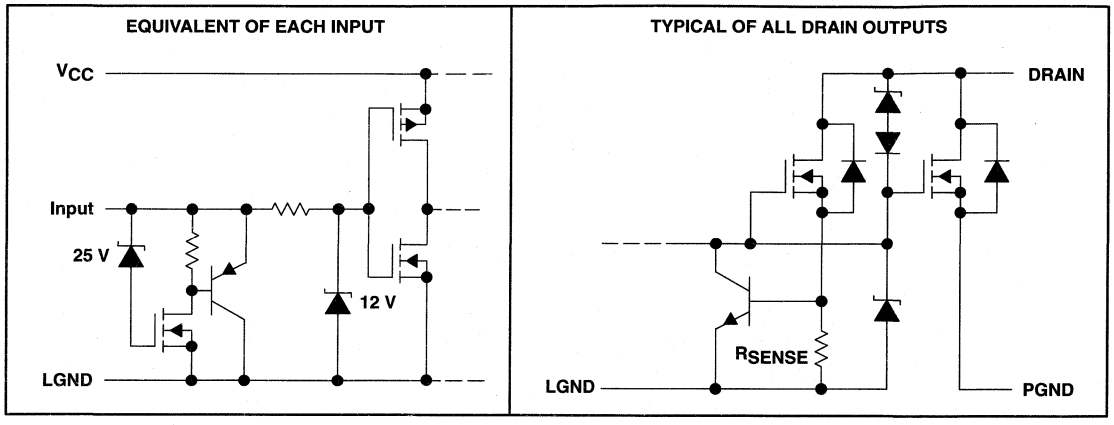


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	1 A
Pulsed source-to-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	350 mA
Peak drain current single output, T_C = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 μs, and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, and I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	0.6	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high before $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 350 mA,	See Note 3			0.8	1.1	V
I_{IH}	High-level input current	$V_I = V_{CC}$					1	µA
I_{IL}	Low-level input current	V_I = 0					−1	µA
I_{CC}	Logic supply current	I_O = 0,	$V_I = V_{CC}$ or 0			0.5	5	mA
I_{OK}	Output current at which chopping starts	T_C = 25°C,	See Note 5 and Figures 3 and 4		0.6	0.8	1.1	A
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_{(nom)} = I_D$, See Notes 5, 6, and 7	T_C = 85°C,		350		mA
I_D	Off-state drain current	V_{DS} = 40 V,	T_C = 25°C			0.1	1	µA
		V_{DS} = 40 V,	T_C = 125°C			0.2	5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 350 mA,	T_C = 25°C	See Notes 5 and 6 and Figures 9 and 10		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C			1.7	2.5	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output from D	C_L = 30 pF, See Figures 1, 2, and 11	I_D = 350 mA,		30		ns
t_{PLH}	Propagation delay time, low- to high-level output from D				125		ns
t_r	Rise time, drain output				60		ns
t_f	Fall time, drain output				30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA, See Notes 5 and 6 and Figure 5	di/dt = 20 A/µs,		100		ns
t_{rr}	Reverse-recovery time				300		ns

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	DW	All eight outputs with equal power		10	°C/W
		NE			10	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		50	°C/W
		NE			50	

PARAMETER MEASUREMENT INFORMATION

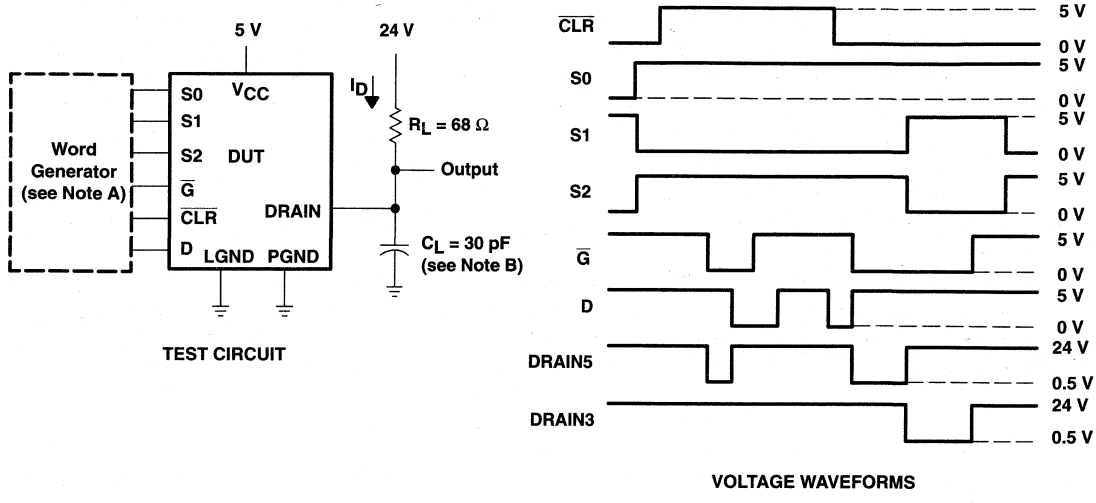


Figure 1. Typical Operation Mode

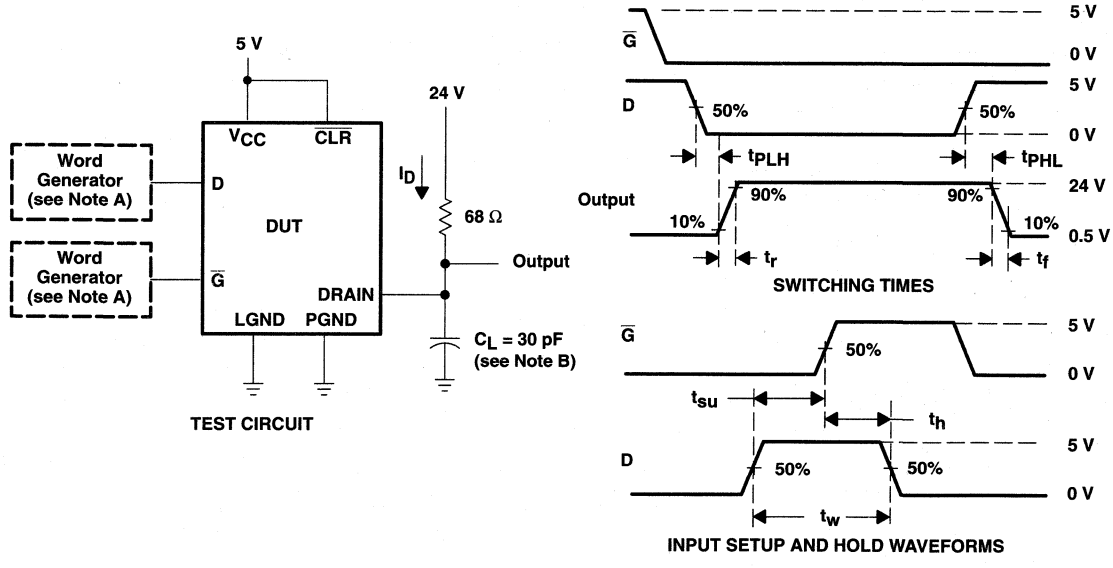
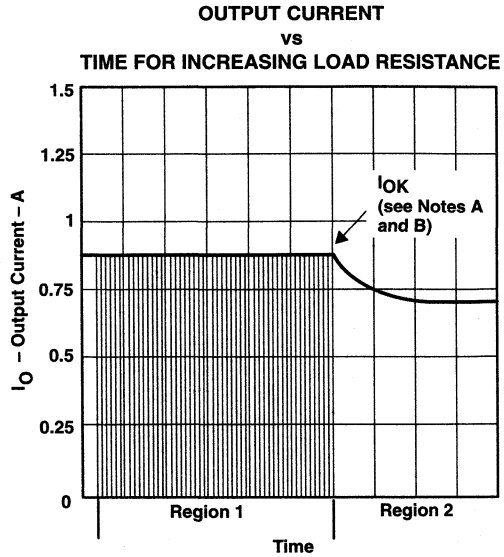
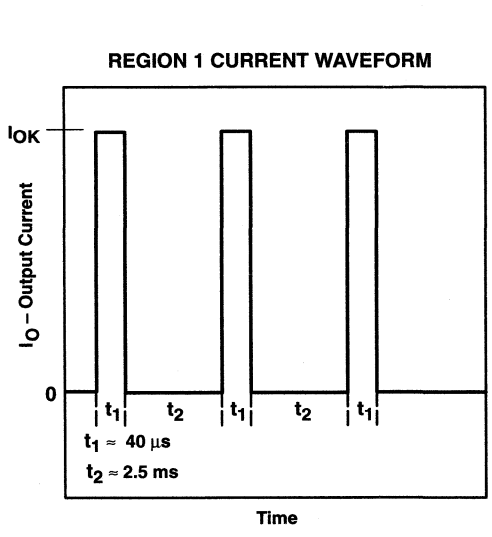


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION





First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

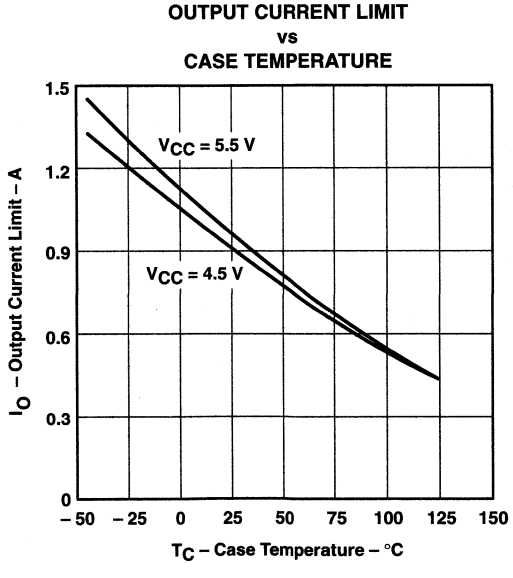
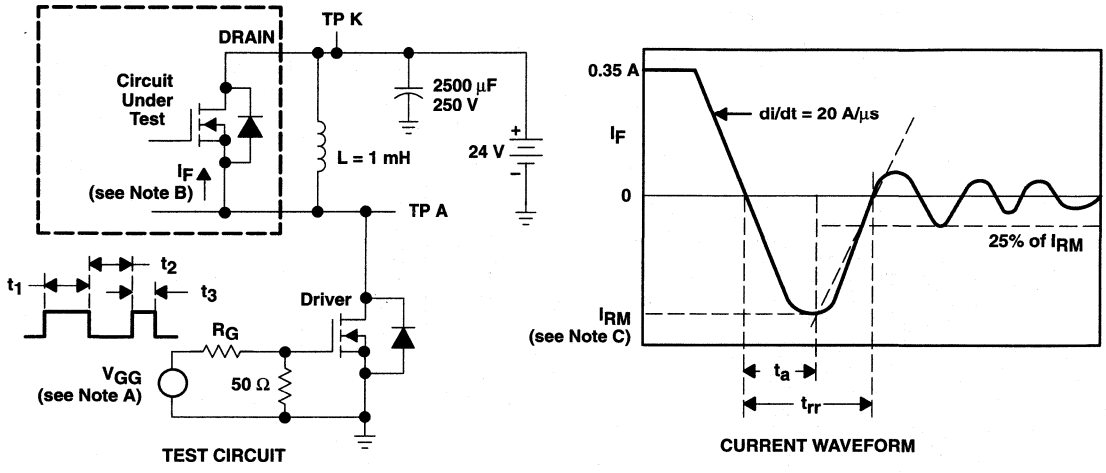


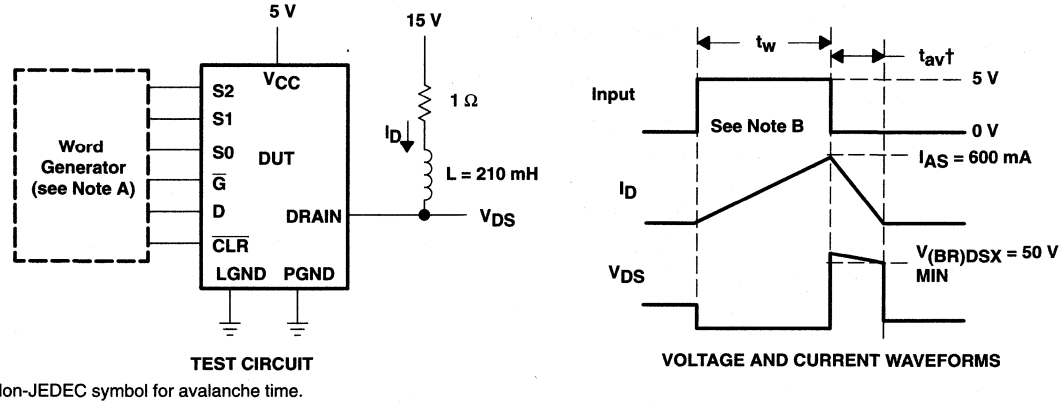
Figure 4

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

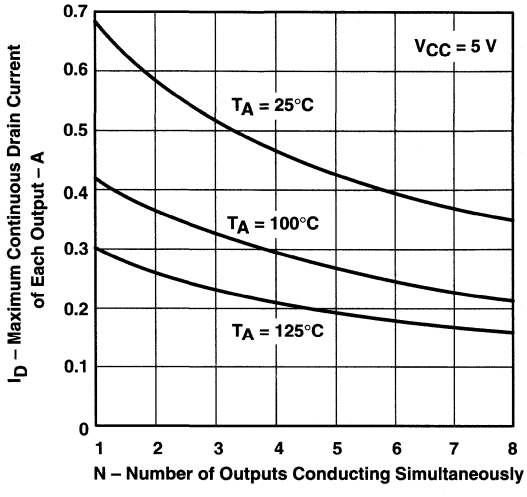


Figure 7

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

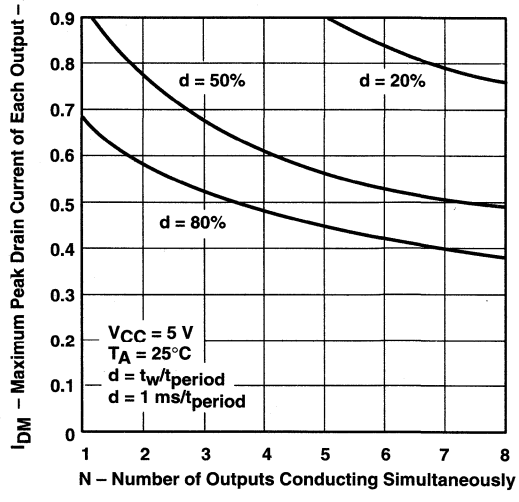


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

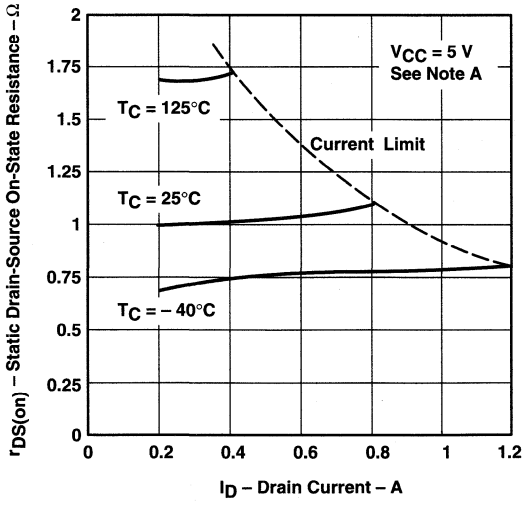


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

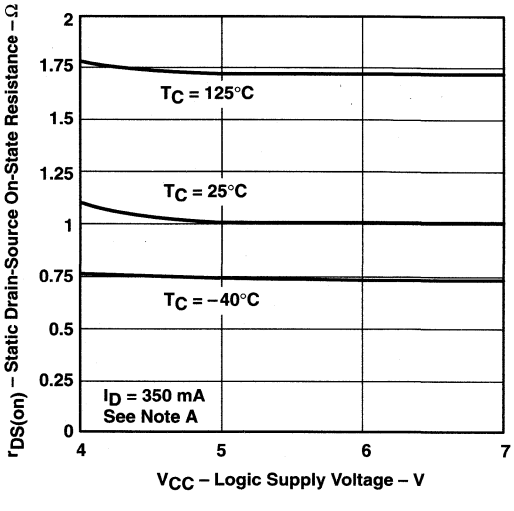
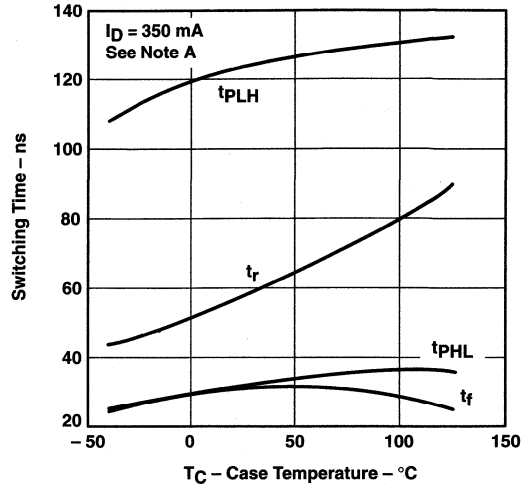


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

TYPICAL CHARACTERISTICS

SWITCHING TIME vs CASE TEMPERATURE

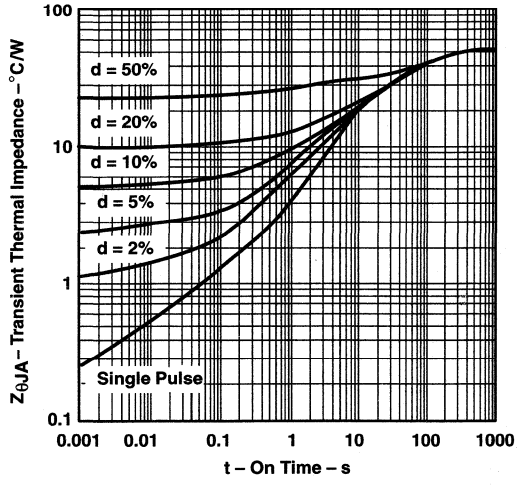


NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE vs ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_\theta(t_w + t_c) + Z_\theta(t_w) - Z_\theta(t_c)$$

Where:

$Z_\theta(t_w)$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_\theta(t_c)$ = the single-pulse thermal impedance for $t = t_c$ seconds

$Z_\theta(t_w + t_c)$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$d = t_w/t_c$

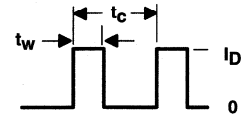
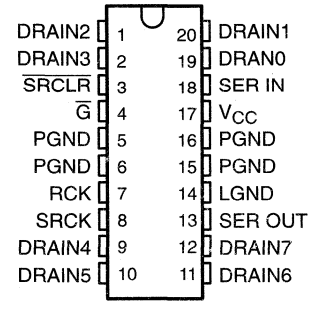


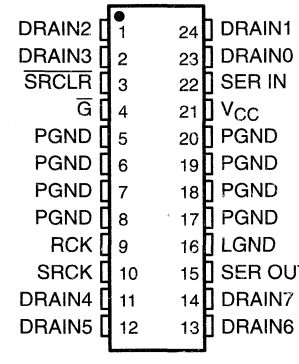
Figure 12

- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Devices Are Cascadable**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



description

The TPIC6A595 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

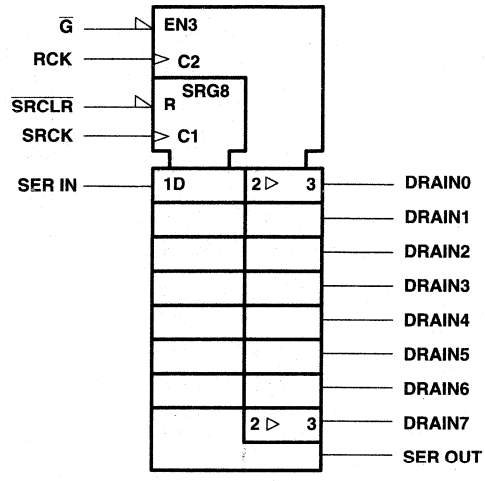
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and a 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

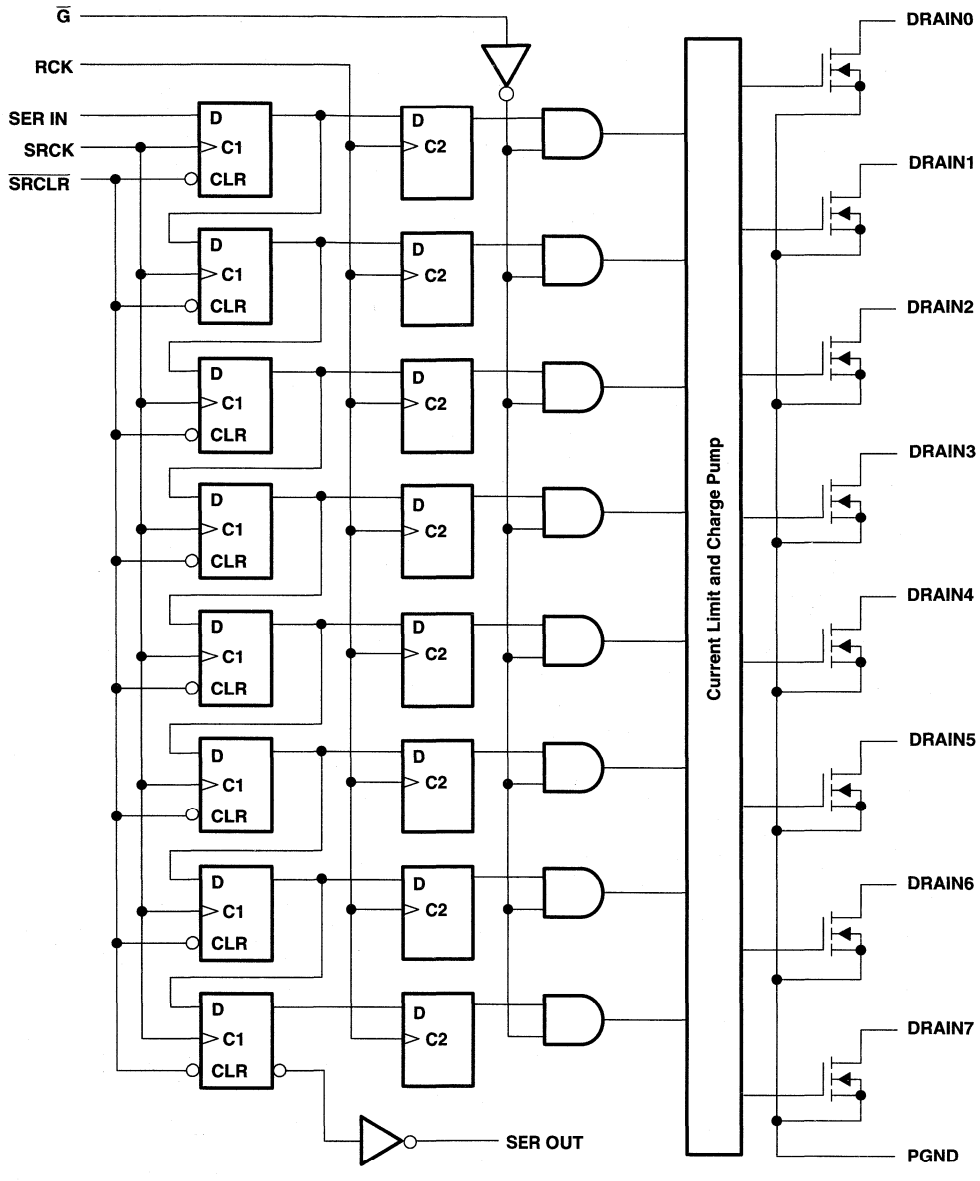
The TPIC6A595 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

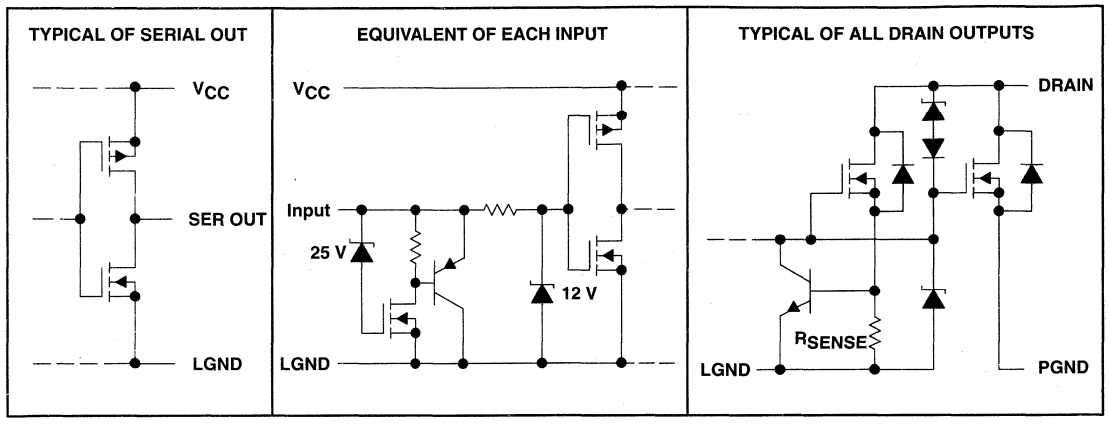


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	350 mA
Peak drain current, single output, T_A = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation	See Dissipation Rating Table
Operating case temperature range, T_C	−40°C to 125°C
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 μs and duty cycle ≤ 2 %.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	0.6	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 350 mA, See Note 3			0.8	1.1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 µA		V_{CC}−0.1	V_{CC}		V
		I_{OH} = −4 mA		V_{CC}−0.5	V_{CC}−0.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA			0	0.1	V
		I_{OL} = 4 mA			0.2	0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_I = 0				−1	µA
$I_{O(chop)}$	Output current at which chopping starts	T_C = 25°C, See Note 5 and Figures 3 and 4		0.6	0.8	1.1	A
I_{CC}	Logic supply current	I_O = 0, $V_I = V_{CC}$ or 0			0.5	5	mA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, $V_I = V_{CC}$ or 0,	I_O = 0, V_{CC} = 5 V, C_L = 30 pF, See Figure 7		1.3		mA
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_{(nom)} = I_D$, T_C = 85°C, See Notes 5, 6, and 7		350		mA
I_D	Drain current, off-state	V_{DS} = 40 V,	T_C = 25°C		0.1	1	µA
		V_{DS} = 40 V,	T_C = 125°C		0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350 mA,	T_C = 25°C		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C		1.7	2.5	
		I_D = 350 mA,	T_C = 40°C				
		See Notes 5 and 6 and Figures 10 and 11					

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

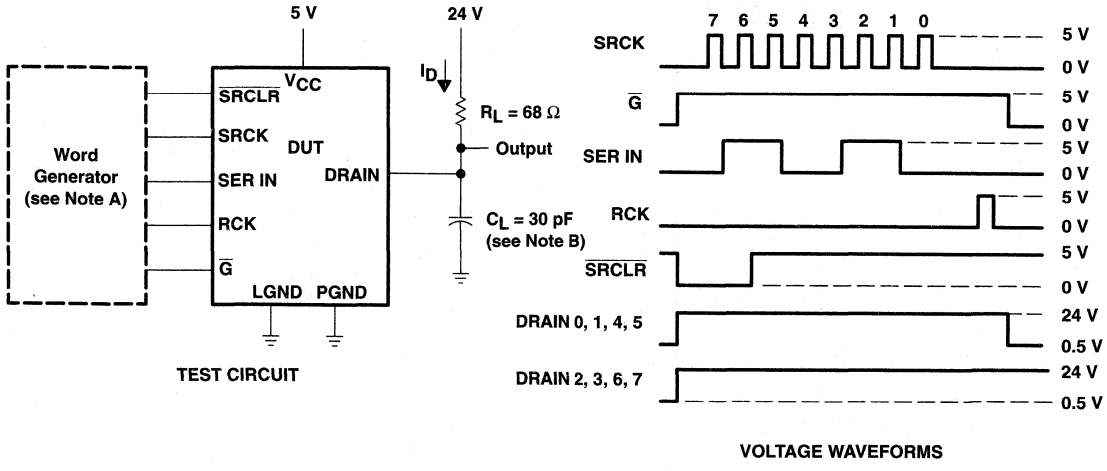
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$	C_L = 30 pF, I_D = 350 mA, See Figures 1, 2, and 12		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$			125		ns
t_r	Rise time, drain output			60		ns
t_f	Fall time, drain output			30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 5		100		ns
t_{rr}	Reverse-recovery time			300		ns

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

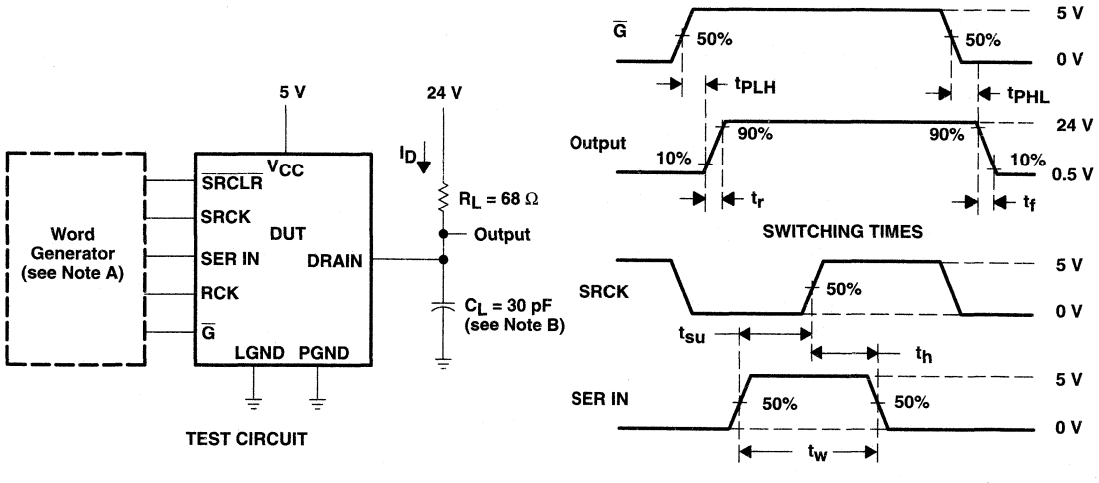
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	DW	All eight outputs with equal power		10	°C/W
		NE			10	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		50	°C/W
		NE			50	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

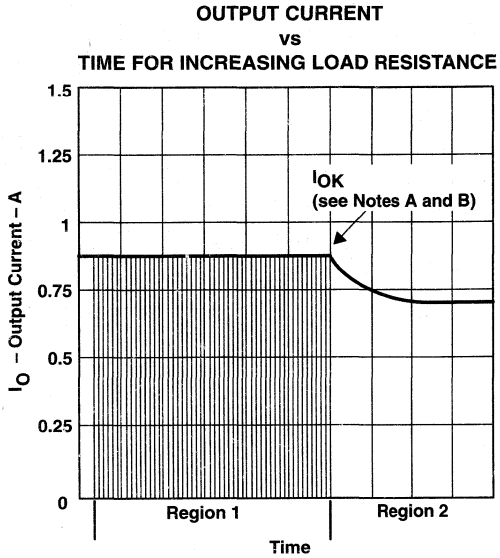
Figure 1. Resistive Load Operation

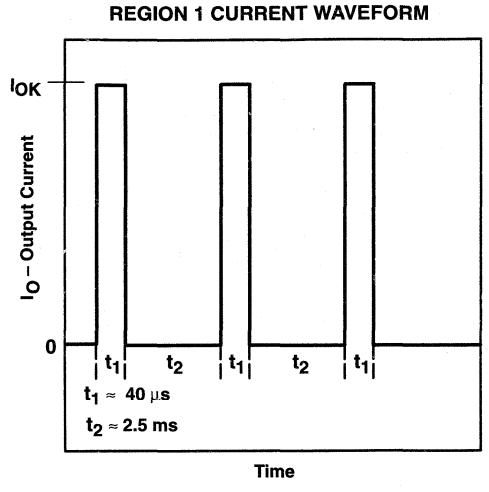


NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION





First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

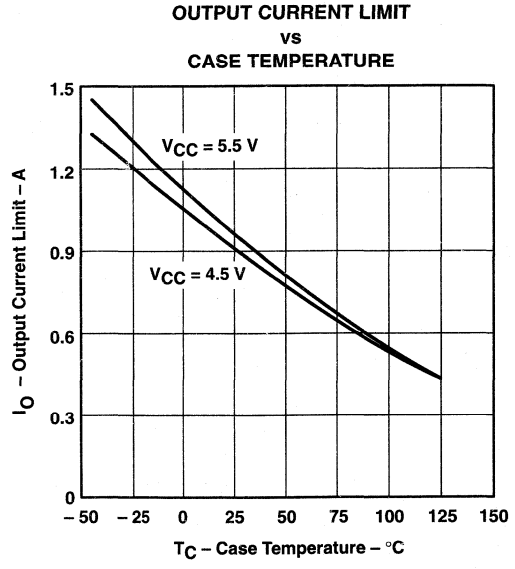


Figure 4

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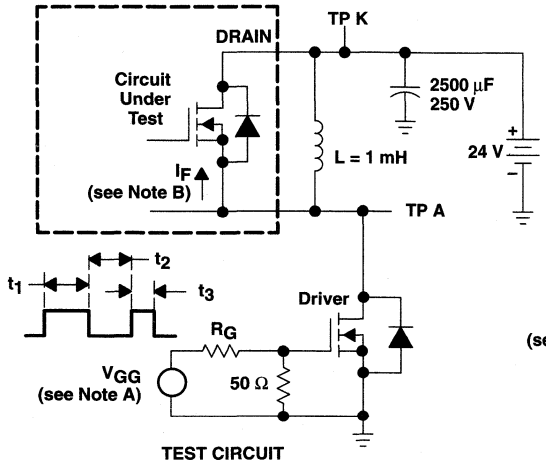
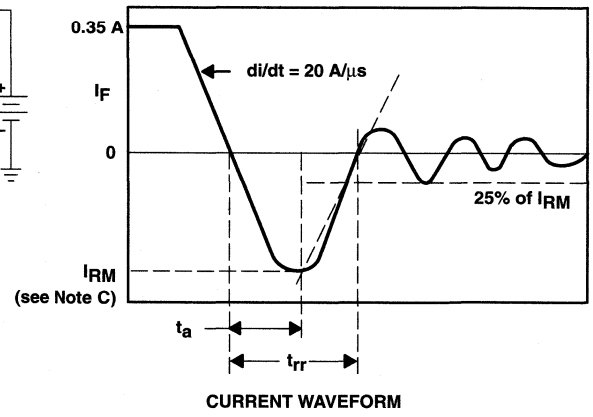
PARAMETER MEASUREMENT INFORMATION



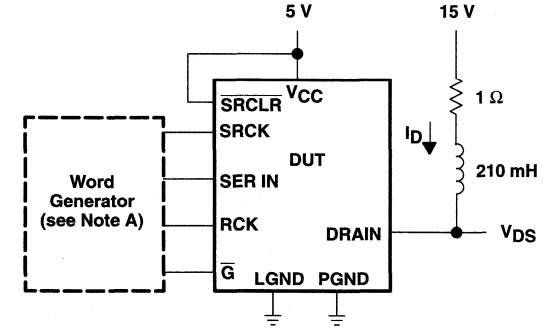
TEST CIRCUIT



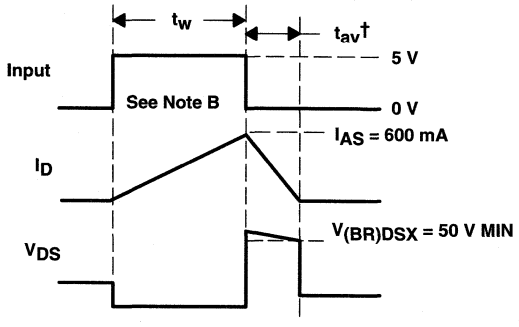
CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

† Non JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

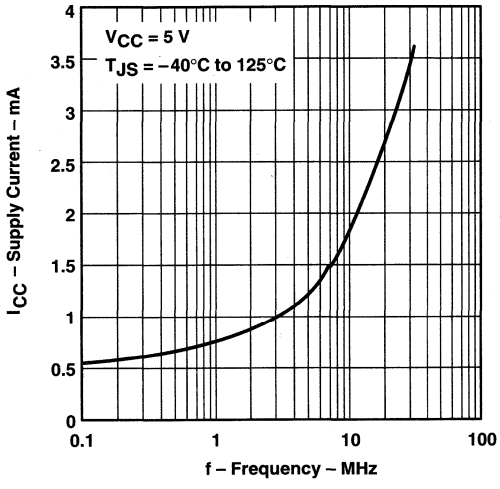


Figure 7

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

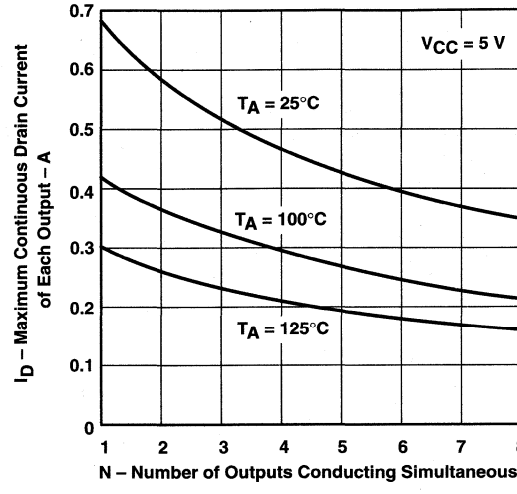


Figure 8

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

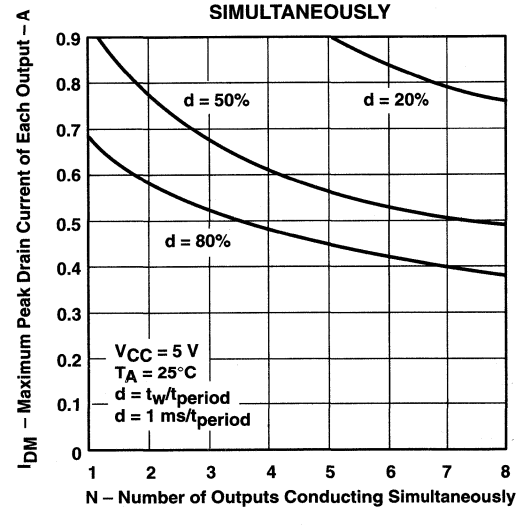
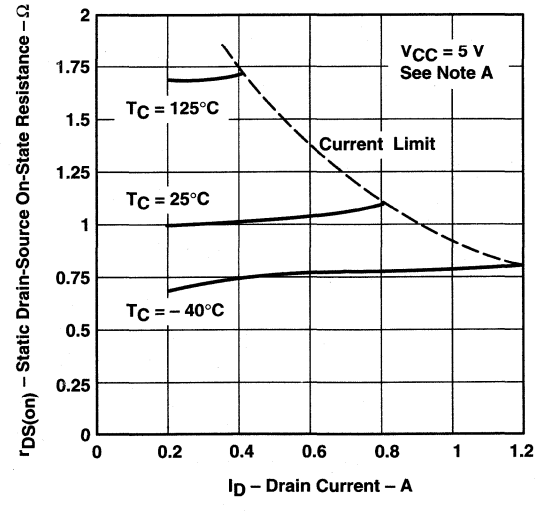


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT



NOTE A: Technique should limit T_J – T_C to 10°C maximum.

Figure 10

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

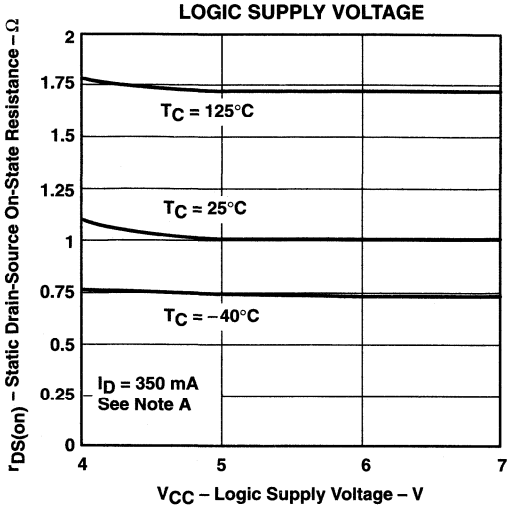


Figure 11

SWITCHING TIME vs CASE TEMPERATURE

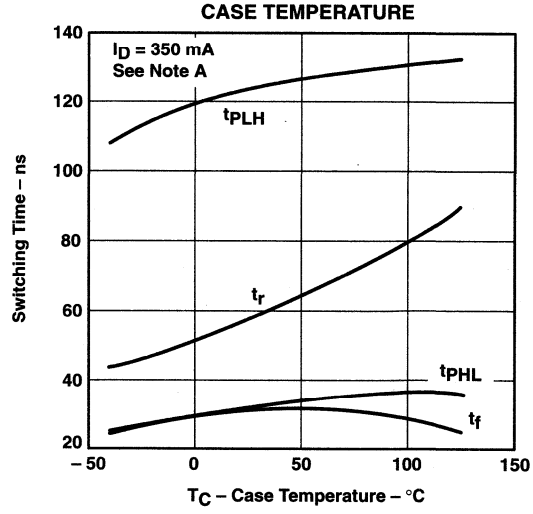
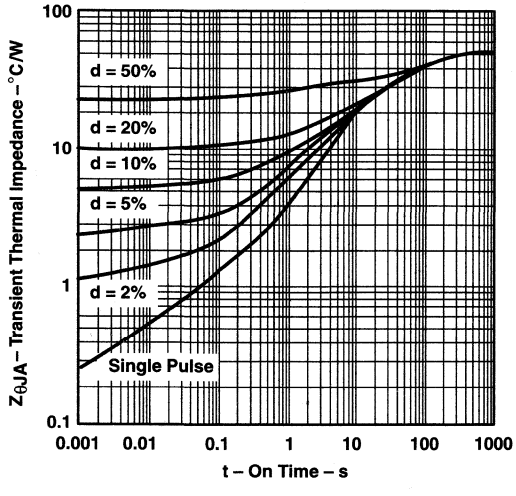


Figure 12

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE vs ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_\theta(t_w + t_c) + Z_\theta(t_w) - Z_\theta(t_c)$$

Where:

$Z_\theta(t_w)$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_\theta(t_c)$ = the single-pulse thermal impedance for $t = t_c$ seconds

$Z_\theta(t_w + t_c)$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$d = t_w/t_c$

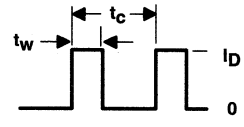
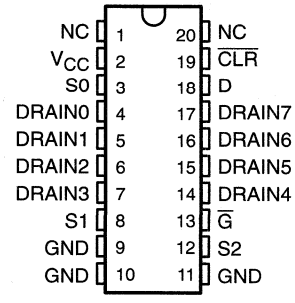


Figure 13

SLIS030 – APRIL 1994 – REVISED JULY 1995

- **Low $r_{DS(on)}$ . . . 5 Ω Typical**
- **Avalanche Energy . . . 30 mJ**
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- **500-mA Typical Current-Limiting Capability**
- **Output Clamp Voltage . . . 50 V**
- **Four Distinct Function Modes**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multi-functional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

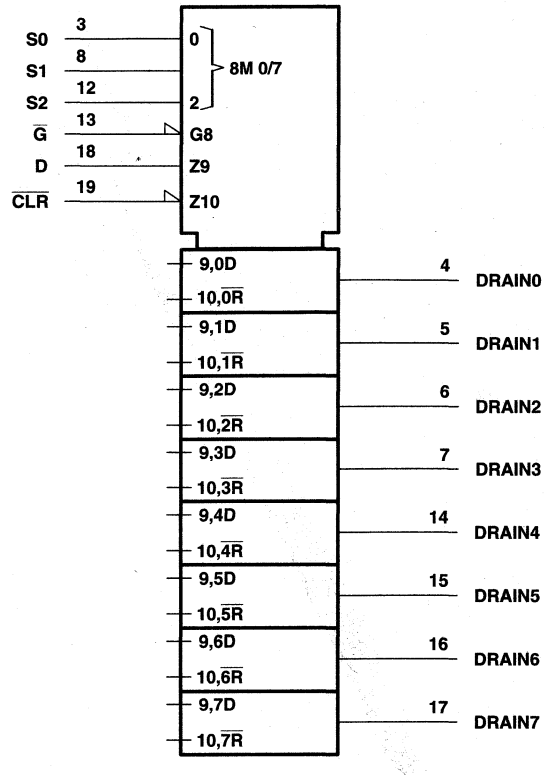
SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

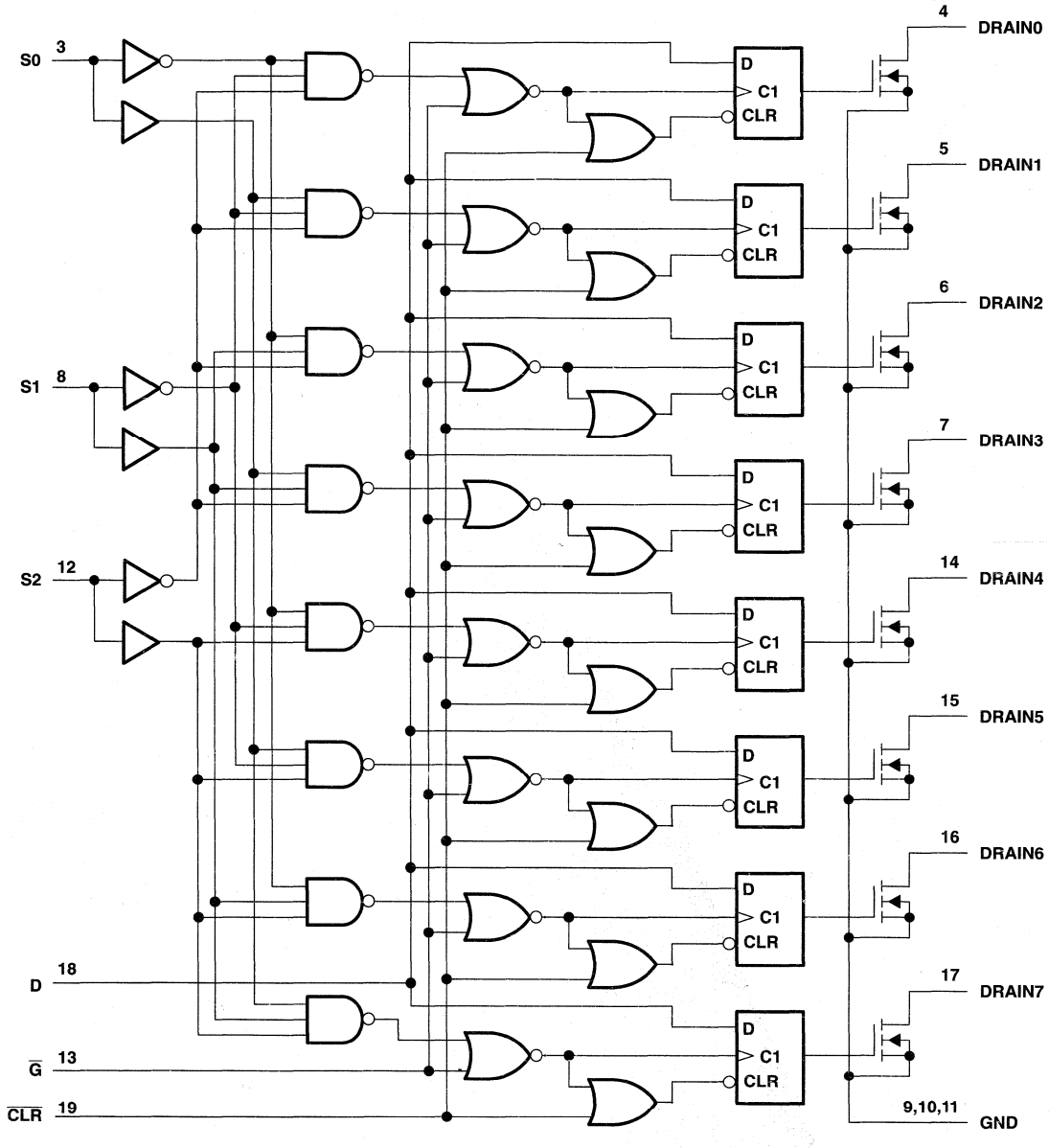
The TPIC6B259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

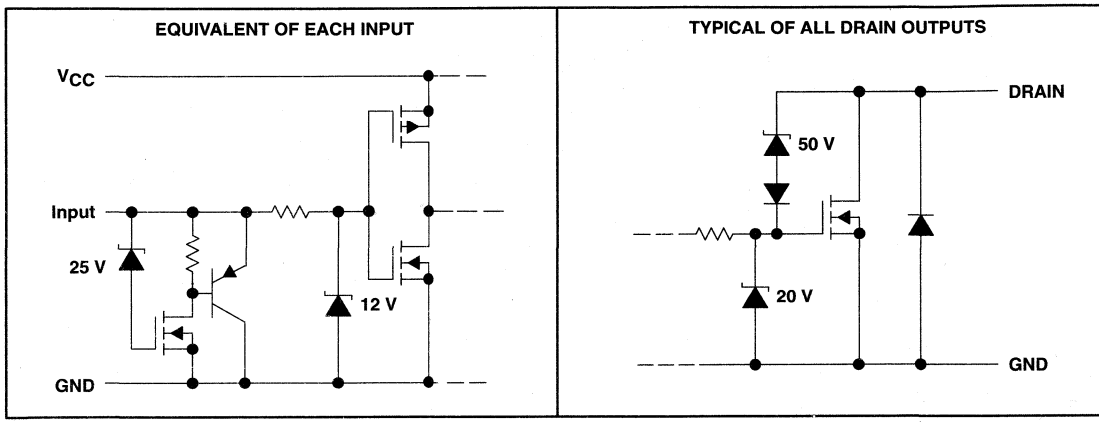


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM}, T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipating Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−500	500	mA
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	20		ns
Hold time, D high after $\overline{G}\uparrow$, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA				0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off			20	100	µA
			All outputs on			150	300	
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, See Notes 5, 6, and 7		T_C = 85°C,		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V,	V_{CC} = 5.5 V,	T_C = 125°C		0.15	8	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 100 mA,	V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 6 and 7		4.2	5.7	Ω
		I_D = 100 mA, T_C = 125°C	V_{CC} = 4.5 V,			6.8	9.5	
		I_D = 350 mA,	V_{CC} = 4.5 V			5.5	8	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

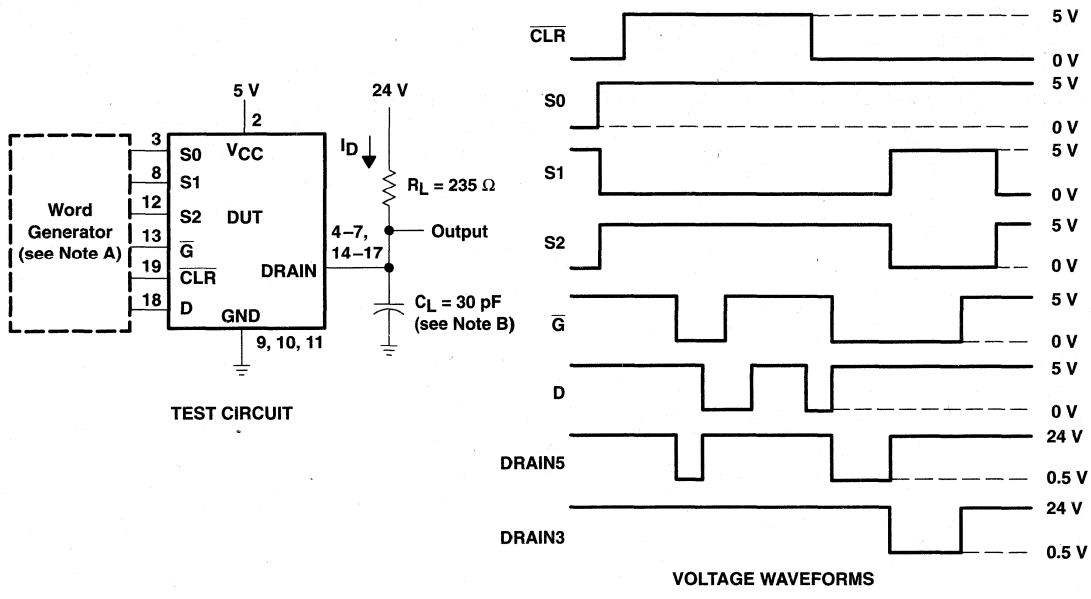
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from D	C_L = 30 pF, See Figures 1, 2, and 8	I_D = 100 mA,		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from D				90		ns
t_r	Rise time, drain output				200		ns
t_f	Fall time, drain output				200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, See Notes 5 and 6 and Figure 3	di/dt = 20 A/µs,		100		ns
t_{rr}	Reverse-recovery time				300		

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

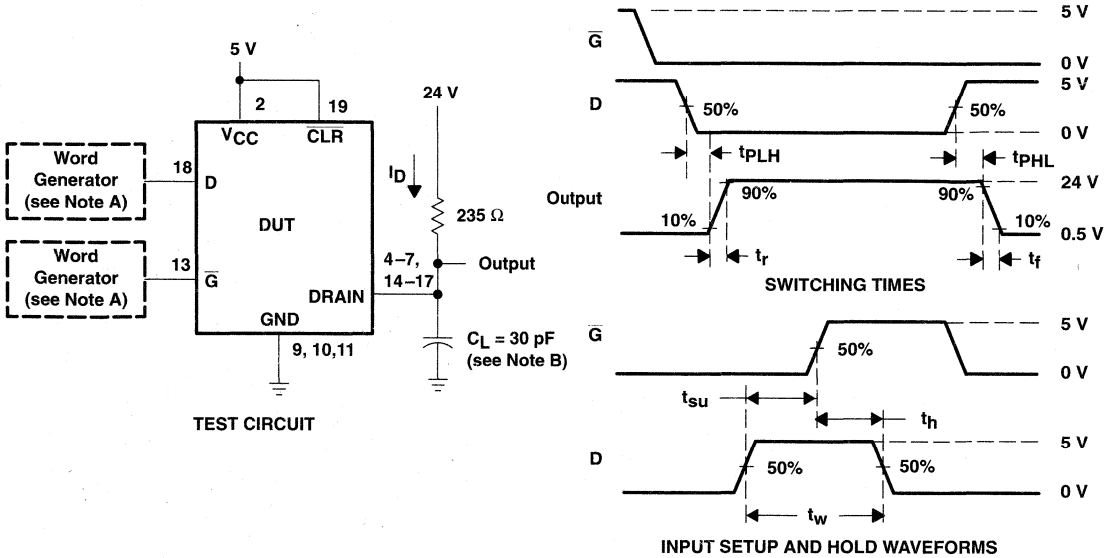
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

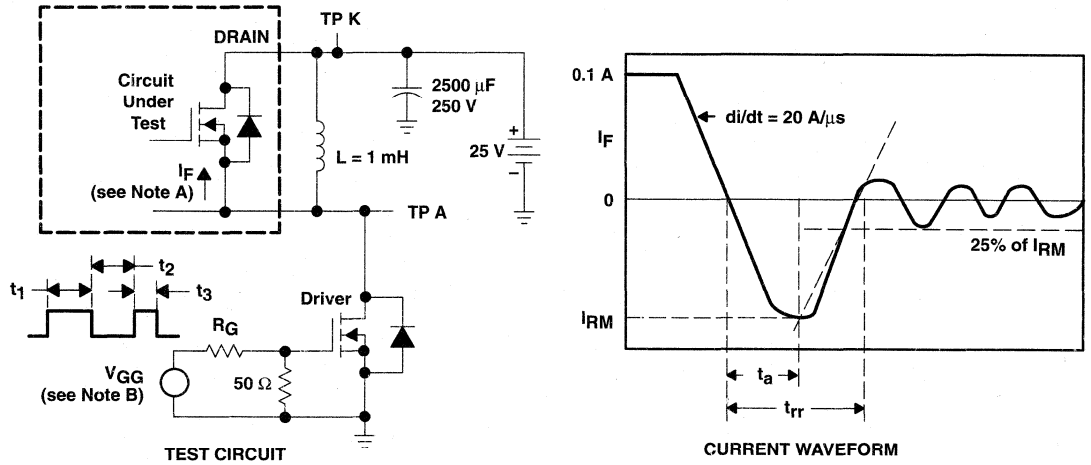
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

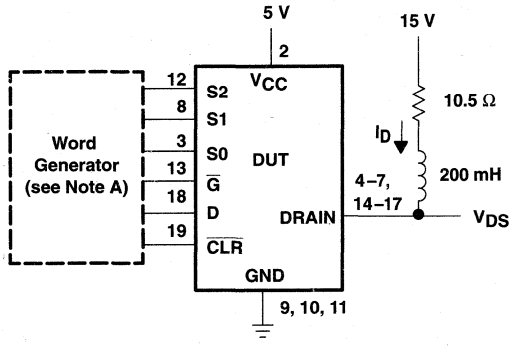
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



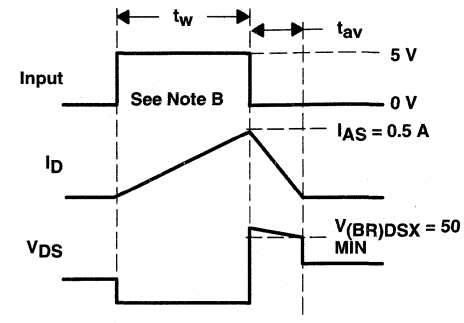
NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10$ µs, $t_2 = 7$ µs, and $t_3 = 3$ µs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current $I_{AS} = 0.5$ A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

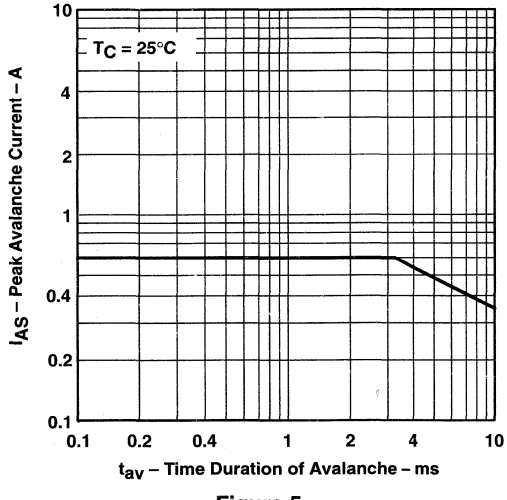
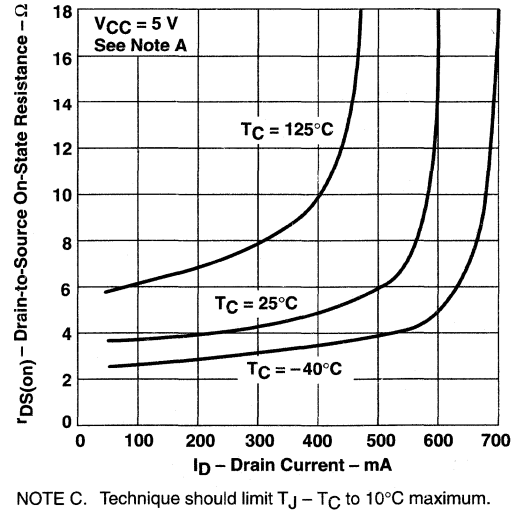


Figure 5

DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT



NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

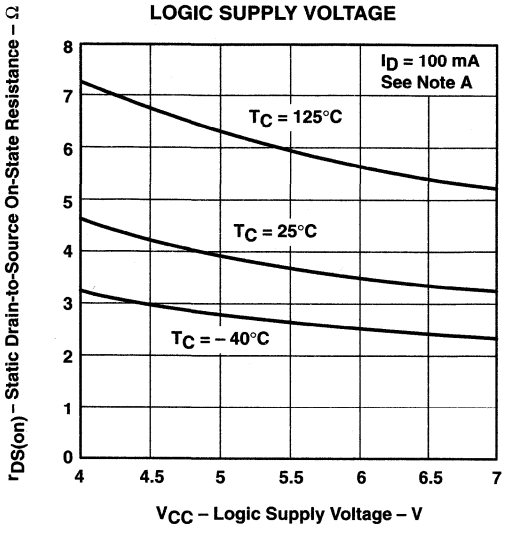


Figure 7

SWITCHING TIME vs CASE TEMPERATURE

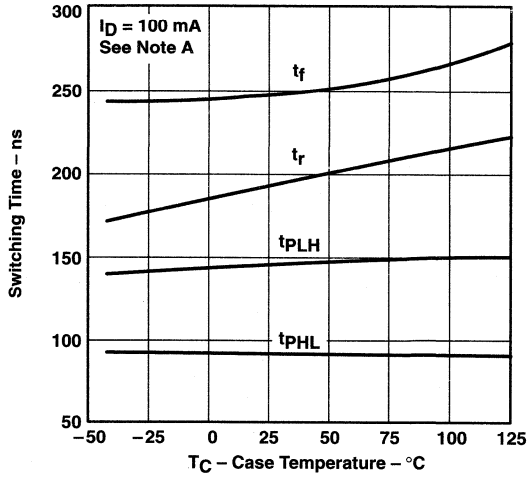


Figure 8

NOTE D. Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

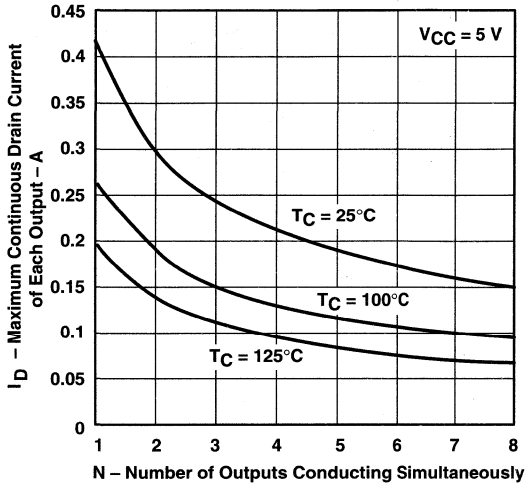


Figure 9

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

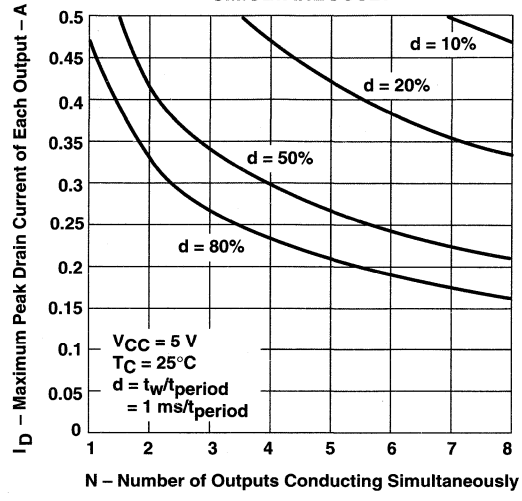
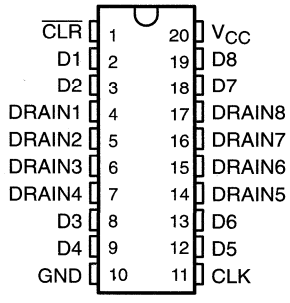


Figure 10

- **Low $r_{DS(on)}$ . . . 5 Ω Typical**
- **Avalanche Energy . . . 30 mJ**
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- **500-mA Typical Current-Limiting Capability**
- **Output Clamp Voltage . . . 50 V**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



description

The TPIC6B273 is a monolithic, high-voltage, medium-current, power logic octal D-type latch with DMOS-transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

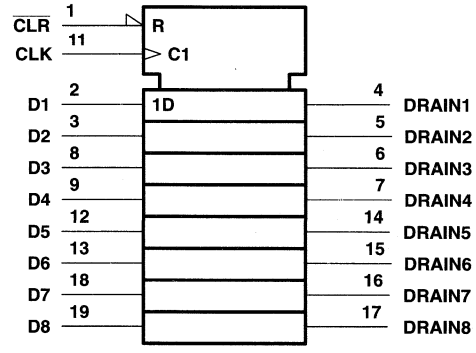
The TPIC6B273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS-transistor output.

When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all eight DMOS-transistor outputs off. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B273 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†



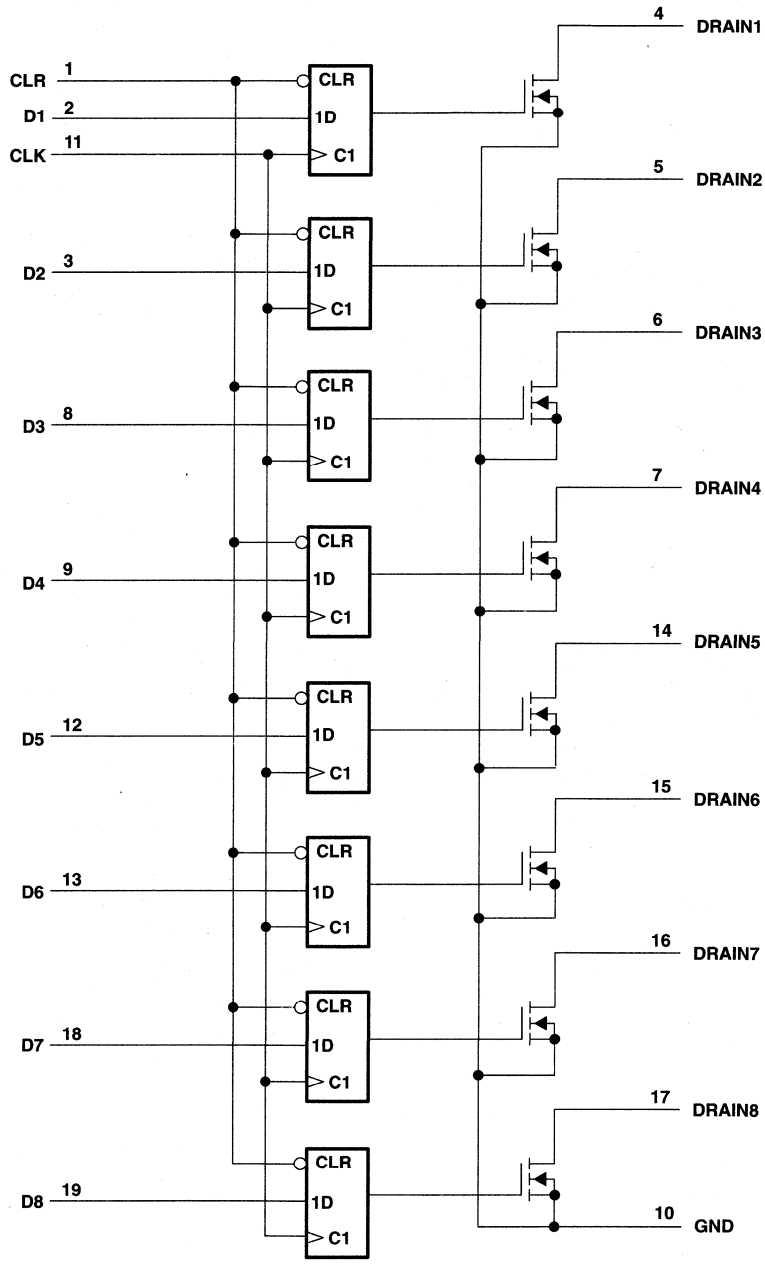
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each channel)

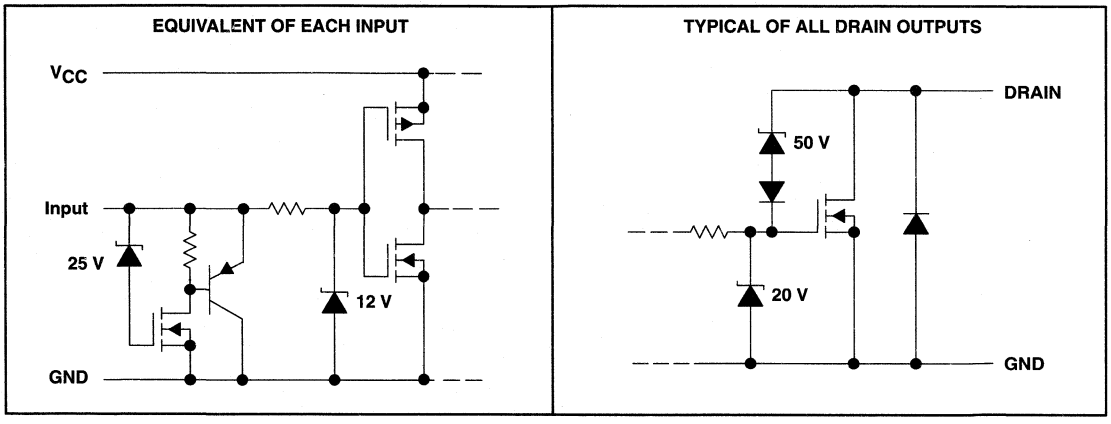
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	DRAIN
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM}, T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−500	500	mA
Setup time, D high before CLK↑, t_{su} (see Figure 2)	20		ns
Hold time, D high after CLK↑, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA				0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off			20	100	µA
			All outputs on			150	300	
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, See Notes 5, 6, and 7		T_C = 85°C,		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V,	V_{CC} = 5.5 V,	T_C = 125°C		0.15	8	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 100 mA,	V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 6 and 7		4.2	5.7	Ω
		I_D = 100 mA, T_C = 125°C	V_{CC} = 4.5 V,			6.8	9.5	
		I_D = 350 mA,	V_{CC} = 4.5 V			5.5	8	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, I_D = 100 mA, See Figures 1, 2, and 8		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK			90		ns
t_r	Rise time, drain output			200		ns
t_f	Fall time, drain output			200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

PARAMETER MEASUREMENT INFORMATION

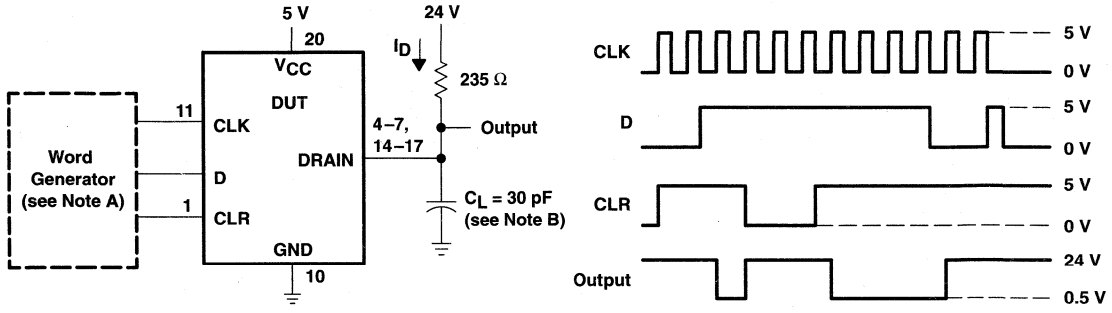


Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

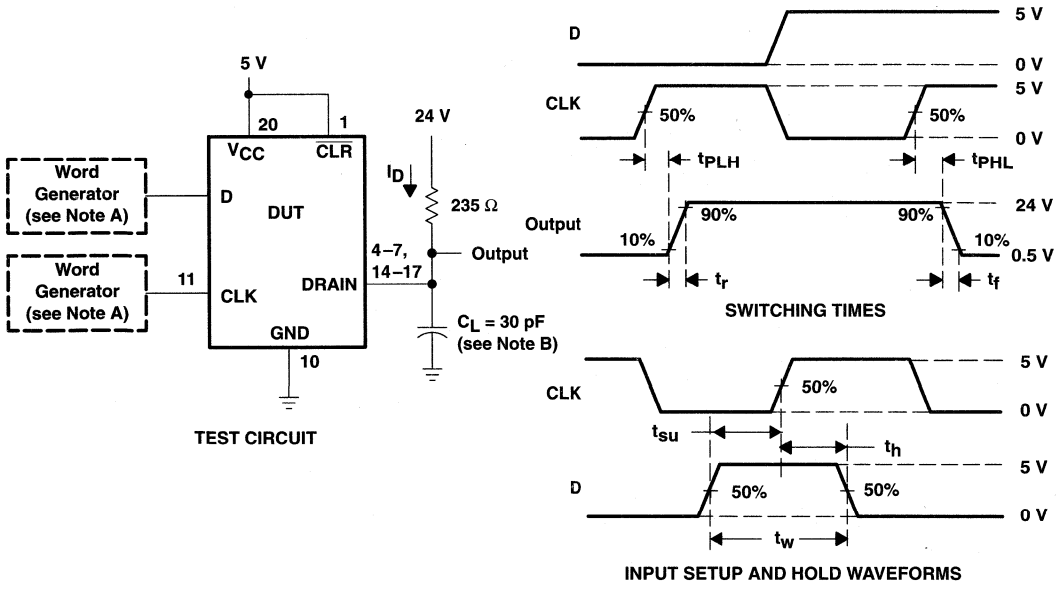
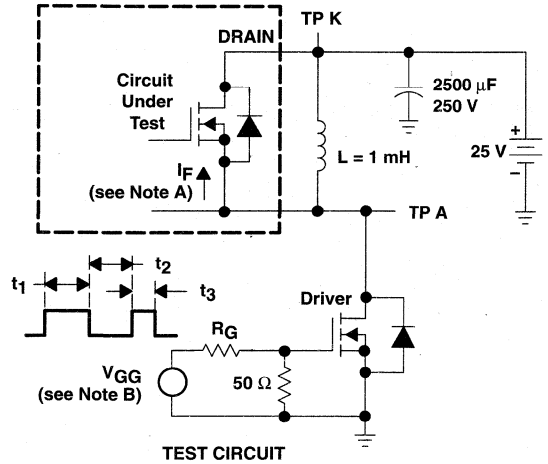


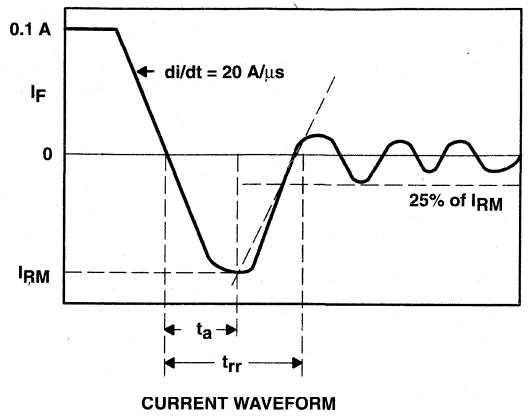
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 KHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



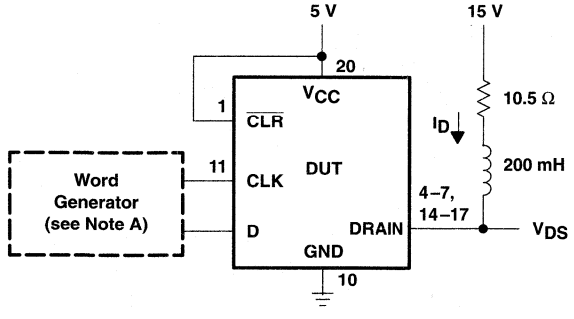
TEST CIRCUIT



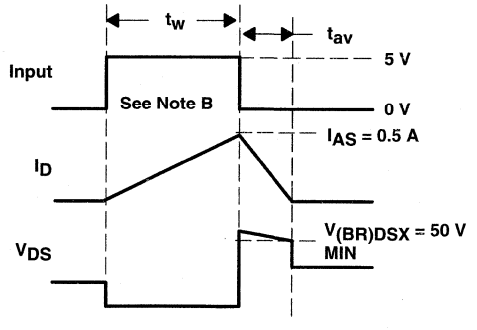
CURRENT WAVEFORM

NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.1 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 0.5 A.
Energy test is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 30 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

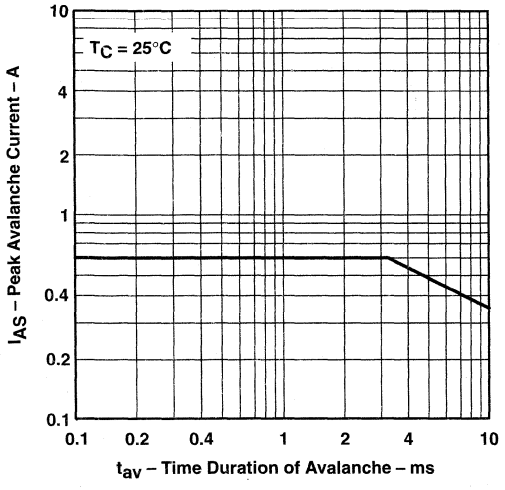


Figure 5

DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

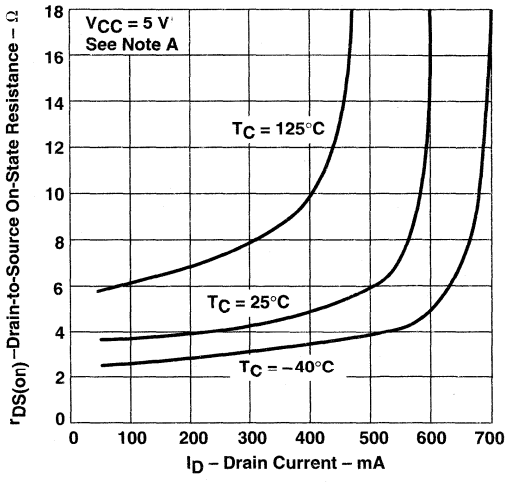


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
LOGIC SUPPLY VOLTAGE

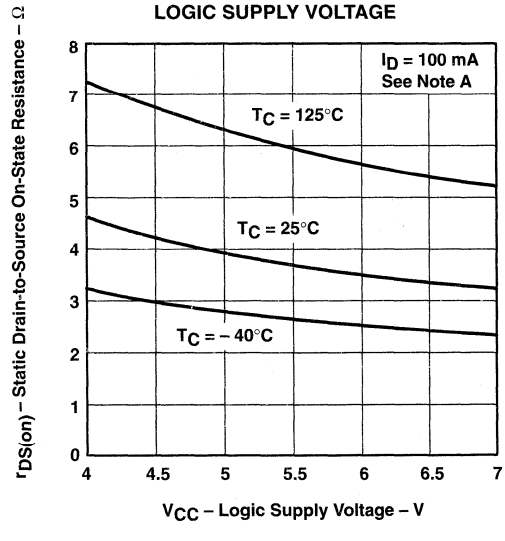


Figure 7

SWITCHING TIME
vs
CASE TEMPERATURE

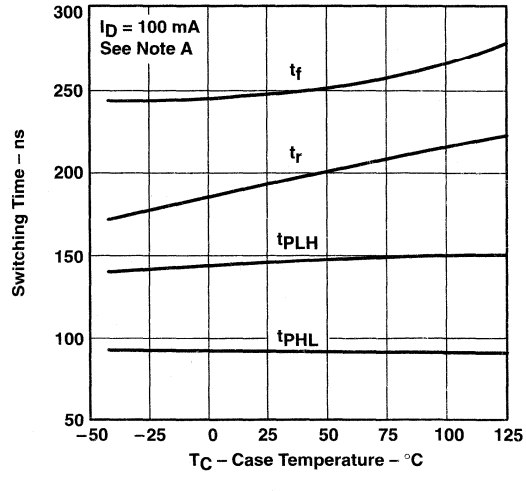


Figure 8

NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

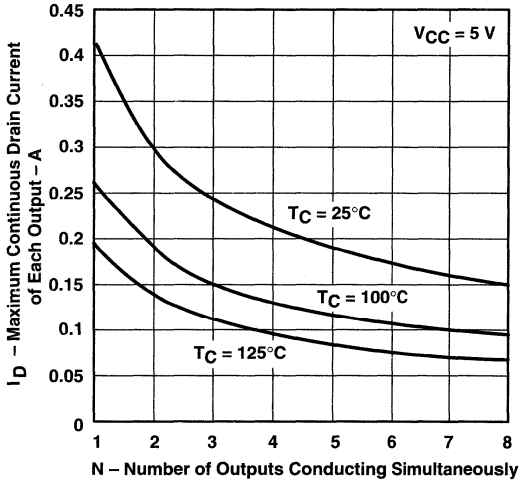


Figure 9

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

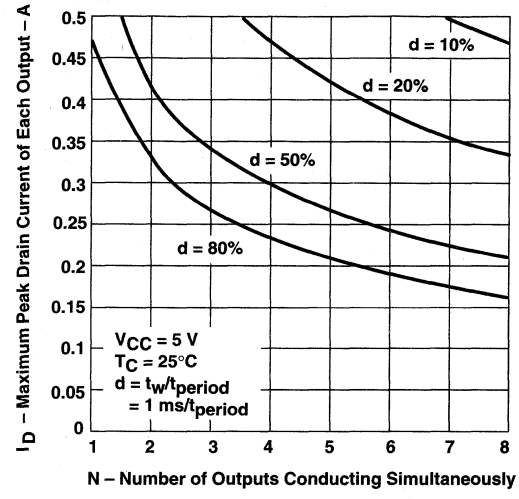
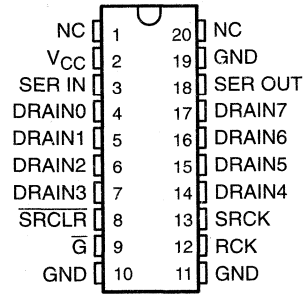


Figure 10

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Low $r_{DS(on)}$ . . . 5 Ω Typical**
- **Avalanche Energy . . . 30 mJ**
- **Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current**
- **500-mA Typical Current-Limiting Capability**
- **Output Clamp Voltage . . . 50 V**
- **Devices Are Cascadable**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



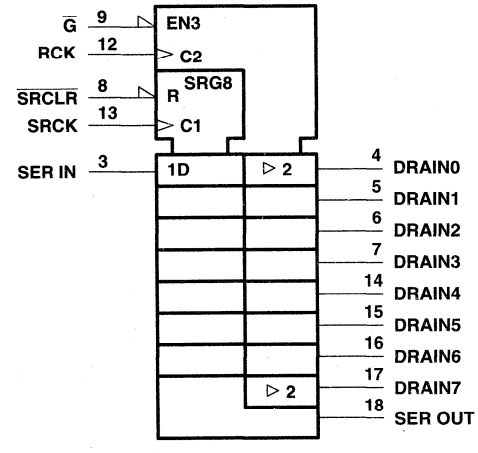
NC – No internal connection

description

The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†

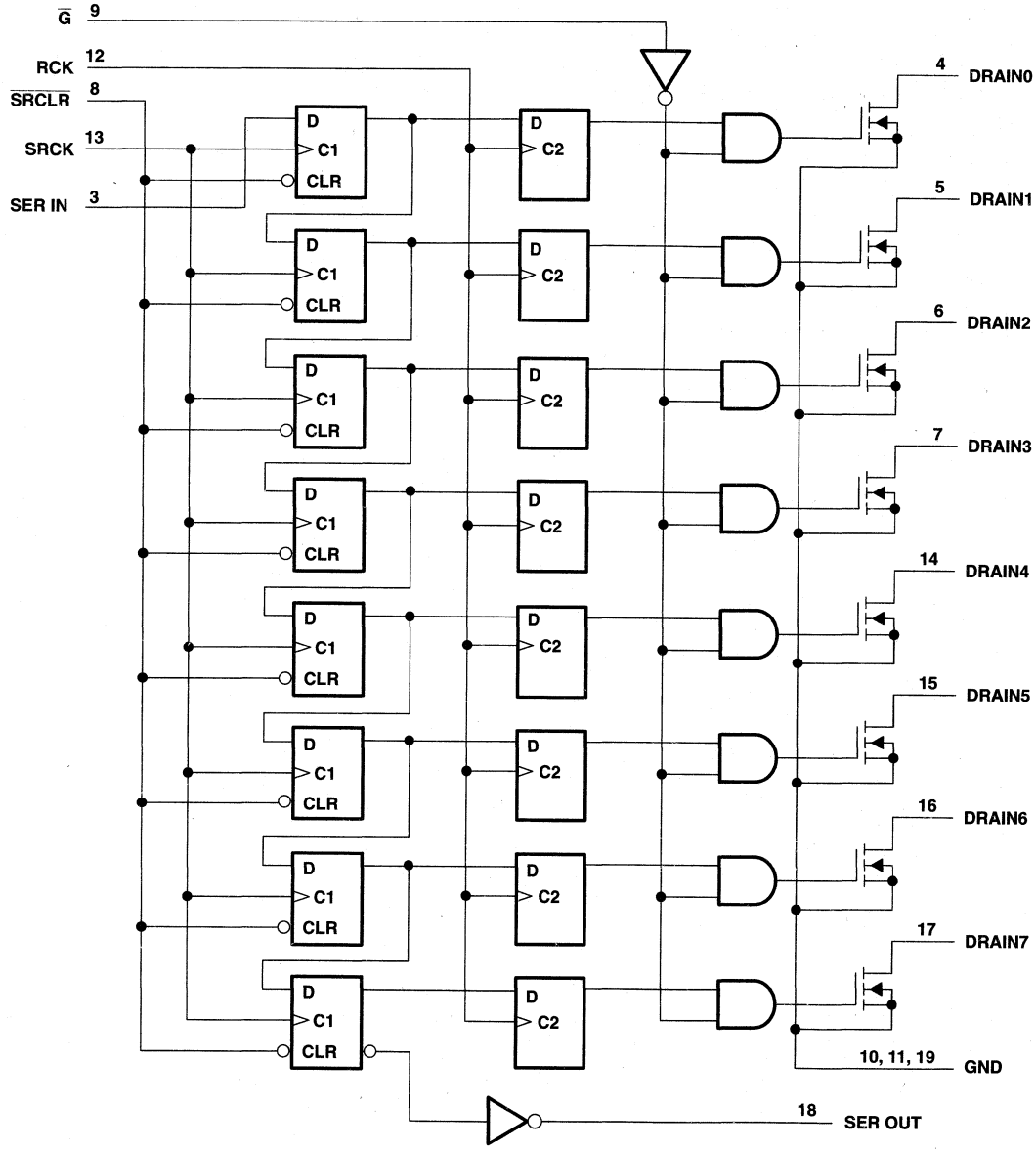


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25°C$. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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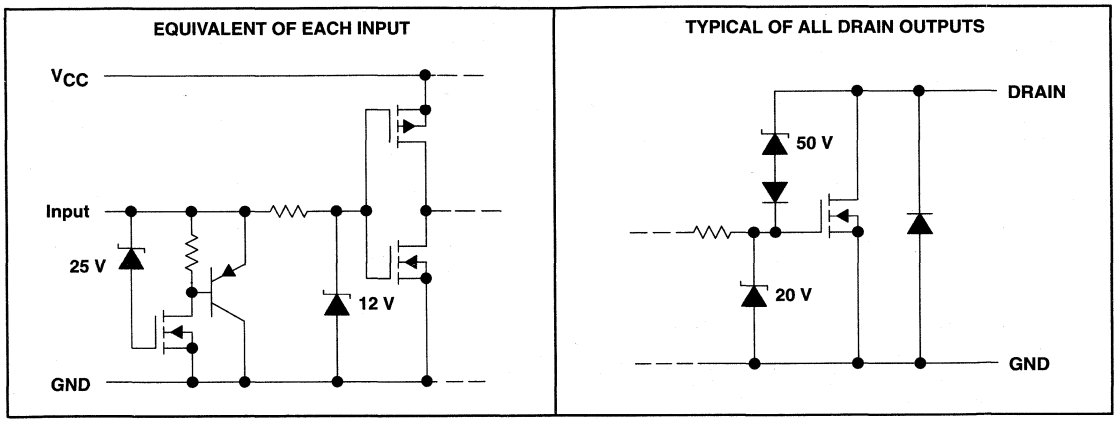
schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM}, T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−500	500	mA
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	20		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 µA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = −4 mA, V_{CC} = 4.5 V		4	4.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA, V_{CC} = 4.5 V			0.005	0.1	V
		I_{OL} = 4 mA, V_{CC} = 4.5 V			0.3	0.5	
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off		20	100	µA
			All outputs on		150	300	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, All outputs off,	See Figures 2 and 6		0.4	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V, V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V, V_{CC} = 5.5 V, T_C = 125°C			0.15	8	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 100 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 7 and 8		4.2	5.7	Ω
		I_D = 100 mA, V_{CC} = 4.5 V, T_C = 125°C			6.8	9.5	
		I_D = 350 mA, V_{CC} = 4.5 V			5.5	8	

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

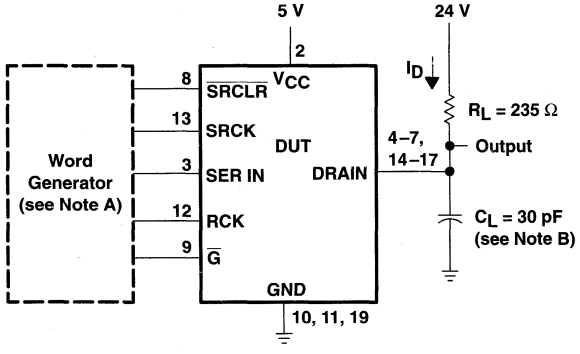
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 100 mA, See Figures 1, 2, and 9		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			90		ns
t_r	Rise time, drain output			200		ns
t_f	Fall time, drain output			200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

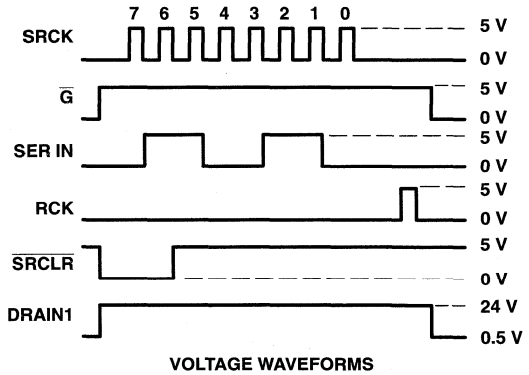
thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

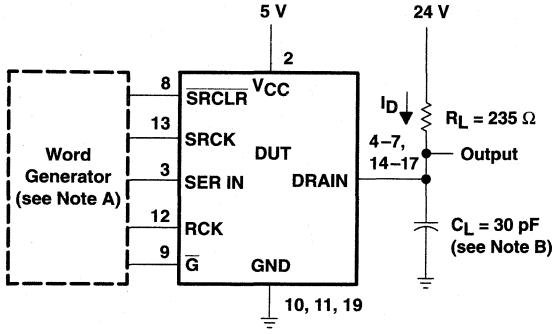


VOLTAGE WAVEFORMS

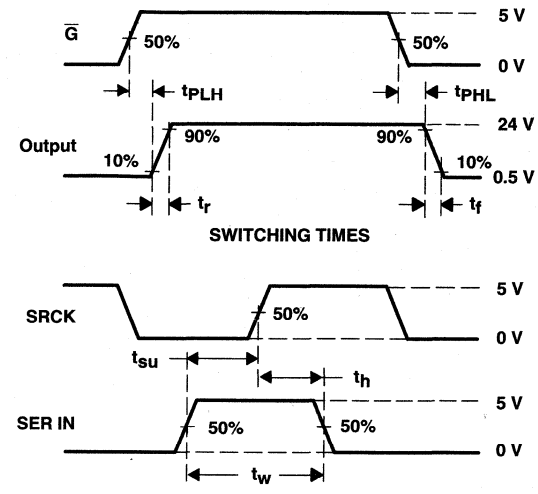
NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 300 ns, pulsed repetition rate (PRR) = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

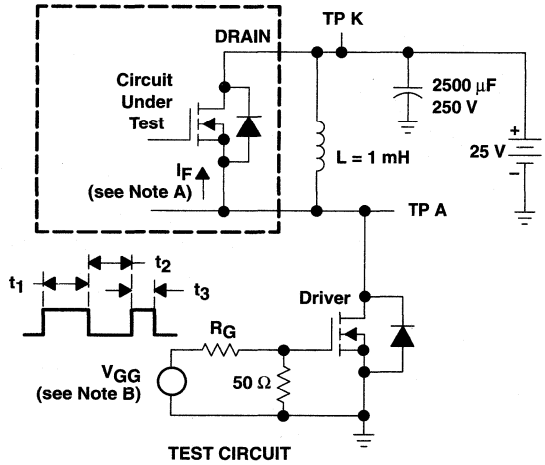


TEST CIRCUIT

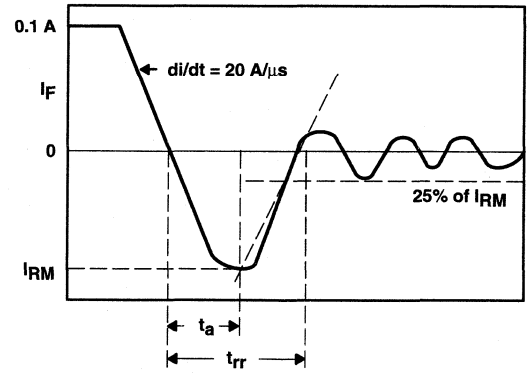


NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



TEST CIRCUIT



CURRENT WAVEFORM

NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10$ µs, $t_2 = 7$ µs, and $t_3 = 3$ µs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

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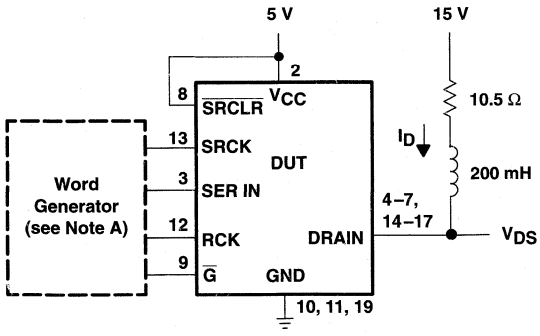
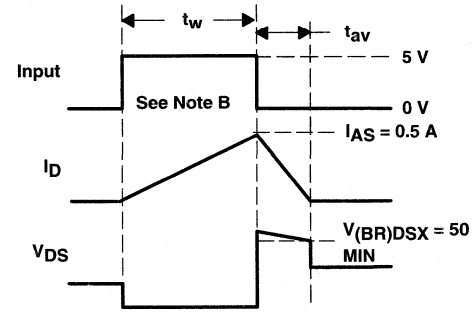
PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current $I_{AS} = 0.5$ A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

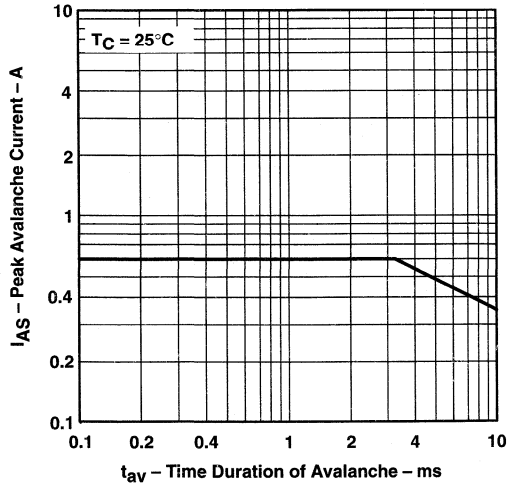


Figure 5

SUPPLY CURRENT
vs
FREQUENCY

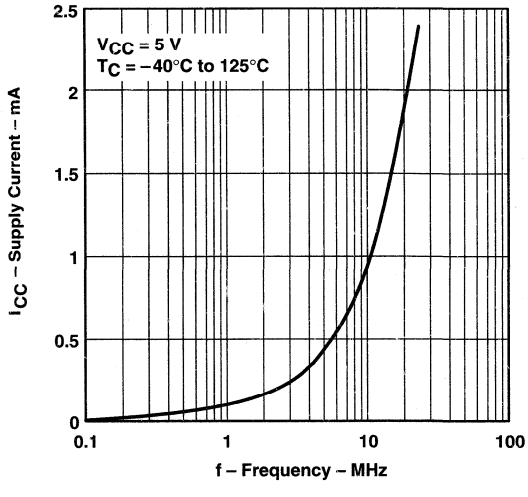


Figure 6

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

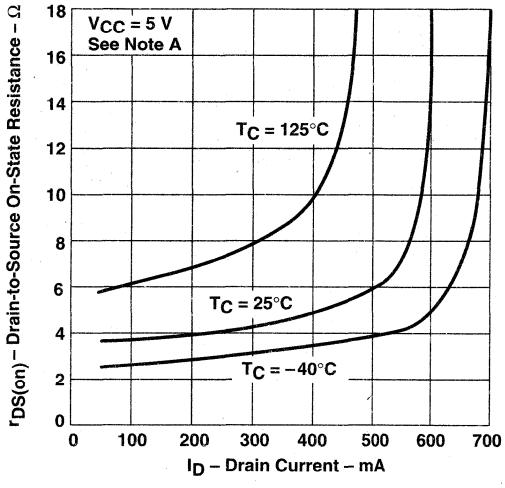


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
LOGIC SUPPLY VOLTAGE

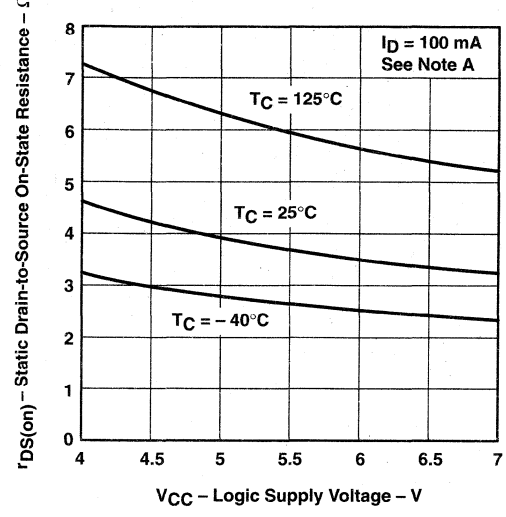


Figure 8

SWITCHING TIME
vs
CASE TEMPERATURE

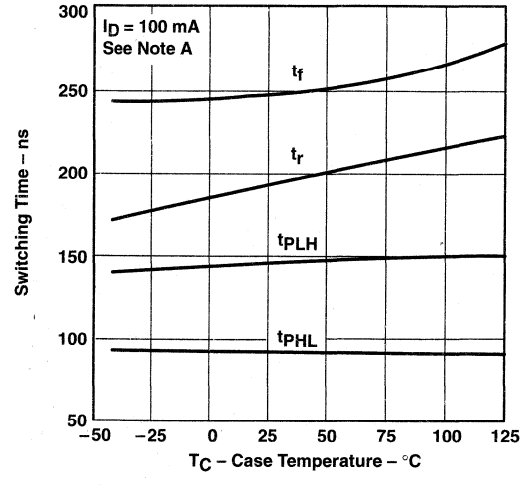


Figure 9

NOTE C. Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

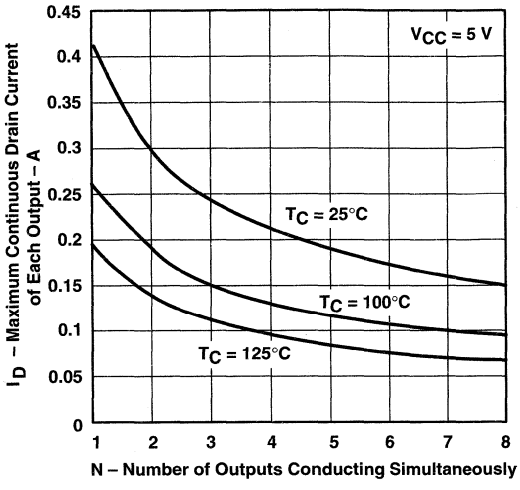


Figure 10

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

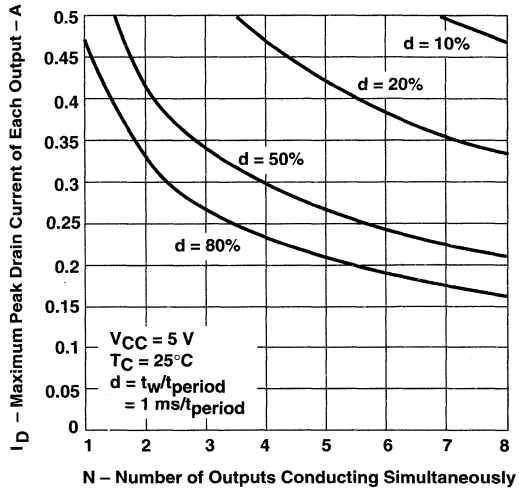
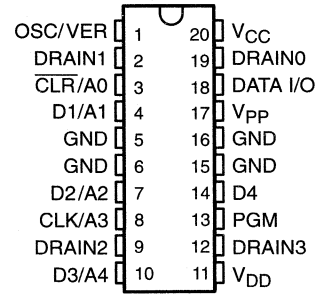


Figure 11

- **Programmable-PWM Current Threshold**
- **Programmable-PWM Frequency Controlled by Internal or External Oscillator**
- **Integrated Output Recirculation Clamp Diodes**
- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Four Power MOSFET Outputs**
- **Integrated Snubbing Clamp Voltage at 40 V**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



description

The power logic quad D-type latch pulse-width-modulation (PWM) driver controls open-drain DMOS transistor outputs and is designed for applications that require relatively high power. The device contains a built-in snubbing clamp and recirculation clamp on the outputs for inductive transient protection and inductive energy recirculation respectively. Power driver applications include solenoids and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent user-programmable PWM circuit that works in conjunction with the recirculation clamping diode in order to control the average current in inductive-load applications. The PWM circuit provides a programmable current-limit threshold that disables the output until the next rising edge of the independent PWM programmable clock. Each clock is generated from a user-programmable internal or external clock reference that in turn is programmed independently for each output through a frequency divide-by circuit.

TERMINAL NOMENCLATURE	
OSC/VER	Oscillator/Verify
DRAIN0 – DRAIN3	Drain Output 0 to 3
$\overline{CLR}$/A0	Clear/Address 0
D1/A1	Data 1/Address 1
GND	Ground
D2/A2	Data 2/Address 2
D3/A4	Data 3/Address 4
D4	Data 4
V_{CC}	Logic Supply Voltage
DATA I/O	Program Data Input/Output
V_{PP}	Programming Supply Voltage
PGM	Program Enable
V_{DD}	Output Supply Voltage
CLK/A3	Clock/Address 3

FUNCTION TABLE
(each channel)

INPUTS			OUTPUT DRAIN
$\overline{CLR}$	CLK	D	
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

User-programmable functions are controlled through 32 EEPROM bits. These bits are programmed by placing the TPIC6E175 into program mode by taking PGM high. The address to be programmed is then set up on dual functionality terminals A0–A4 (see Tables 1 and 2). The data bit to be programmed is set up on DATA I/O, and V_{PP} is then ramped from V_{CC} to V_{PPH} and back to V_{CC} to program the bit. The programming data can then be verified by taking VER high while monitoring DATA I/O, which gives the value of the data at the address selected on A0–A4. For each user-programmable parameter, Table 3 shows the binary programming values and the option selected by each programming value.

The TPIC6E175 contains four positive-edge-triggered D-type flip-flops with direct clear input. Each flip-flop features an open-drain power DMOS-transistor output.

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description (continued)

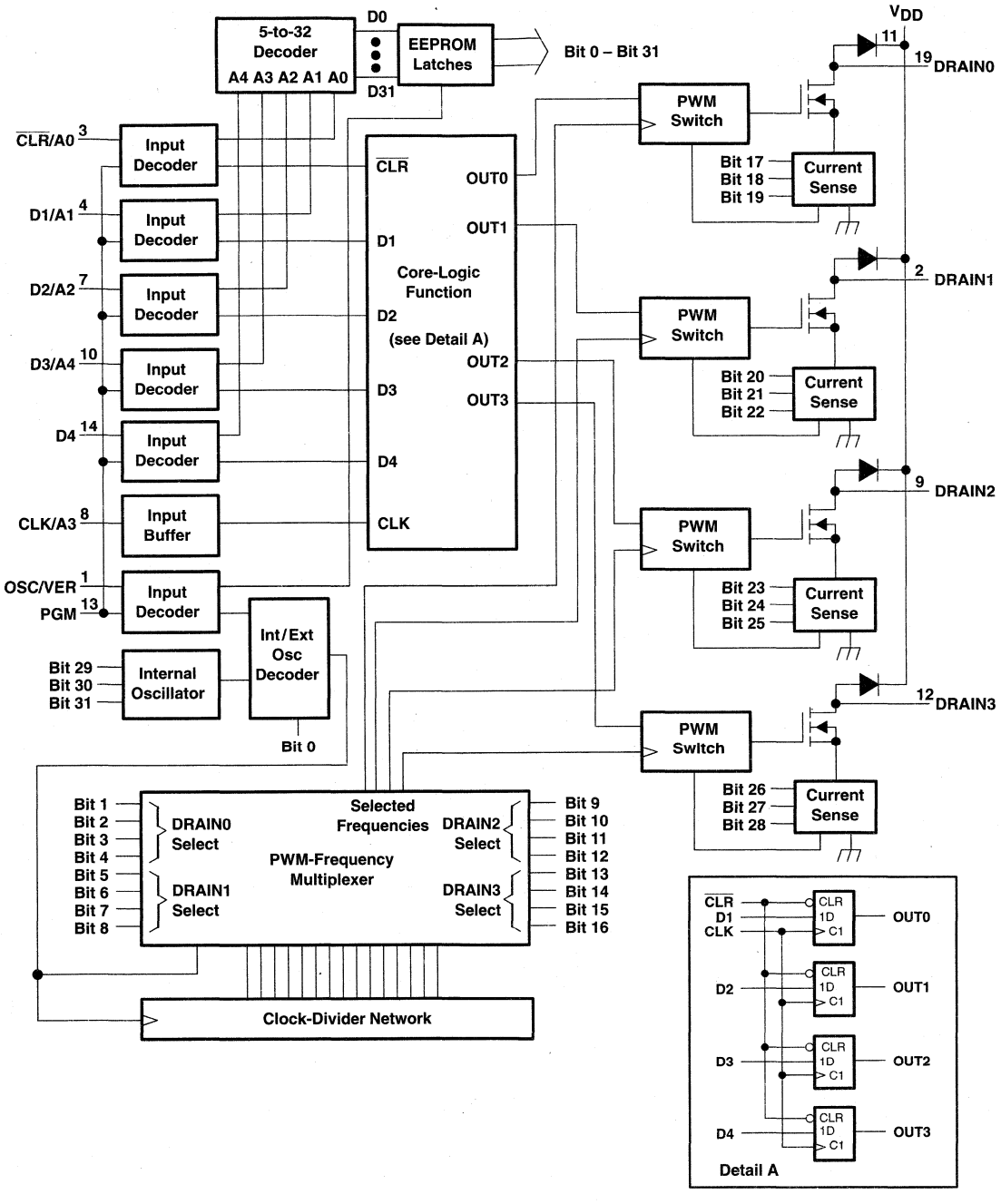
When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements, is transferred to the DRAIN outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all four DMOS-transistor outputs off. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

For proper operation, V_{DD} must be connected to a voltage source equal to or greater than the maximum drain voltage in the application.

The TPIC6E175 is offered in a 20-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the operating case temperature range of –40°C to 125°C.

PRODUCT PREVIEW

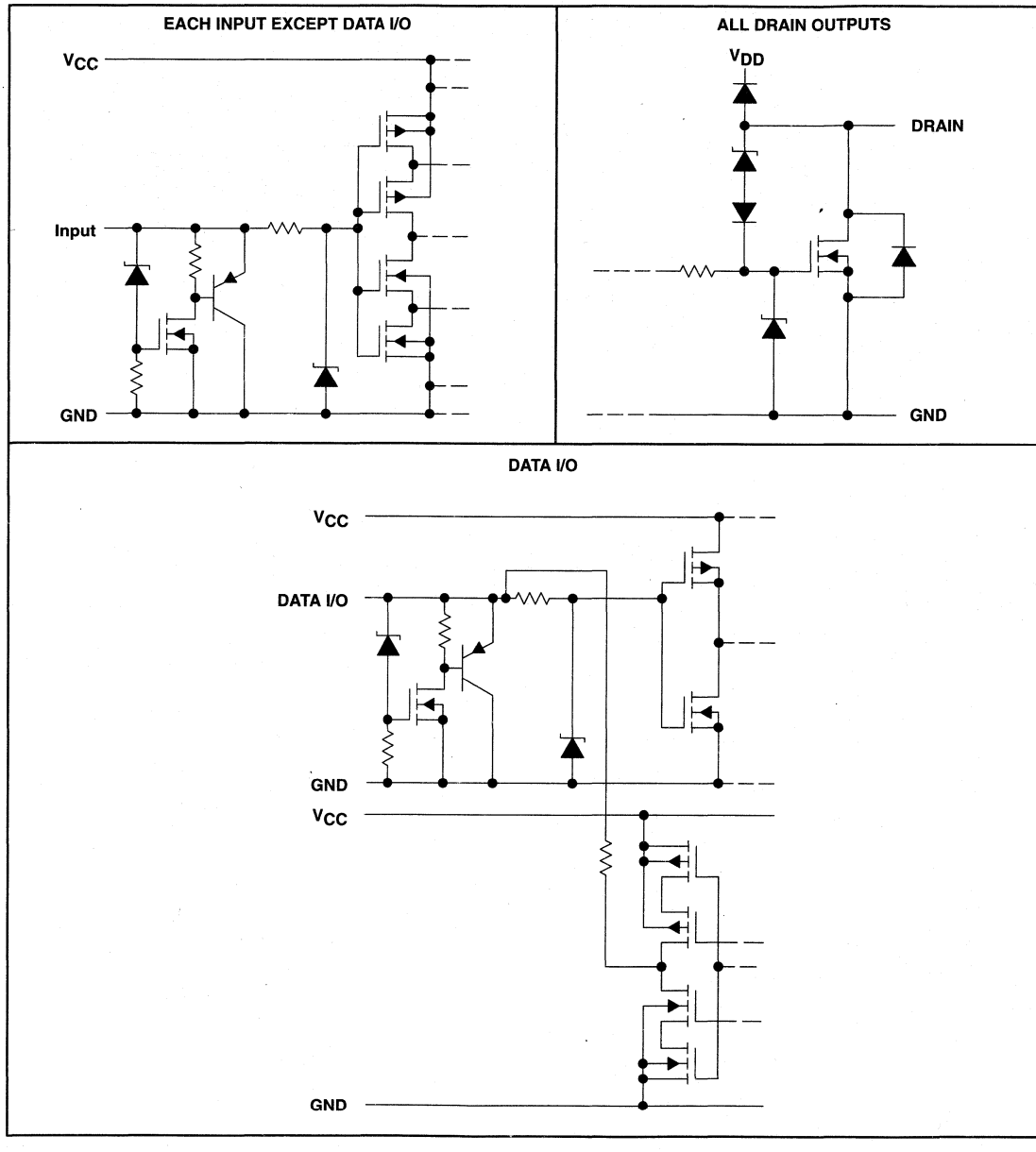
functional block diagram



PRODUCT PREVIEW

PRODUCT PREVIEW

equivalent inputs and outputs



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DATA I/O	18	I/O	Programming data input/output
DRAIN0 DRAIN1 DRAIN2 DRAIN3	19 2 9 12	O	Drain outputs 0–3
D2/A2	7	I	Data 2 or Address 2
GND	5, 6, 15, 16	—	Ground
OSC/VER	1	I	Oscillator or Programming verify
PGM	13	I	Program enable
D3/A4	10	I	Data 3 or Address 4
$\overline{CLR}$/A0	3	I	Clear or Address 0
CLK/A3	8	O	Clock or Address 3
D1/A1	4	I	Data 1 or Address 1
D4	14	I	Data 4
V_{CC}	20	—	Logic supply voltage
V_{DD}	11	—	Output supply voltage
V_{PP}	17	—	Programming supply voltage

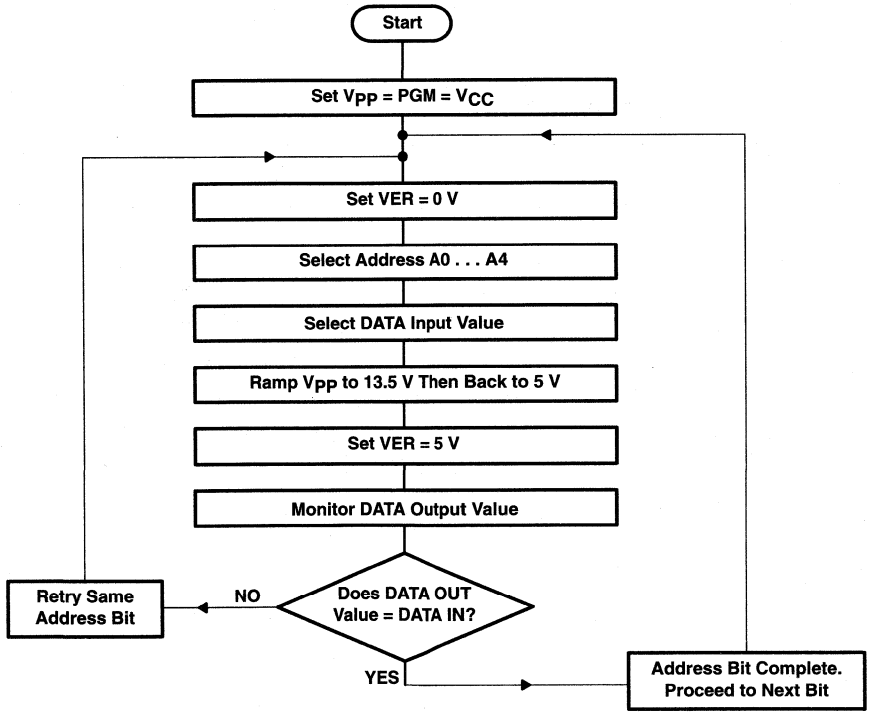

Figure 1. Recommended EEPROM Programming Sequence

PRODUCT PREVIEW

Table 1. Function Selection for Dual-Functionality Terminals

TERMINAL NUMBER	NORMAL MODE (PGM = L)	PROGRAM MODE (PGM = H)
1	OSC	VER
3	$\overline{\text{CLR}}$	A0
4	D1	A1
7	D2	A2
8	CLK	A3
10	D3	A4

H = high level, L = low level

Table 2. EEPROM Bit Description

BIT NO.	BIT ADDRESS	USER-PROGRAMMABLE PARAMETER	DESCRIPTION†
0	00000	Internal/External Oscillator	Selects internal or external oscillator to be used for PWM clock
1 (LSB) 2 3 4 (MSB)	00001 00010 00011 00100	DRAIN0 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
5 (LSB) 6 7 8 (MSB)	00101 00110 00111 01000	DRAIN1 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
9 (LSB) 10 11 12 (MSB)	01001 01010 01011 01100	DRAIN2 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
13 (LSB) 14 15 16 (MSB)	01101 01110 01111 10000	DRAIN3 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
17 (LSB) 18 19 (MSB)	10001 10010 10011	DRAIN0 Current Sense Adjust	Selects the peak current for the PWM-chop mode
20 (LSB) 21 22 (MSB)	10100 10101 10110	DRAIN1 Current Sense Adjust	Selects the peak current for the PWM-chop mode
23 (LSB) 24 25 (MSB)	10111 11000 11001	DRAIN2 Current Sense Adjust	Selects the peak current for the PWM-chop mode
26 (LSB) 27 28 (MSB)	11010 11011 11100	DRAIN3 Current Sense Adjust	Selects the peak current for the PWM-chop mode
29 (LSB) 30 31 (MSB)	11101 11110 11111	Oscillator Frequency Adjust	Selects the frequency of the internal oscillator

† See Table 3

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Table 3. EEPROM Programming Values

PROGRAMMABLE PARAMETER	OPTION SELECTED	BINARY VALUE MSB< . . . > LSB
Internal/External Oscillator	Internal Oscillator	0
	External Oscillator	1
Frequency Multiplexer for All Drain Outputs	Oscillator ÷ 1	0000
	Oscillator ÷ 2	0001
	Oscillator ÷ 4	0010
	Oscillator ÷ 8	0011
	Oscillator ÷ 16	0100
	Oscillator ÷ 32	0101
	Oscillator ÷ 64	0110
	Oscillator ÷ 128	0111
	Oscillator ÷ 256	1000
	Oscillator ÷ 512	1001
	Oscillator ÷ 1024	1010
	Oscillator ÷ 2048	1011
	Oscillator ÷ 4096	1100
	Oscillator ÷ 8192	1101
	Oscillator ÷ 16384	1110
	Oscillator ÷ 32768	1111
Current Sense Adjust for All Drain Outputs	300 mA†	000
	400 mA†	001
	500 mA†	010
	600 mA†	011
	700 mA†	100
	800 mA†	101
	900 mA†	110
	1000 mA†	111
Oscillator Frequency Adjust	Internal Oscillator, Frequency = 1.2 MHz	000
	Internal Oscillator, Frequency = 1.1 MHz	001
	Internal Oscillator, Frequency = 0.9 MHz	010
	Internal Oscillator, Frequency = 0.8 MHz	011
	Internal Oscillator, Frequency = 0.6 MHz	100
	Internal Oscillator, Frequency = 0.5 MHz	101
	Internal Oscillator, Frequency = 0.3 MHz	110
	Internal Oscillator, Frequency = 0.1 MHz	111

† Current target ±20%

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absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) ..... 7 V
Logic input voltage range, V_I ..... −0.3 V to 7 V
Output supply voltage, V_{DD} (see Note 1) ..... 40 V
Programming supply voltage during programming, V_{PP} (see Notes 1 and 2) ..... 16 V
Programming supply voltage, verify/normal operation, V_{PP} ..... 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 3) ..... 40 V
Continuous source-to-drain diode current ..... 1 A
Pulsed source-to-drain diode current (see Note 3) ..... 1 A
PWM output current, each output, all outputs on, $I_{O(PWM)}$, T_A = 25°C, d = 10%
(see Note 4 and Figure 10) ..... 900 mA
PWM output current, each output, all outputs on, $I_{O(PWM)}$, T_A = 25°C, d = 50%
(see Note 4 and Figure 9) ..... 800 mA
Peak drain current, single output, $I_{D(PWM)}$, T_A = 25°C (see Notes 3 and 4) ..... 1 A
Avalanche current, $I_{(av)}$ (see Note 5 and Figure 7) ..... 1 A
Single-pulse avalanche energy, E_A (see Note 5 and Figure 7) ..... 100 mJ
Continuous total power dissipation ..... See Dissipation Rating Table
Operating case temperature range, T_C ..... −40°C to 125°C
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. For programming waveform, see Figure 2.
3. Each power DMOS source is internally connected to GND. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
4. Output current depends upon program current-sense adjust and load conditions.
5. V_{supply} = 24 V, starting junction temperature, (T_{JS}) = 25°C, L = 87 mH, I_{AS} = 1 A.

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
NE	2775 mW	20 mW/°C	775 mW
NE on FR-4 PCB	4163 mW	33.3 mW/°C	833 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
Output supply voltage, V_{DD}		40	V
Programming supply voltage during programming, V_{PP}	12	15	V
Programming supply voltage during verify or normal operation, V_{PP}	V_{CC}−0.7	V_{CC}	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Operating case temperature, T_C	−40	125	°C

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA			40			V
V_{SD}	Source-drain diode forward voltage	I_F = 1 A				1	1.5	V
$V_{OH(DATA\ I/O)}$	High-level data output voltage	I_{OH} = −100 µA,	V_{CC} = 4.5 V		4.25	4.48		V
$V_{OL(DATA\ I/O)}$	Low-level data output voltage	I_{OL} = 100 µA,	V_{CC} = 4.5 V			200	250	mV
V_f	Forward clamp voltage	I_f = 1 A				1.35	2	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0,	All inputs low			1.6	5	mA
$I_{CC(freq)}$	Logic supply current at frequency	SRCK = 5 MHz,	I_O = 0			5.5		mA
I_{DS}	Off-state drain current	V_{DD} = 40 V,	V_{DS} = 35 V			0.2	1	µA
		V_{DD} = 40 V,	V_{DS} = 30 V,	T_C = 125°C		1	5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 200 mA,	V_{CC} = 4.5 V			1	1.5	Ω
		I_D = 200 mA,	V_{CC} = 4.5 V,	T_C = 125°C		1.6	2.4	
		I_D = 750 mA,	V_{CC} = 4.5 V			1.1	1.75	

timing requirements over recommended ranges of supply voltage and operating case temperature

		MIN	MAX	UNIT
t_{su}	Setup time, D high before CLK↑ (see Figure 5)	20		ns
t_{su1}	Setup time, VER to PGM (see Figure 2)	2		µs
t_{su2}	Setup time, address and DATA I/O to V_{PP} (see Figure 2)	2		µs
t_{su3}	Setup time, PGM to DATA I/O (see Figure 2)	2		µs
t_{su4}	Setup time, PGM to address (see Figure 2)	2		µs
t_h	Hold time, D high before CLK↑ (see Figure 5)	20		ns
t_{h1}	PGM hold time, DATA I/O (see Figure 2)	2		µs
t_{h2}	Hold time, DATA I/O after V_{PP} (see Figure 2)	2		µs
t_w	Pulse duration (see Figure 5)	40		ns
t_{w1}	Pulse duration, V_{PP} program (see Figure 2)	5		ms
t_{pd}	Propagation delay, VER to DATA I/O (see Figure 2)	2		µs
t_r	Rise time, V_{PP} during programming (see Figure 2)	2	3	ms
t_f	Fall time, V_{PP} during programming (see Figure 2)	2	3	ms

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, See Figure 5	I_D = 250 mA,		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK				150		ns
t_{r1}	Rise time, drain output (see Figure 5)				750		ns
t_{f1}	Fall time, drain output (see Figure 5)				425		ns
t_{rr}	Reverse-recovery time (see Figure 6)	I_F = 250 mA,	di/dt = 40 A/µs		300		ns
t_{rra}	Reverse-recovery current rise time (see Figure 6)				100		ns

PRODUCT PREVIEW

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All four outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All four outputs with equal power		50	

PARAMETER MEASUREMENT INFORMATION

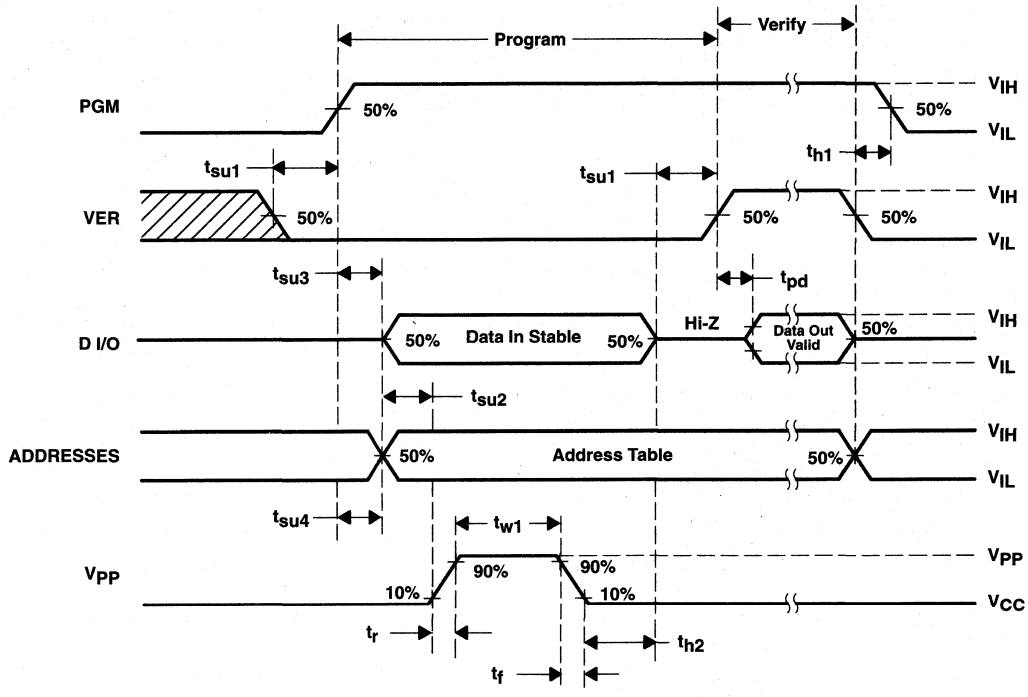


Figure 2. Programming Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

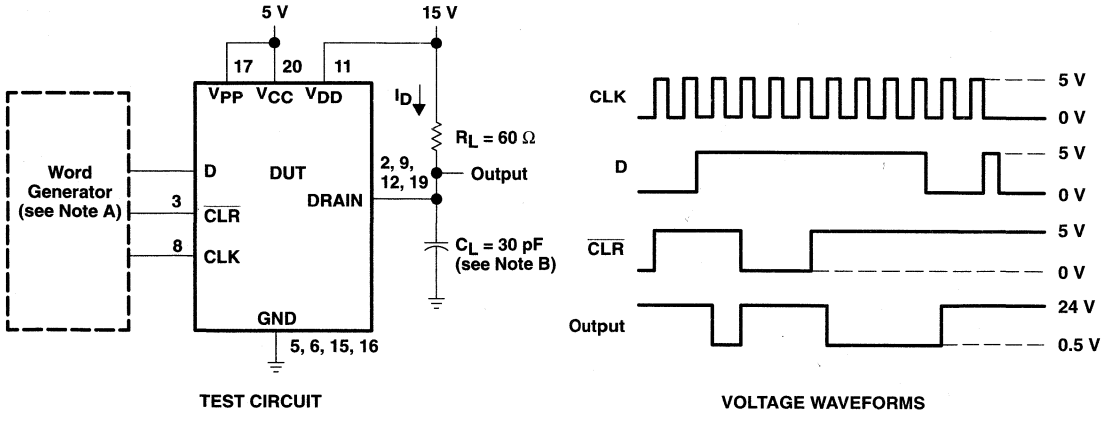


Figure 3. Resistive Load Operation

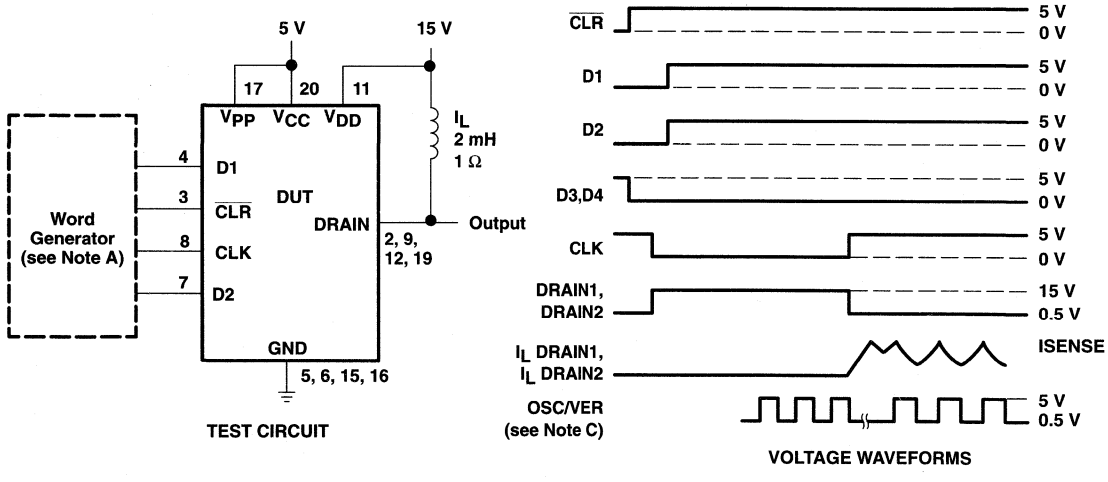
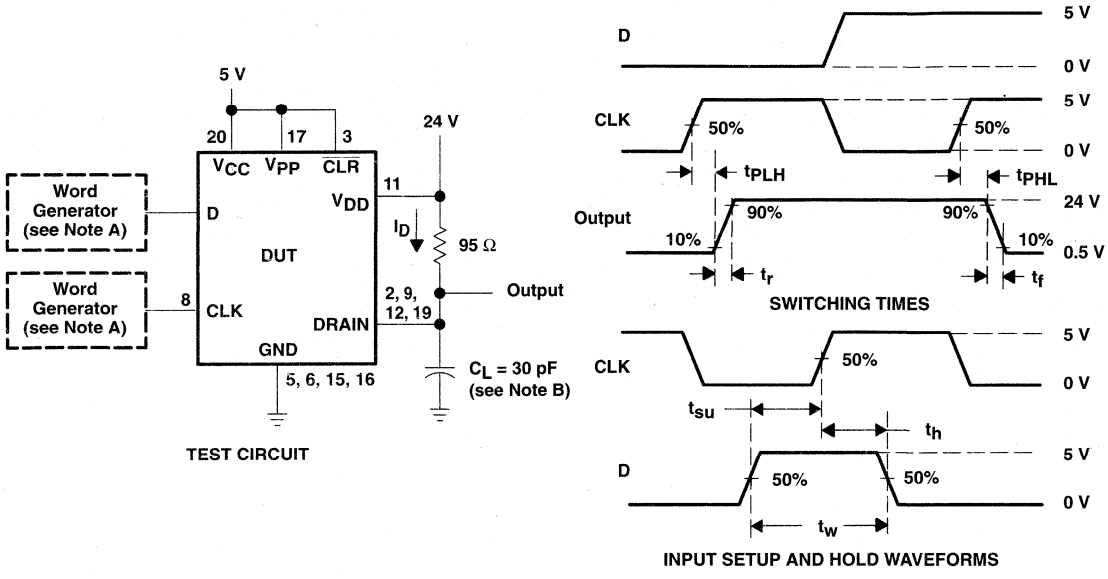


Figure 4. Inductor Load Operation

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. DRAIN0 and DRAIN3 remain at 15 V with 0_A I_L.

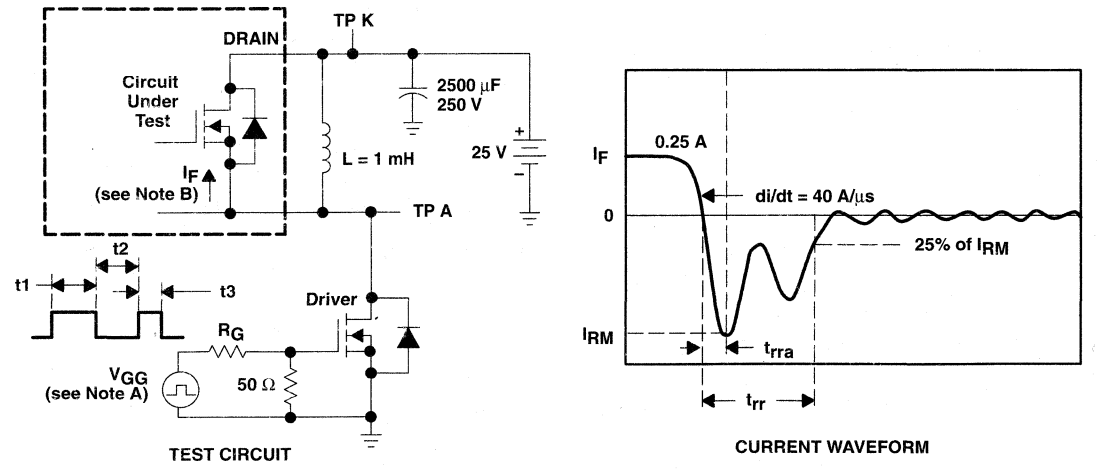
PRODUCT PREVIEW

PARAMETER MEASUREMENT



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

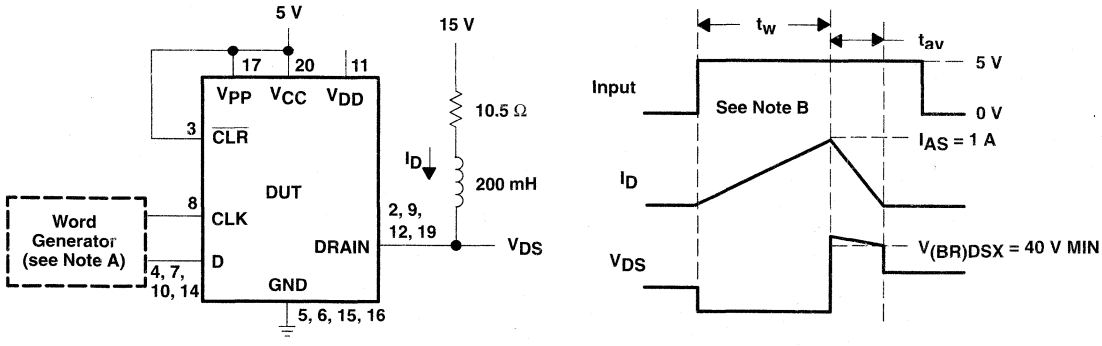
Figure 5. Test Circuit and Voltage Waveforms, Switching Times



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 40 A/µs. A V_{GG} double-pulse train sets I_F = 0.25 A, where t1 = 15 µs, t2 = 8.5 µs, and t3 = 3.5 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 6. Reverse-Recovery-Current Test Circuit and Waveform of Source Drive Device

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE-ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is controlled by the value of peak current $I_{AS} = 1$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 100$ mJ,
where t_{av} = avalanche time.

Figure 7. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

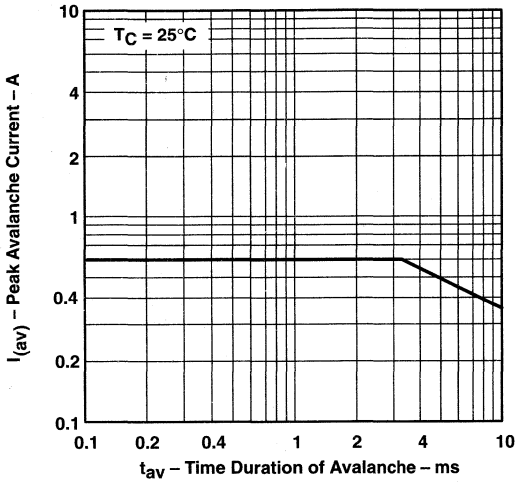


Figure 8

MAXIMUM PWM
CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

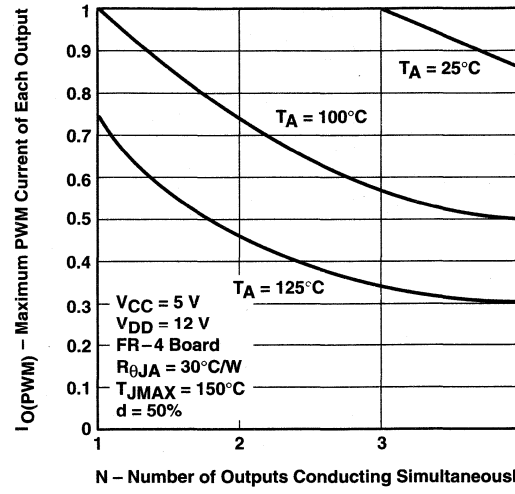


Figure 9

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

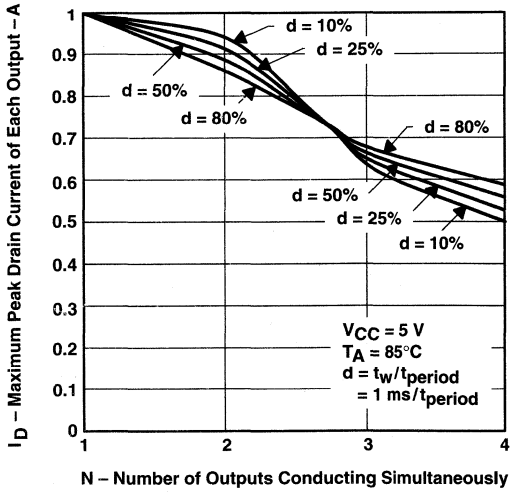
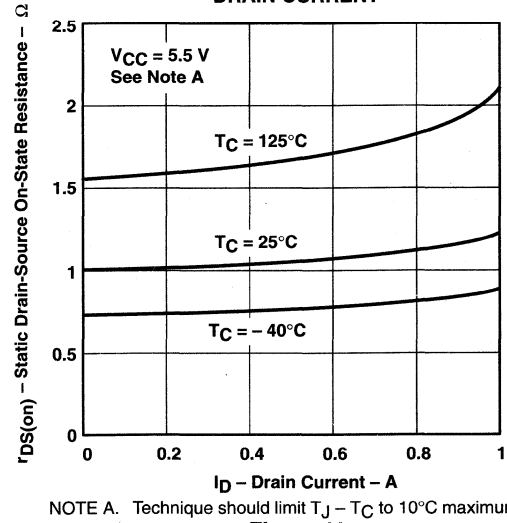


Figure 10

STATIC DRAIN-SOURCE
ON-STATE RESISTANCE
vs
DRAIN CURRENT

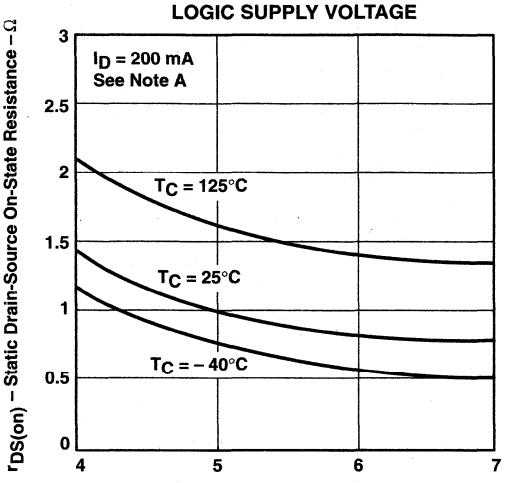


NOTE A. Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 12

SWITCHING TIME vs FREE-AIR TEMPERATURE

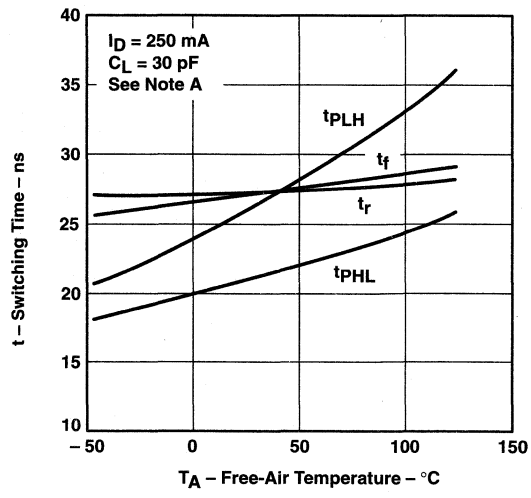
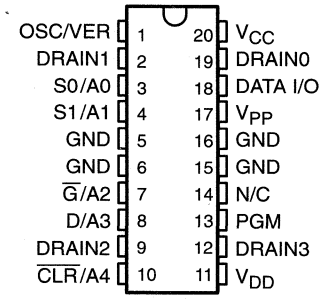


Figure 13

PRODUCT PREVIEW

- **Programmable-PWM Current Threshold**
- **Programmable-PWM Frequency Controlled by Internal or External Oscillator**
- **Integrated Output Recirculation Clamp Diodes**
- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Four Power MOSFET Outputs**
- **Integrated Snubbing Clamp Voltage at 40 V**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



description

The power logic 4-bit addressable latch pulse-width-modulation (PWM) driver controls open-drain DMOS transistor outputs and is designed for applications that require relatively high power. The device contains a built-in snubbing clamp and recirculation clamp on the outputs for inductive transient protection and inductive energy recirculation, respectively. Power driver applications include solenoids and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent user-programmable PWM circuit that works in conjunction with the recirculation clamping diode in order to control the average current in inductive-load applications. The PWM circuit provides a programmable current-limit threshold that disables the output until the next rising edge of the independent PWM programmable clock. Each clock is generated from a user-programmable internal or external clock reference that in turn is programmed independently for each output through a frequency divide-by circuit.

User-programmable functions are controlled via 32 EEPROM bits. These bits are programmed by placing the TPIC6E261 into program mode by taking PGM high. The address to be programmed is then set up on dual functionality terminals A0–A4 (see Tables 1 and 2). The data bit to be programmed is set up on DATA I/O, and V_{PP} is then ramped from V_{CC} to V_{PPH} and back to V_{CC} to program the bit. The programming data can then be verified by taking OSC/VER VER high while monitoring DATA I/O, which gives the value of the data at the address selected on A0–A4. For each user-programmable parameter, Table 3 shows the binary programming values and the option selected by each programming value.

TERMINAL NOMENCLATURE

OSC/VER	Oscillator/Verify
DRAIN0 – DRAIN3	Drain Output 0 to 3
S0/A0	Select 0/Address 0
S1/A1	Select 1/Address 1
GND	Ground
G/A2	Function Select/Address 2
D/A3	Data/Address 3
CLR/A4	Function Select/Address 4
V_{CC}	Logic Supply Voltage
DATA I/O	Program Data Input/Output
V_{PP}	Programming Supply Voltage
PGM	Program Enable
V_{DD}	Output Supply Voltage

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
CLR	G	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

SELECT INPUTS		DRAIN ADDRESSED
S1	S0	
L	L	0
L	H	1
H	L	2
H	H	3

PRODUCT PREVIEW

description (continued)

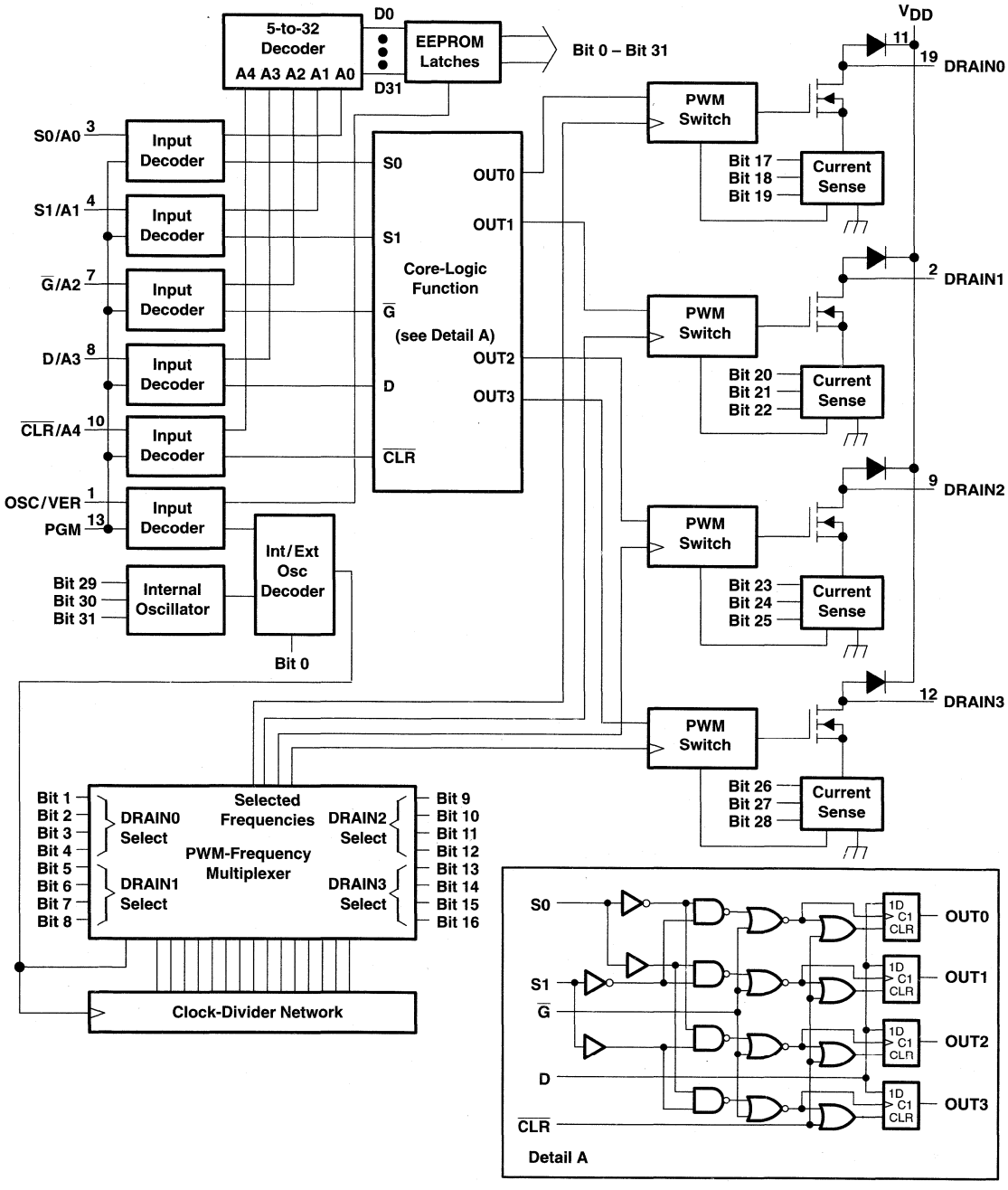
Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

For proper operation, V_{DD} must be connected to a voltage source equal to or greater than the maximum drain voltage in the application.

The TPIC6E261 is offered in a 20-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the operating case temperature range of –40°C to 125°C.

PRODUCT PREVIEW

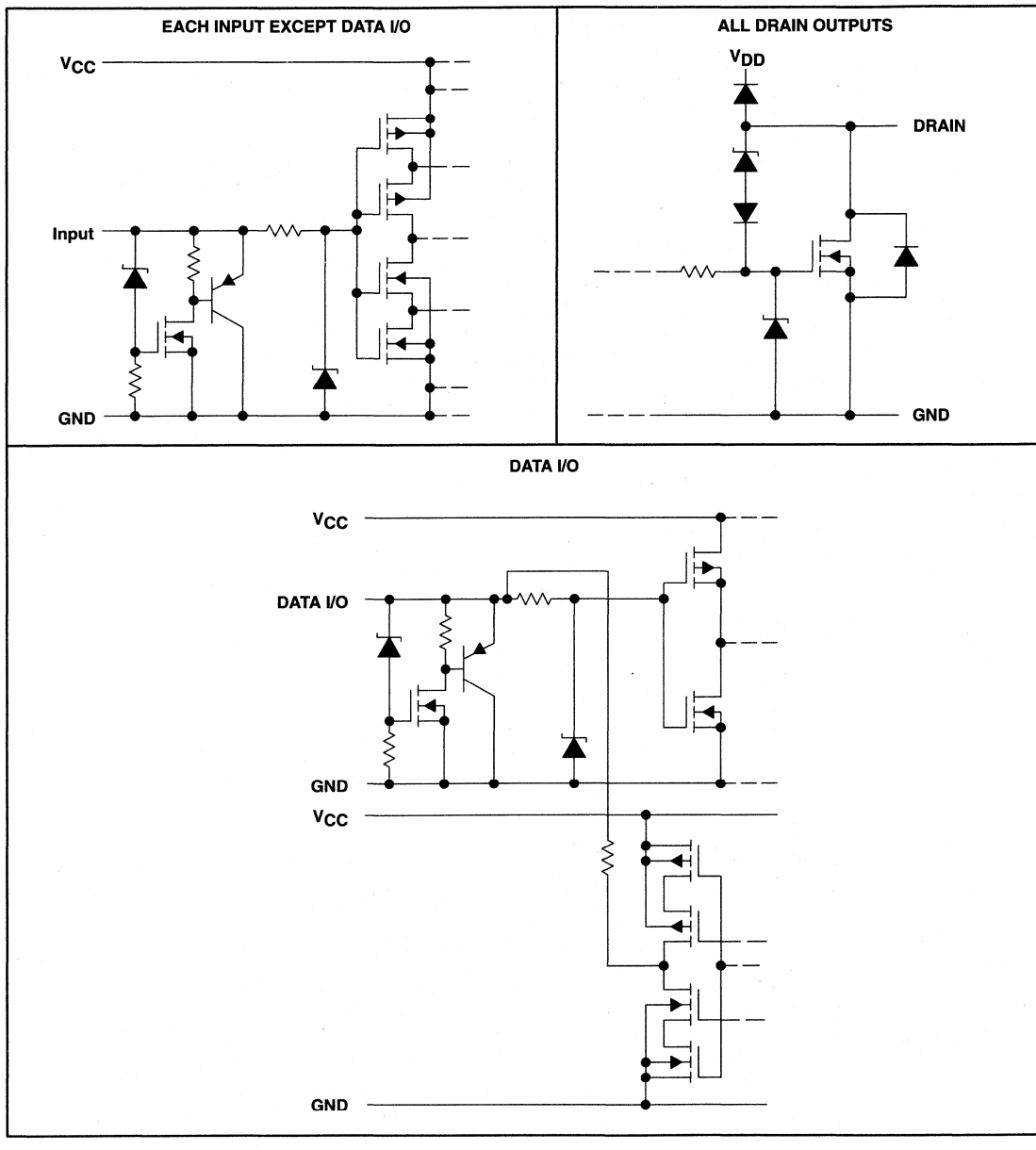
functional block diagram



PRODUCT PREVIEW

PRODUCT PREVIEW

equivalent inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DATA I/O	18	I/O	Programming data input/output
DRAIN0 DRAIN1 DRAIN2 DRAIN3	19 2 9 12	O	Drain outputs 0 to 3
$\overline{G}$/A2	7	I	Function select or Address 2
GND	5, 6, 15, 16	—	Ground
OSC/VER	1	I	Oscillator or Programming verify
PGM	13	I	Program enable
D/A3	8	I	Data or Address 3
S0/A0	3	I	Select 0 or Address 0
S1/A1	4	I	Select 1 or Address 1
$\overline{CLR}$/A4	10	I	Function select or Address 4
V_{CC}	20	—	Logic supply voltage
V_{DD}	11	—	Output supply voltage
V_{PP}	17	—	Programming supply voltage

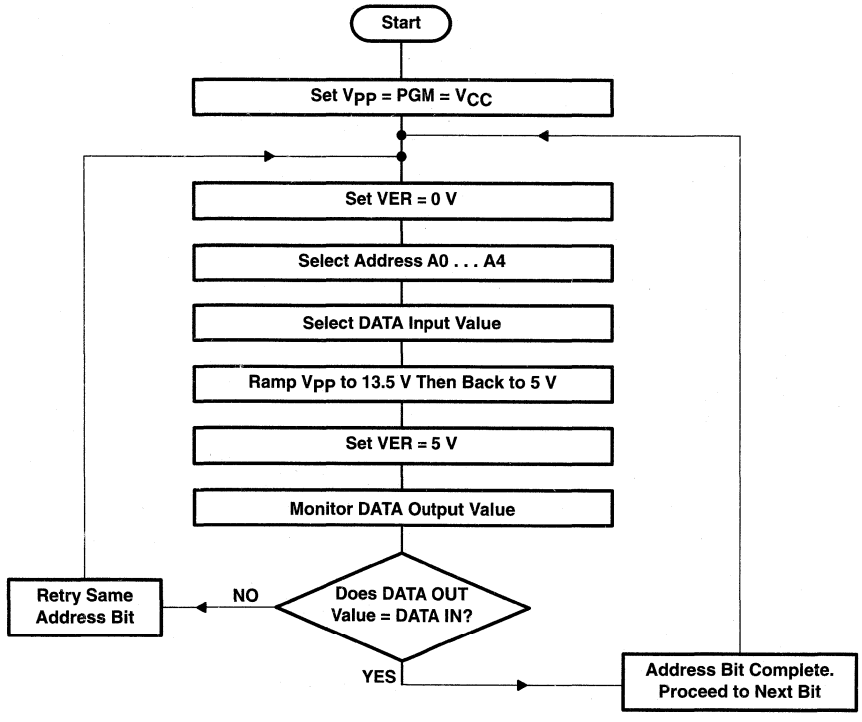


Figure 1. Recommended EEPROM Programming Sequence

PRODUCT PREVIEW

Table 1. Function Selection for Dual-Functionality Terminals

TERMINAL NUMBER	NORMAL MODE (PGM = L)	PROGRAM MODE (PGM = H)
1	OSC	VER
3	S0	A0
4	S1	A1
7	$\overline{G}$	A2
8	D	A3
10	$\overline{CLR}$	A4

H = high level, L = low level

Table 2. EEPROM Bit Description

BIT NO.	BIT ADDRESS	USER-PROGRAMMABLE PARAMETER	DESCRIPTION†
0	00000	Internal/External Oscillator	Selects internal or external oscillator to be used for PWM clock
1 (LSB)	00001	DRAIN0 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
2	00010		
3	00011		
4 (MSB)	00100		
5 (LSB)	00101	DRAIN1 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
6	00110		
7	00111		
8 (MSB)	01000		
9 (LSB)	01001	DRAIN2 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
10	01010		
11	01011		
12 (MSB)	01100		
13 (LSB)	01101	DRAIN3 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
14	01110		
15	01111		
16 (MSB)	10000		
17 (LSB)	10001	DRAIN0 Current Sense Adjust	Selects the peak current for the PWM-chop mode
18	10010		
19 (MSB)	10011		
20 (LSB)	10100	DRAIN1 Current Sense Adjust	Selects the peak current for the PWM-chop mode
21	10101		
22 (MSB)	10110		
23 (LSB)	10111	DRAIN2 Current Sense Adjust	Selects the peak current for the PWM-chop mode
24	11000		
25 (MSB)	11001		
26 (LSB)	11010	DRAIN3 Current Sense Adjust	Selects the peak current for the PWM-chop mode
27	11011		
28 (MSB)	11100		
29 (LSB)	11101	Oscillator Frequency Adjust	Selects the frequency of the internal oscillator
30	11110		
31 (MSB)	11111		

† See Table 3

PRODUCT PREVIEW

Table 3. EEPROM Programming Values

PROGRAMMABLE PARAMETER	OPTION SELECTED	BINARY VALUE MSB< . . . > LSB
Internal/External Oscillator	Internal Oscillator	0
	External Oscillator	1
Frequency Multiplexer for All Drain Outputs	Oscillator ÷ 1	0000
	Oscillator ÷ 2	0001
	Oscillator ÷ 4	0010
	Oscillator ÷ 8	0011
	Oscillator ÷ 16	0100
	Oscillator ÷ 32	0101
	Oscillator ÷ 64	0110
	Oscillator ÷ 128	0111
	Oscillator ÷ 256	1000
	Oscillator ÷ 512	1001
	Oscillator ÷ 1024	1010
	Oscillator ÷ 2048	1011
	Oscillator ÷ 4096	1100
	Oscillator ÷ 8192	1101
	Oscillator ÷ 16384	1110
	Oscillator ÷ 32768	1111
Current Sense Adjust for All Drain Outputs	300 mA†	000
	400 mA†	001
	500 mA†	010
	600 mA†	011
	700 mA†	100
	800 mA†	101
	900 mA†	110
	1000 mA†	111
Oscillator Frequency Adjust	Internal Oscillator, Frequency = 1.2 MHz	000
	Internal Oscillator, Frequency = 1.1 MHz	001
	Internal Oscillator, Frequency = 0.9 MHz	010
	Internal Oscillator, Frequency = 0.8 MHz	011
	Internal Oscillator, Frequency = 0.6 MHz	100
	Internal Oscillator, Frequency = 0.5 MHz	101
	Internal Oscillator, Frequency = 0.3 MHz	110
	Internal Oscillator, Frequency = 0.1 MHz	111

† Current target ±20%

PRODUCT PREVIEW

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) ..... 7 V
Logic input voltage range, V_I ..... −0.3 V to 7 V
Output supply voltage, V_{DD} (see Note 1) ..... 40 V
Programming supply voltage during programming, V_{PP} (see Notes 1 and 2) ..... 16 V
Programming supply voltage, verify/normal operation, V_{PP} ..... 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 3) ..... 40 V
Continuous source-to-drain diode current ..... 1 A
Pulsed source-to-drain diode current (see Note 3) ..... 1 A
PWM output current, each output, all outputs on, $I_{O(PWM)}$, T_A = 25°C, d = 10%
(see Note 4 and Figure 10) ..... 900 mA
PWM output current, each output, all outputs on, $I_{O(PWM)}$, T_A = 25°C, d = 50%
(see Note 4 and Figure 9) ..... 800 mA
Peak drain current, single output, $I_{D(Peak)}$, T_A = 25°C (see Notes 3 and 4) ..... 1 A
Peak Avalanche current, $I_{(av)}$ (see Note 5 and Figure 7) ..... 1 A
Single-pulse avalanche energy, E_A (see Note 5 and Figure 7) ..... 100 mJ
Continuous total power dissipation ..... See Dissipation Rating Table
Operating case temperature range, T_C ..... −40°C to 125°C
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. For programming waveform, see Figure 2.
3. Each power DMOS source is internally connected to GND. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
4. Output current depends upon program current-sense adjust and load conditions.
5. V_{supply} = 24 V, starting junction temperature, (T_{JS}) = 25°C, L = 87 mH, I_{AS} = 1 A.

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
NE	2775 mW	20 mW/°C	775 mW
NE on FR-4 PCB	4163 mW	33.3 mW/°C	833 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
Output supply voltage, V_{DD}		40	V
Programming supply voltage during programming, V_{PP}	12	15	V
Programming supply voltage during verify or normal operation, V_{PP}	V_{CC}−0.7	V_{CC}	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Operating case temperature, T_C	−40	125	°C

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA			40			V
V_{SD}	Source-drain diode forward voltage	I_F = 1 A				1	1.5	V
$V_{OH(DATA\ I/O)}$	High-level data output voltage	I_{OH} = −100 µA,	V_{CC} = 4.5 V		4.25	4.48		V
$V_{OL(DATA\ I/O)}$	Low-level data output voltage	I_{OL} = 100 µA,	V_{CC} = 4.5 V			200	250	mV
V_f	Forward clamp voltage	I_f = 1 A				1.35	2	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0,	All inputs low			1.6	5	mA
$I_{CC(freq)}$	Logic supply current at frequency	SRCK = 5 MHz,	I_O = 0			5.5		mA
I_{DS}	Off-state drain current	V_{DD} = 40 V,	V_{DS} = 35 V			0.2	1	µA
		V_{DD} = 40 V,	V_{DS} = 30 V,	T_C = 125°C		1	5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 200 mA,	V_{CC} = 4.5 V			1	1.5	Ω
		I_D = 200 mA,	V_{CC} = 4.5 V,	T_C = 125°C		1.6	2.4	
		I_D = 750 mA,	V_{CC} = 4.5 V			1.1	1.75	

timing requirements over recommended ranges of supply voltage and operating case temperature

		MIN	MAX	UNIT
t_{su}	Setup time, D high before $\overline{G}\uparrow$ (see Figure 5)	20		ns
t_{su1}	Setup time, VER to PGM (see Figure 2)	2		µs
t_{su2}	Setup time, address and DATA I/O to V_{PP} (see Figure 2)	2		µs
t_{su3}	Setup time, PGM to DATA I/O (see Figure 2)	2		µs
t_{su4}	Setup time, PGM to address (see Figure 2)	2		µs
t_h	Hold time, D high before $\overline{G}\uparrow$ (see Figure 5)	20		ns
t_{h1}	PGM hold time, DATA I/O (see Figure 2)	2		µs
t_{h2}	Hold time, DATA I/O after V_{PP} (see Figure 2)	2		µs
t_w	Pulse duration (see Figure 5)	40		ns
t_{w1}	Pulse duration, V_{PP} program (see Figure 2)	5		ms
t_{pd}	Propagation delay, VER to DATA I/O (see Figure 2)	2		µs
t_r	Rise time, V_{PP} during programming (see Figure 2)	2	3	ms
t_f	Fall time, V_{PP} during programming (see Figure 2)	2	3	ms

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from D	C_L = 30 pF, See Figure 5	I_D = 250 mA,		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from D				150		ns
t_{r1}	Rise time, drain output (see Figure 5)				750		ns
t_{f1}	Fall time, drain output (see Figure 5)				425		ns
t_{rr}	Reverse-recovery time (see Figure 6)	I_F = 250 mA,	di/dt = 40 A/µs		300		ns
t_{rra}	Reverse-recovery current rise time (see Figure 6)				100		ns

PRODUCT PREVIEW

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All four outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All four outputs with equal power		50	

PARAMETER MEASUREMENT INFORMATION

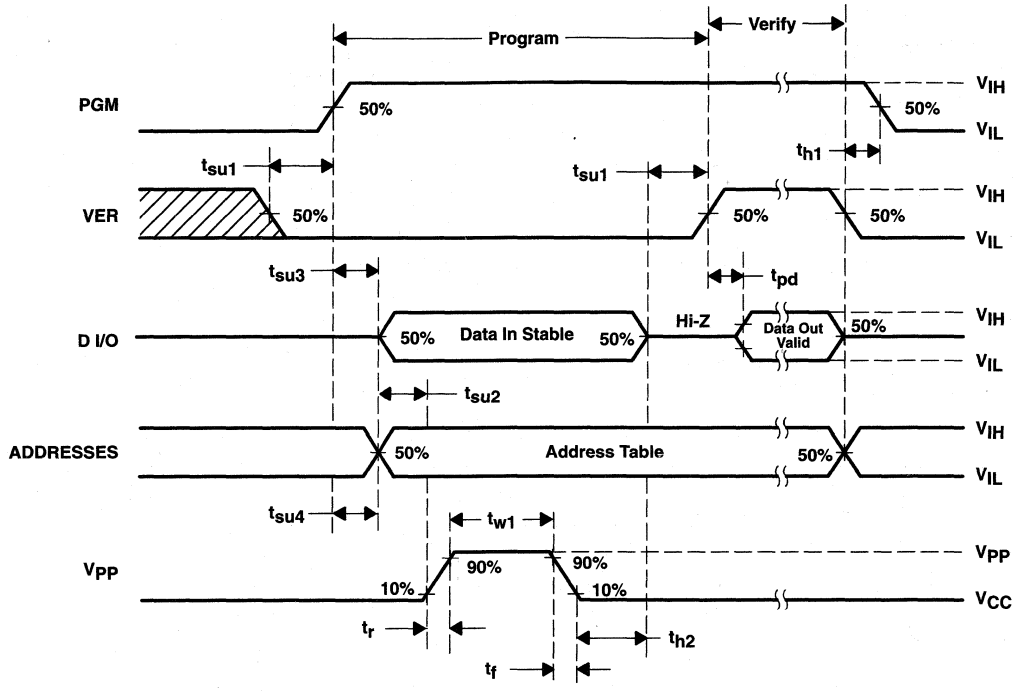


Figure 2. Programming Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

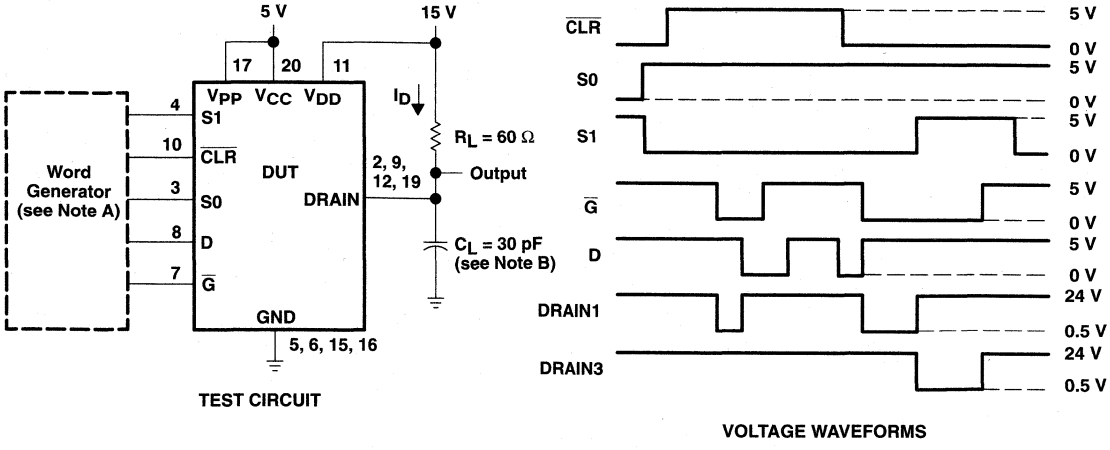


Figure 3. Resistive Load Operation

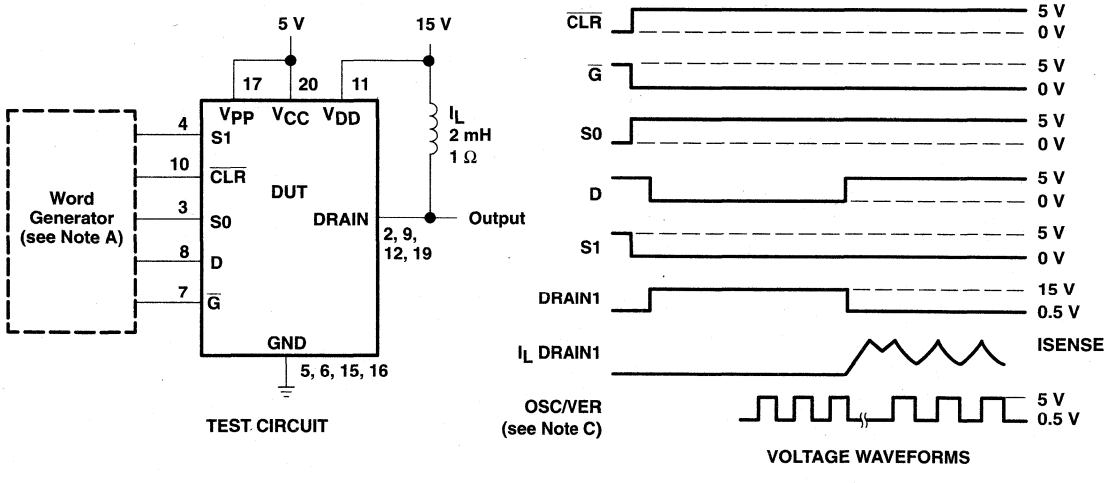
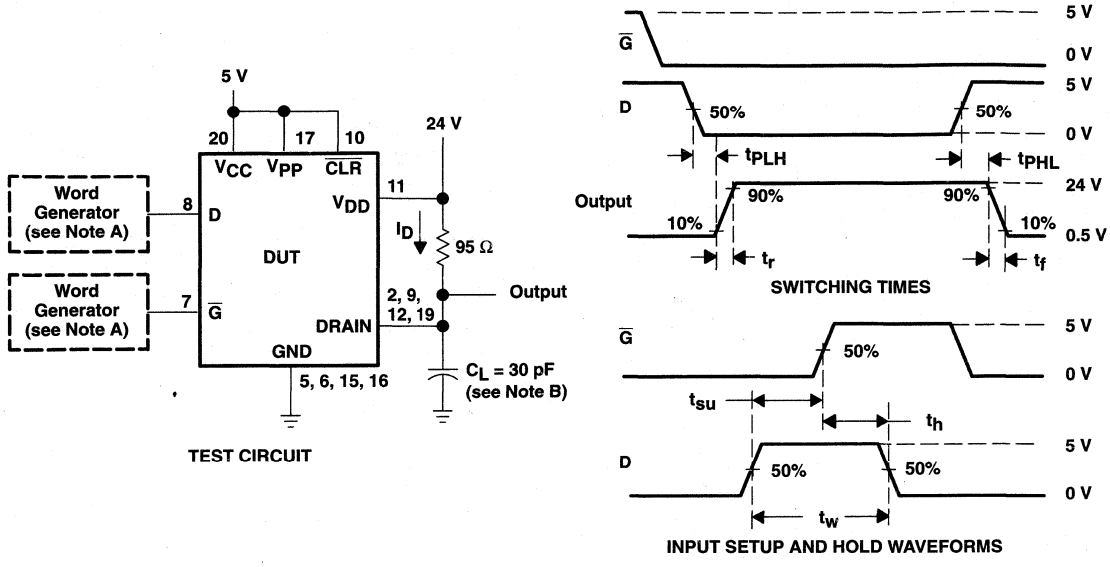


Figure 4. Inductor Load Operation

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. DRAIN0 and DRAIN3 remain at 15 V with 0_A I_L.

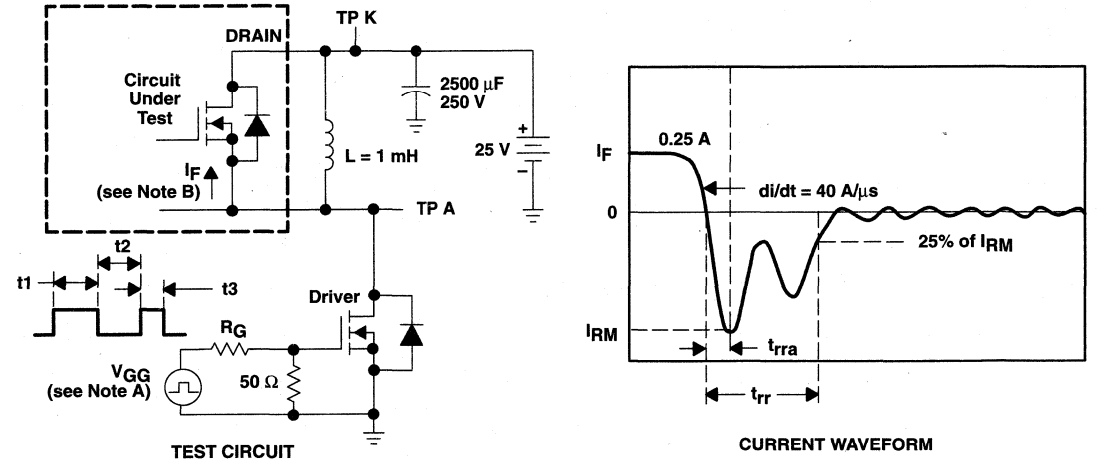
PRODUCT PREVIEW

PARAMETER MEASUREMENT



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 5. Test Circuit and Voltage Waveforms, Switching Times

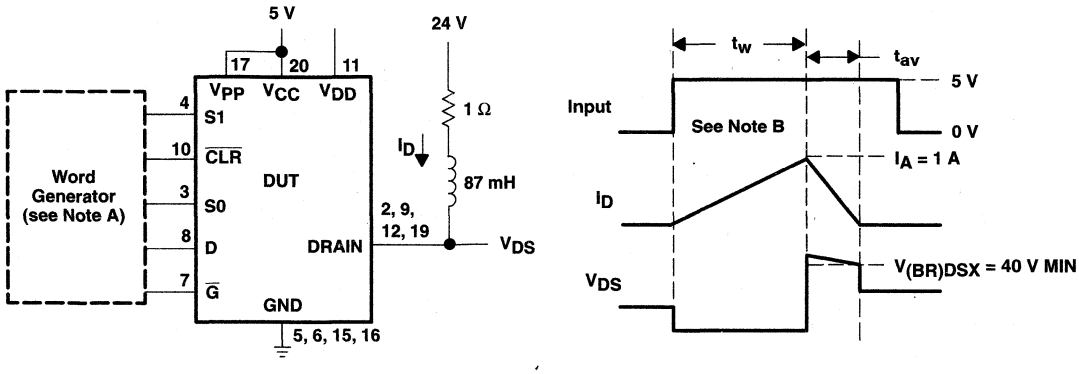


NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 40 A/µs. A V_{GG} double-pulse train sets I_F = 0.25 A, where t1 = 15 µs, t2 = 8.5 µs, and t3 = 3.5 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 6. Reverse-Recovery-Current Test Circuit and Waveform of Source Drive Device

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE-ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_W) is controlled by the value of peak avalanche current $I_{(av)} = 1$ A.

Energy test level is defined as $E_A = \dfrac{I_{(av)} \times V_{(BR)DSX} \times t_{av}}{2} = 100$ mJ,

where t_{av} = avalanche time.

Figure 7. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

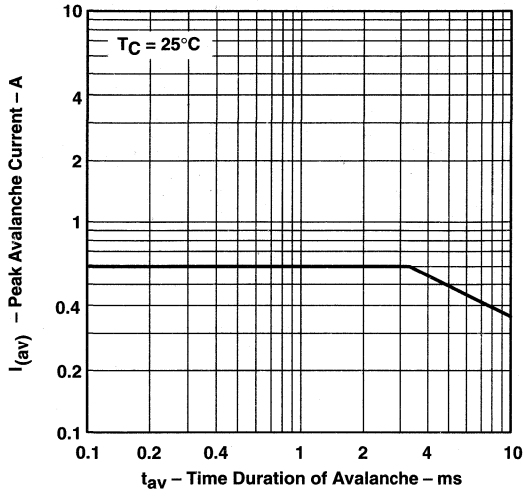


Figure 8

MAXIMUM PWM
CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

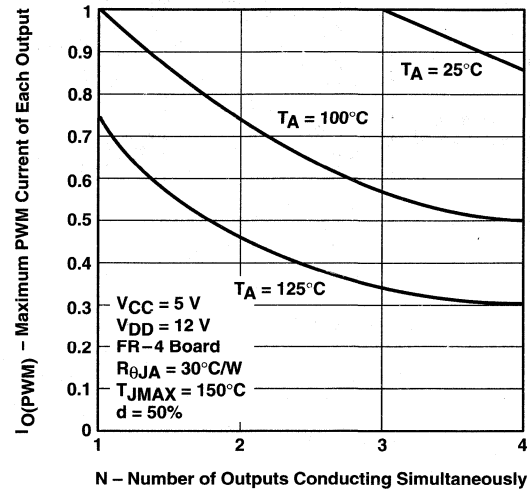


Figure 9

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

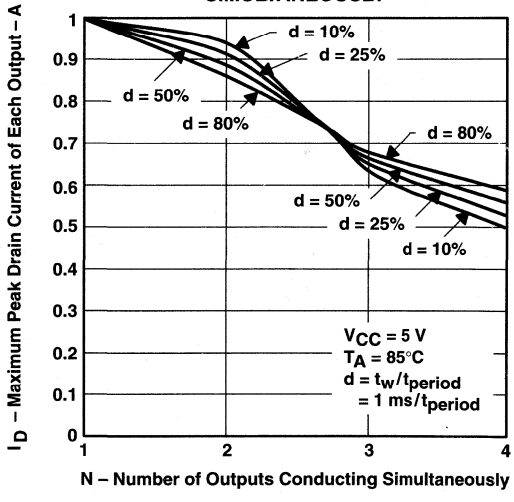
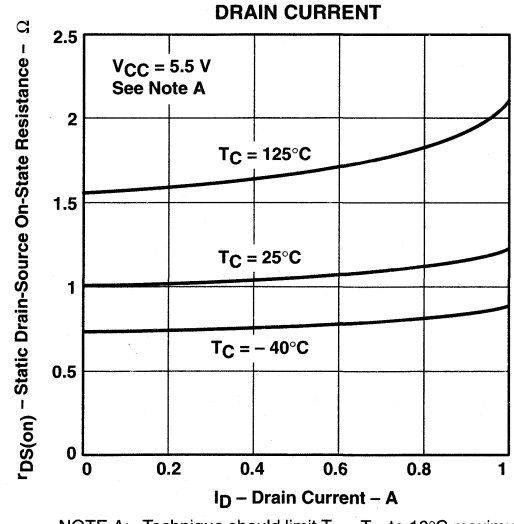


Figure 10

STATIC DRAIN-SOURCE
ON-STATE RESISTANCE
vs
DRAIN CURRENT



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

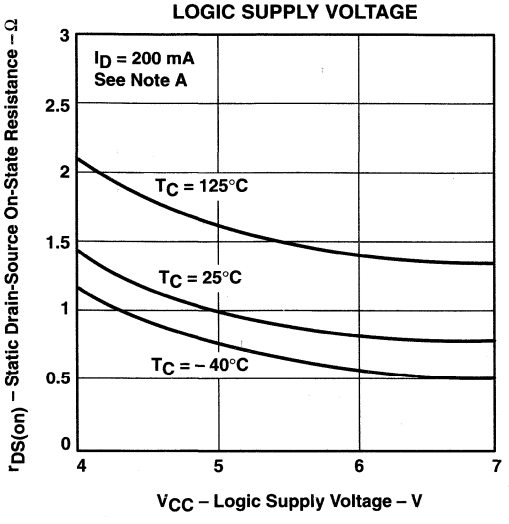


Figure 12

SWITCHING TIME vs FREE-AIR TEMPERATURE

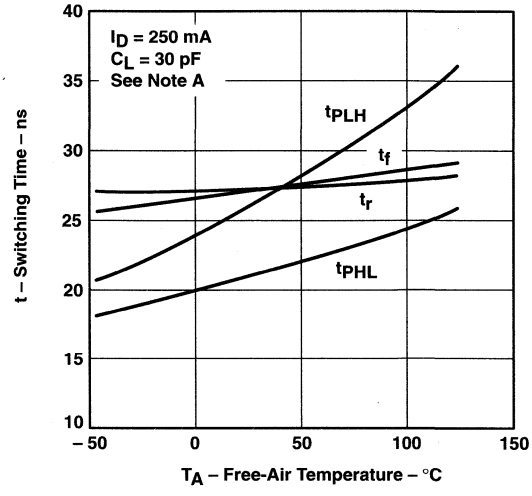


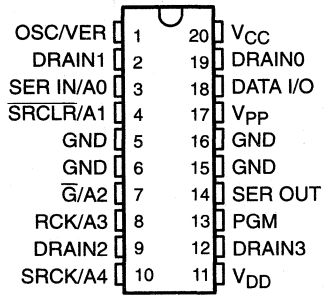
Figure 13

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

PRODUCT PREVIEW

- **Programmable-PWM Current Threshold**
- **Programmable-PWM Frequency Controlled by Internal or External Oscillator**
- **Integrated Output Recirculation Clamp Diodes**
- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Four Power MOSFET Outputs**
- **Integrated Snubbing Clamp Voltage at 40 V**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



description

The power logic 4-bit shift-register pulse-width-modulation (PWM) driver controls open-drain DMOS transistor outputs and is designed for applications that require relatively high power. The device contains a built-in snubbing clamp and recirculation clamp on the outputs for inductive transient protection and inductive energy recirculation, respectively. Power driver applications include solenoids and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent user-programmable PWM circuit that works in conjunction with the recirculation clamping diode in order to control the average current in inductive-load applications. The PWM circuit provides a programmable current-limit threshold that disables the output until the next rising edge of the independent PWM programmable clock.Each clock is generated from a user-programmable internal or external clock reference that in turn is programmed independently for each output through a frequency divide-by circuit.

TERMINAL NOMENCLATURE	
OSC/VER	Oscillator/Verify
DRAIN0 – DRAIN3	Drain Output
SER IN/A0	Serial Input/Address 0
SRCLR/A1	Shift Register Clear/Address 1
GND	Ground
G/A2	Output enable/Address 2
RCK/A3	Register clock/Address 3
SRCK/A4	Shift Register Clock/Address 4
V_{CC}	Logic Supply Voltage
DATA I/O	Program Data Input/Output
V_{PP}	Programming Supply Voltage
SER OUT	Serial Output
PGM	Program Enable
V_{DD}	Output Supply Voltage

User-programmable functions are controlled via 32 EEPROM bits. These bits are programmed by placing the TPIC6E585 into program mode by taking PGM high. The address to be programmed is then set up on dual functionality terminals A0–A4 (see Tables 1 and 2). The data bit to be programmed is set up on DATA I/O, and V_{PP} is then ramped from V_{CC} to V_{PPH} and back to V_{CC} to program the bit. The programming data can then be verified by taking VER high while monitoring DATA I/O, which gives the value of the data at the address selected on A0–A4. For each user-programmable parameter, Table 3 shows the binary programming values and the option selected by each programming value.

The core logic on this device contains a 4-bit serial-in, parallel-out shift register that feeds a 4-bit D-type register. When the shift register clear ($\overline{SRCLR}$) is high, data transfers through the shift register on the rising edge of the shift-register clock (SRCK). It is then transferred to the storage register on the rising edge of the register clock (RCK). When $\overline{SRCLR}$ is low, the shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

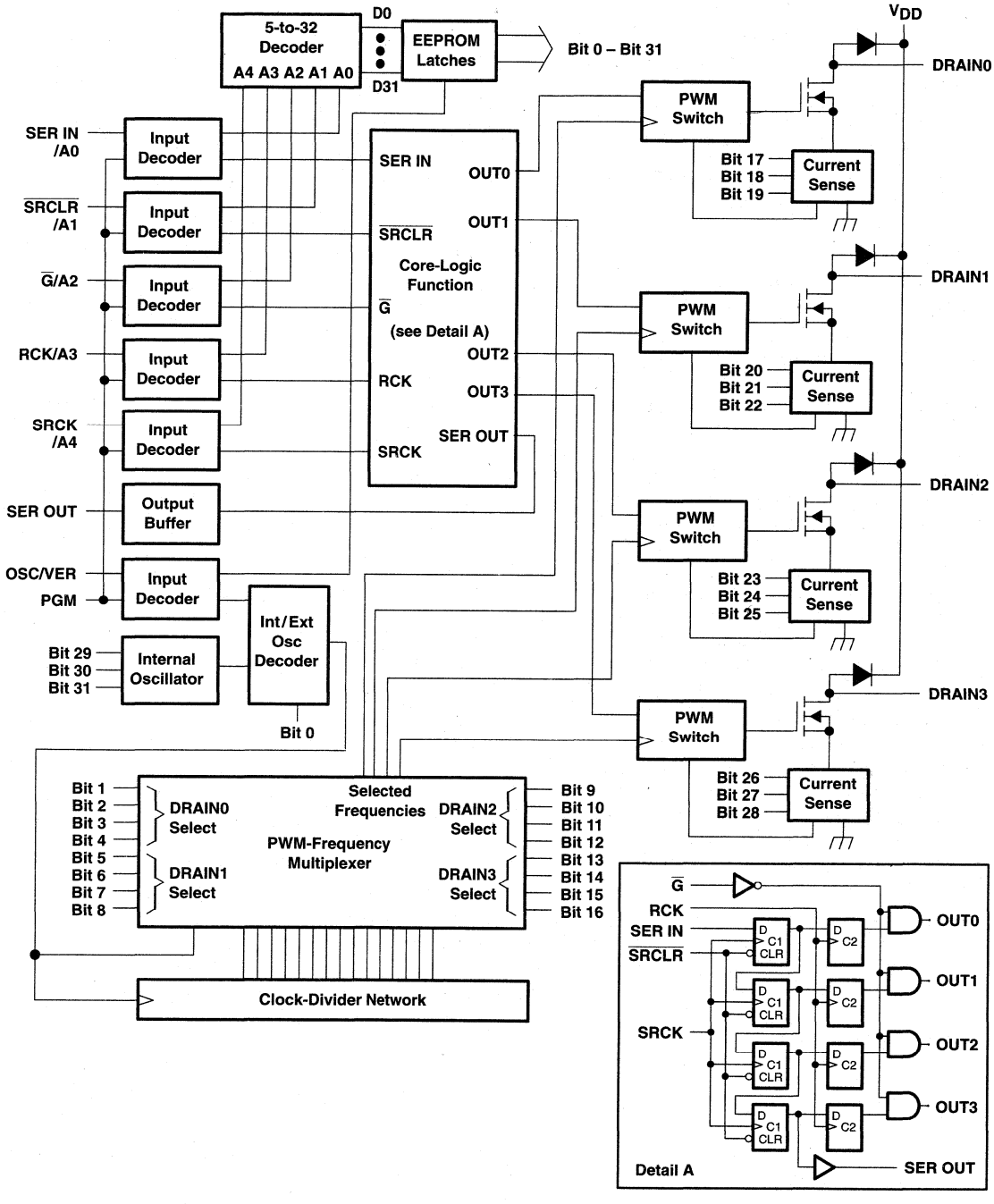
For proper operation, V_{DD} must be connected to a voltage source equal to or greater than the maximum drain voltage in the application.

The TPIC6E585 is offered in a 20-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the operating case temperature range of –40°C to 125°C.

PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram



TEXAS INSTRUMENTS
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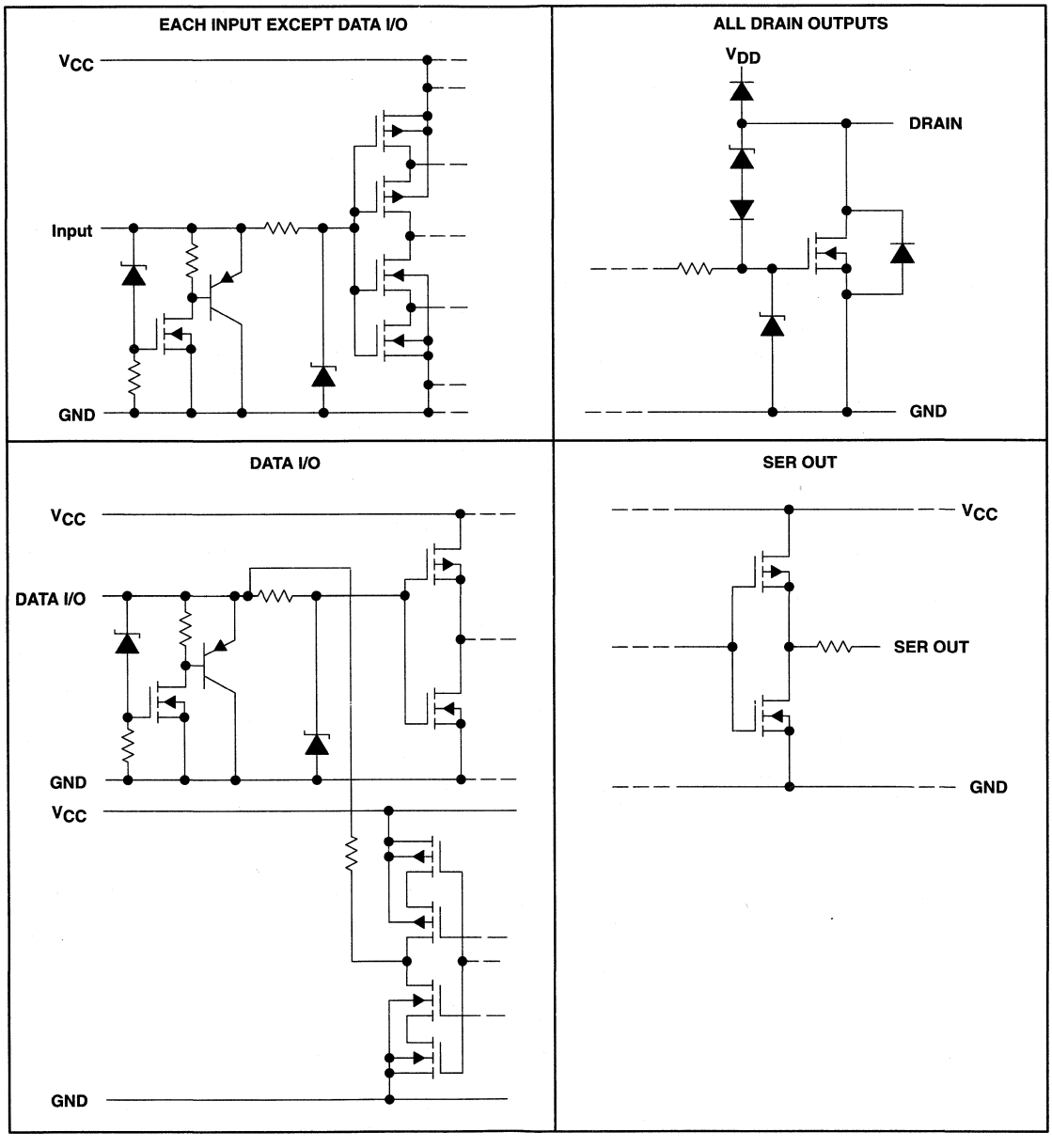
equivalent inputs and outputs



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DATA I/O	18	I/O	Programming data input/output
DRAIN0 DRAIN1 DRAIN2 DRAIN3	19 2 9 12	O	Drain outputs 0–3
$\overline{G}$/A2	7	I	Output Enable or Address 2
GND	5, 6, 15, 16	—	Ground
OSC/VER	1	I	Oscillator or Programming Verify
PGM	13	I	Program enable
RCK/A3	8	I	Register clock or Address 3
SER IN/A0	3	I	Serial input or Address 0
SER OUT	14	O	Serial out
$\overline{SRCLR}$/A1	4	I	Shift-register clear or Address 1
SRCK/A4	10	I	Shift-register clock or Address 4
V_{CC}	20	—	Logic supply voltage
V_{DD}	11	—	Output supply voltage
V_{PP}	17	—	Programming supply voltage

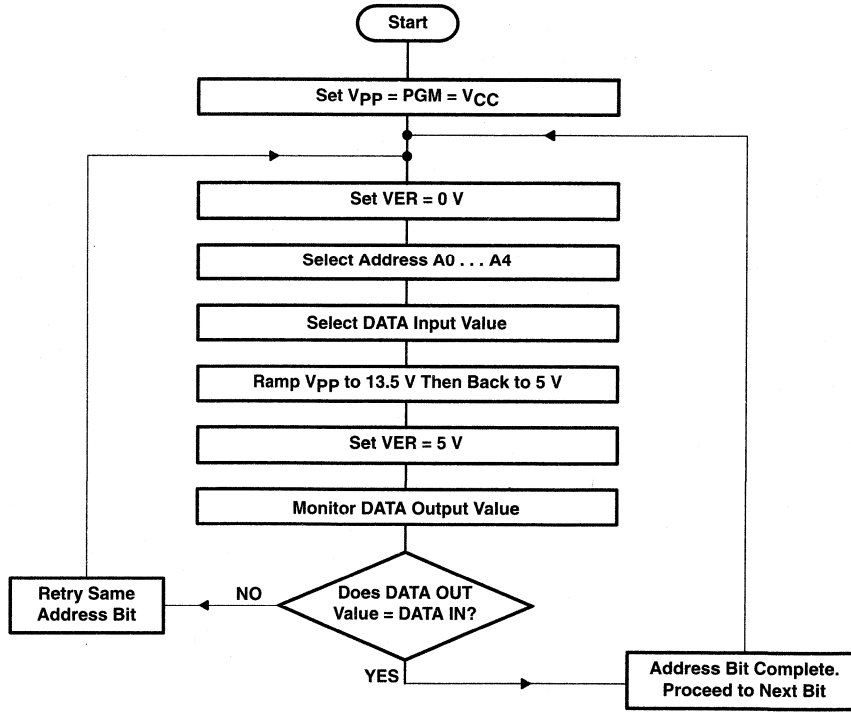


Figure 1. Recommended EEPROM Programming Sequence

Table 1. Function Selection for Dual-Functionality Terminals

TERMINAL NUMBER	NORMAL MODE (PGM = L)	PROGRAM MODE (PGM = H)
1	OSC	VER
3	SER IN	A0
4	$\overline{\text{SRCLR}}$	A1
7	$\overline{\text{G}}$	A2
8	RCK	A3
10	SRCK	A4

H = high level, L = low level

Table 2. EEPROM Bit Description

BIT NO.	BIT ADDRESS	USER-PROGRAMMABLE PARAMETER	DESCRIPTION†
0	00000	Internal/External Oscillator	Selects internal or external oscillator to be used for PWM clock
1 (LSB) 2 3 4 (MSB)	00001 00010 00011 00100	DRAIN0 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
5 (LSB) 6 7 8 (MSB)	00101 00110 00111 01000	DRAIN1 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
9 (LSB) 10 11 12 (MSB)	01001 01010 01011 01100	DRAIN2 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
13 (LSB) 14 15 16 (MSB)	01101 01110 01111 10000	DRAIN3 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
17 (LSB) 18 19 (MSB)	10001 10010 10011	DRAIN0 Current Sense Adjust	Selects the peak current for the PWM-chop mode
20 (LSB) 21 22 (MSB)	10100 10101 10110	DRAIN1 Current Sense Adjust	Selects the peak current for the PWM-chop mode
23 (LSB) 24 25 (MSB)	10111 11000 11001	DRAIN2 Current Sense Adjust	Selects the peak current for the PWM-chop mode
26 (LSB) 27 28 (MSB)	11010 11011 11100	DRAIN3 Current Sense Adjust	Selects the peak current for the PWM-chop mode
29 (LSB) 30 31 (MSB)	11101 11110 11111	Oscillator Frequency Adjust	Selects the frequency of the internal oscillator

† See Table 3

PRODUCT PREVIEW

Table 3. EEPROM Programming Values

PROGRAMMABLE PARAMETER	OPTION SELECTED	BINARY VALUE MSB< . . . > LSB
Internal/External Oscillator	Internal Oscillator	0
	External Oscillator	1
Frequency Multiplexer for All Drain Outputs	Oscillator ÷ 1	0000
	Oscillator ÷ 2	0001
	Oscillator ÷ 4	0010
	Oscillator ÷ 8	0011
	Oscillator ÷ 16	0100
	Oscillator ÷ 32	0101
	Oscillator ÷ 64	0110
	Oscillator ÷ 128	0111
	Oscillator ÷ 256	1000
	Oscillator ÷ 512	1001
	Oscillator ÷ 1024	1010
	Oscillator ÷ 2048	1011
	Oscillator ÷ 4096	1100
	Oscillator ÷ 8192	1101
	Oscillator ÷ 16384	1110
	Oscillator ÷ 32768	1111
Current Sense Adjust for All Drain Outputs	300 mA†	000
	400 mA†	001
	500 mA†	010
	600 mA†	011
	700 mA†	100
	800 mA†	101
	900 mA†	110
	1000 mA†	111
Oscillator Frequency Adjust	Internal Oscillator, Frequency = 1.2 MHz	000
	Internal Oscillator, Frequency = 1.1 MHz	001
	Internal Oscillator, Frequency = 0.9 MHz	010
	Internal Oscillator, Frequency = 0.8 MHz	011
	Internal Oscillator, Frequency = 0.6 MHz	100
	Internal Oscillator, Frequency = 0.5 MHz	101
	Internal Oscillator, Frequency = 0.3 MHz	110
	Internal Oscillator, Frequency = 0.1 MHz	111

† Current target ±20%

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) ..... 7 V
Logic input voltage range, V_I ..... −0.3 V to 7 V
Output supply voltage, V_{DD} (see Note 1) ..... 40 V
Programming supply voltage during programming, V_{PP} (see Notes 1 and 2) ..... 16 V
Programming supply voltage, verify/normal operation, V_{PP} ..... 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 3) ..... 40 V
Continuous source-to-drain diode current ..... 1 A
Pulsed source-to-drain diode current (see Note 3) ..... 1 A
PWM output current, each output, all outputs on, I_{Dn}, T_A = 25°C, d = 10%
(see Note 4 and Figure 10) ..... 900 mA
PWM output current, each output, all outputs on, I_{Dn}, T_A = 25°C, d = 50%
(see Note 4 and Figure 9) ..... 800 mA
Peak drain current, single output, I_{Dn}, T_A = 25°C (see Notes 3 and 4) ..... 1 A
Avalanche current, I_{AS} (see Note 5 and Figure 7) ..... 1 A
Single-pulse avalanche energy, E_{AS} (see Note 5 and Figure 7) ..... 100 mJ
Continuous total dissipation ..... See Dissipation Rating Table
Operating case temperature range, T_C ..... −40°C to 125°C
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. For programming waveform, see Figure 2.
3. Each power DMOS source is internally connected to GND. Pulse duration ≤100 µs, duty cycle ≤ 2%.
4. Depends upon program current-sense adjust and load conditions.
5. V_{supply} = 24 V, starting junction temperature, (T_{JS}) = 25°C, L = 87 mH, I_{AS} = 1 A.

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
NE	2775 mW	20 mW/°C	555 mW
NE on FR-4 PCB	4163 mW	33.3 mW/°C	833 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
Output supply voltage, V_{DD}		40	V
Programming supply voltage during programming, V_{PP}	12	15	V
Programming supply voltage during verify or normal operation, V_{PP}	V_{CC}−0.7	V_{CC}	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Operating case temperature, T_C	−40	125	°C

PRODUCT PREVIEW

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electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA			40			V
V_{SD}	Source-drain diode forward voltage	I_F = 1 A				1	1.5	V
$V_{OH(SER\ OUT)}$	High-level output voltage	I_{OH} = −20 µA,	V_{CC} = 4.5 V		4.4	4.45		V
		I_{OH} = −4 mA,	V_{CC} = 4.5 V		4	4.2		
$V_{OL(SER\ OUT)}$	Low-level output voltage	I_{OL} = 20 µA,	V_{CC} = 4.5 V			20	100	mV
		I_{OL} = 4 mA,	V_{CC} = 4.5 V			300	600	
$V_{OH(DATA\ I/O)}$	High-level data output voltage	I_{OH} = −100 µA,	V_{CC} = 4.5 V		4.25	4.48		V
$V_{OL(DATA\ I/O)}$	Low-level data output voltage	I_{OL} = 100 µA,	V_{CC} = 4.5 V			200	250	mV
V_f	Forward clamp voltage	I_f = 1 A				1.35	2	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0,	All inputs low			1.6	5	mA
$I_{CC(freq)}$	Logic supply current at frequency	SRCK = 5 MHz,	I_O = 0			5.5		mA
I_{DSX}	Off-state drain current	V_{DD} = 40 V,	V_{DS} = 35 V			0.2	1	µA
		V_{DD} = 40 V,	V_{DS} = 30 V,	T_C = 125°C		1	5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 200 mA,	V_{CC} = 4.5 V			1	1.5	Ω
		I_D = 200 mA,	V_{CC} = 4.5 V,	T_C = 125°C		1.6	2.4	
		I_D = 750 mA,	V_{CC} = 4.5 V			1.1	1.75	

timing requirements over recommended ranges of supply voltage and operating case temperature

		MIN	MAX	UNIT
t_{su}	Setup time, SER IN high before SRCK↑ (see Figure 5)	20		ns
t_{su1}	Setup time, VER to PGM (see Figure 2)	2		µs
t_{su2}	Setup time, address and DATA I/O to V_{PP} (see Figure 2)	2		µs
t_{su3}	Setup time, PGM to DATA I/O (see Figure 2)	2		µs
t_{su4}	Setup time, PGM to address (see Figure 2)	2		µs
t_h	Hold time, SER IN high before SRCK↑ (see Figure 5)	20		ns
t_{h1}	PGM hold time, DATA I/O (see Figure 2)	2		µs
t_{h2}	Hold time, DATA I/O after V_{PP} (see Figure 2)	2		µs
t_w	Pulse duration (see Figure 5)	40		ns
t_{w1}	Pulse duration, V_{PP} program (see Figure 2)	5		ms
t_{pd}	Propagation delay, VER to DATA I/O (see Figure 2)	2		µs
t_r	Rise time, V_{PP} during programming (see Figure 2)	2	3	ms
t_f	Fall time, V_{PP} during programming (see Figure 2)	2	3	ms

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, See Figure 5	I_D = 250 mA,		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$				150		ns
t_{r1}	Rise time, drain output (see Figure 5)				750		ns
t_{f1}	Fall time, drain output (see Figure 5)				425		ns
t_{rr}	Reverse-recovery time (see Figure 6)	I_F = 250 mA,	di/dt = 40 A/µs		300		ns
t_{rra}	Reverse-recovery current rise time (see Figure 6)				100		ns

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All four outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All four outputs with equal power		50	°C/W

PARAMETER MEASUREMENT INFORMATION

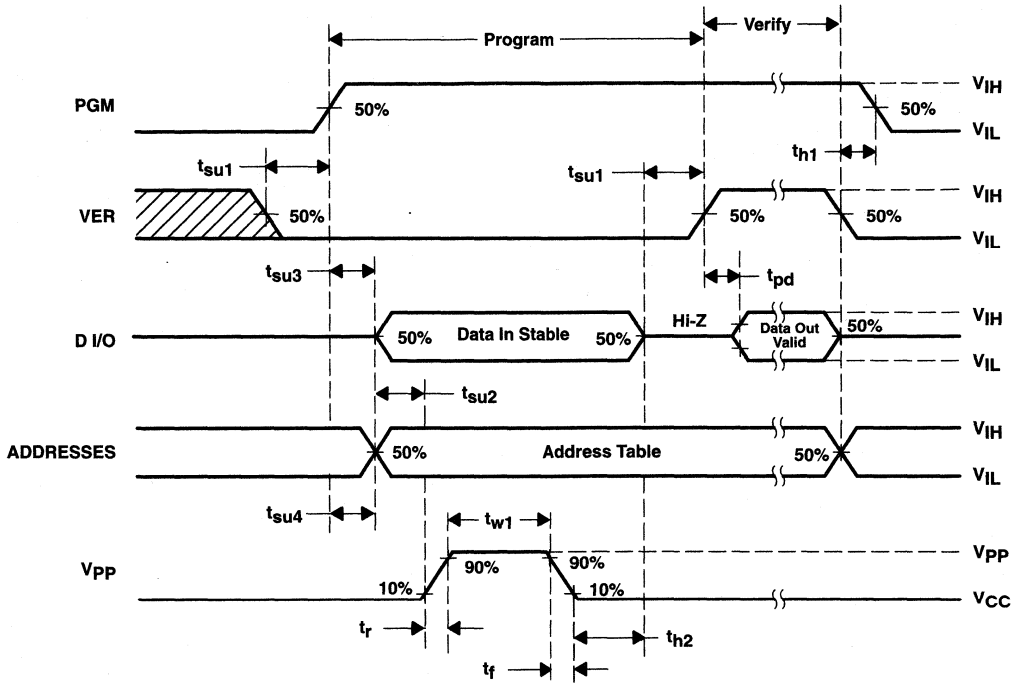


Figure 2. Programming Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

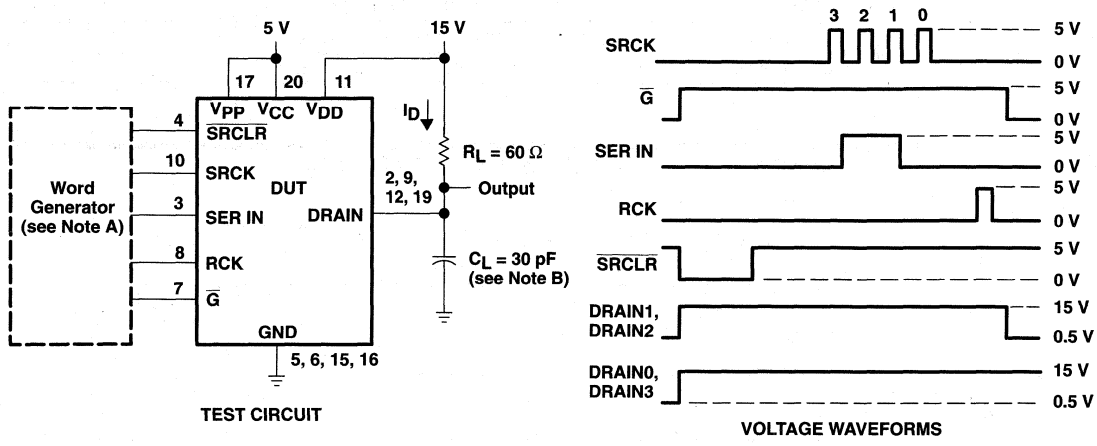


Figure 3. Resistive Load Operation

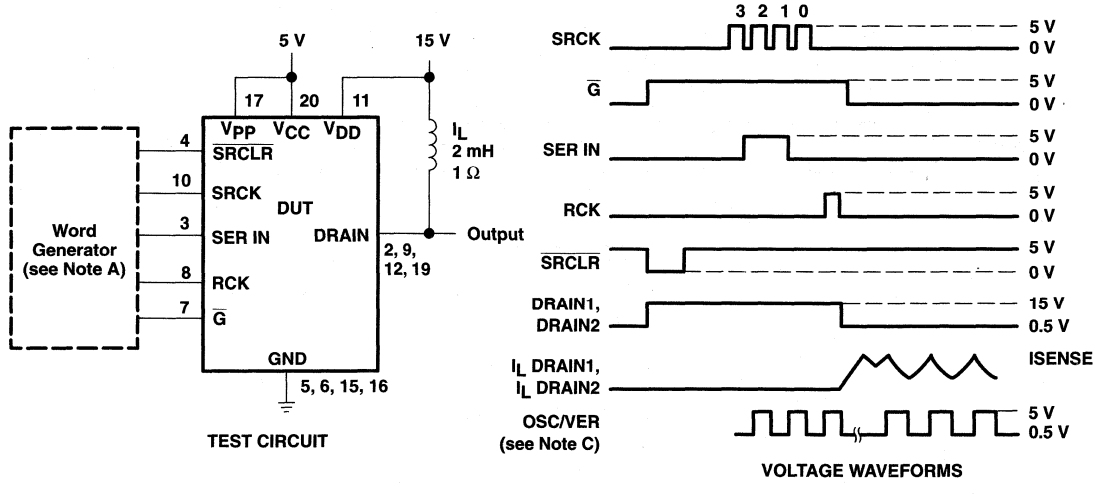
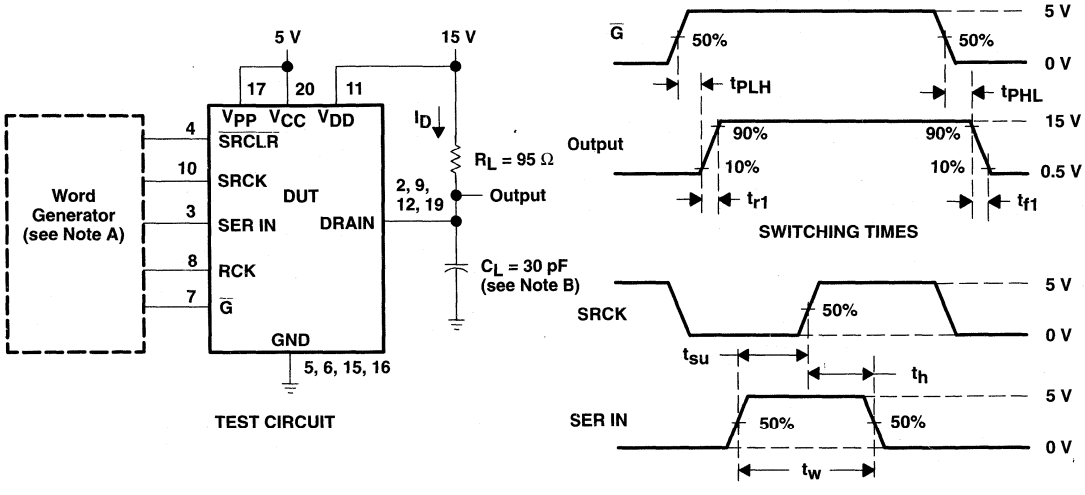


Figure 4. Inductor Load Operation

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. DRAIN0 and DRAIN3 remain at 0$_A$ I_L.

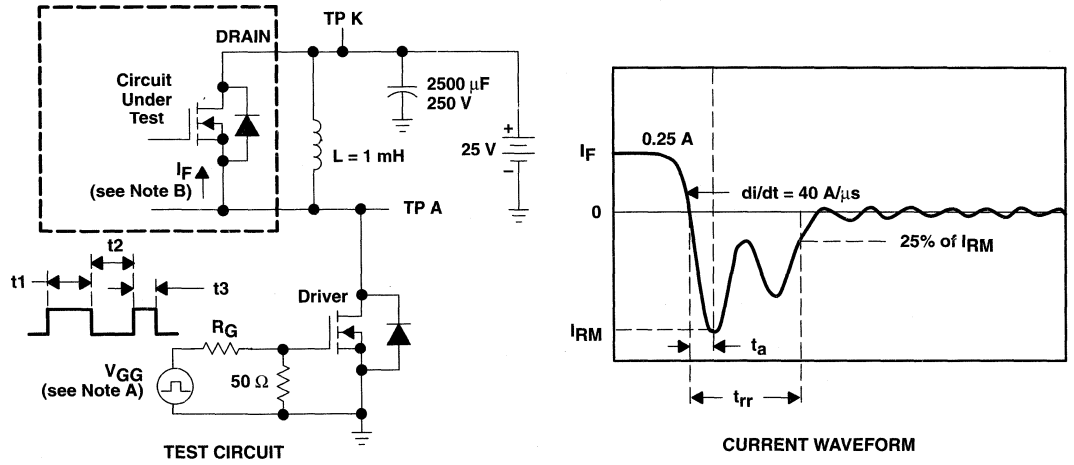
PRODUCT PREVIEW

PARAMETER MEASUREMENT



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 5. Test Circuit and Voltage Waveforms, Switching Times

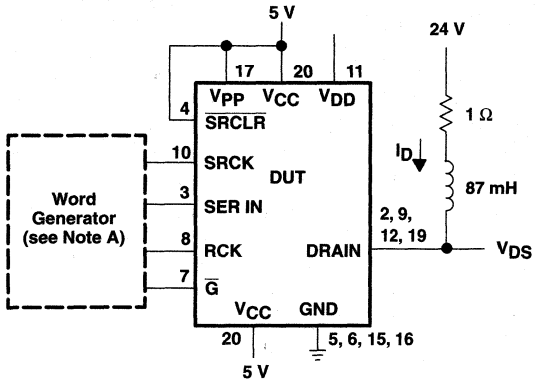


NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 40 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t1 = 15 µs, t2 = 8.5 µs, and t3 = 3.5 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

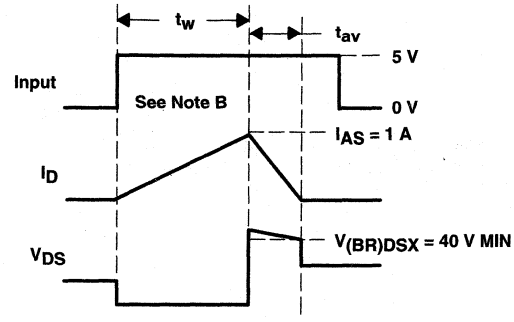
Figure 6. Reverse-Recovery-Current Test Circuit and Waveform of Source Drive Device

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE-ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is controlled by the value of peak current $I_{AS} = 1$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 100$ mJ,

where t_{av} = avalanche time.

Figure 7. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

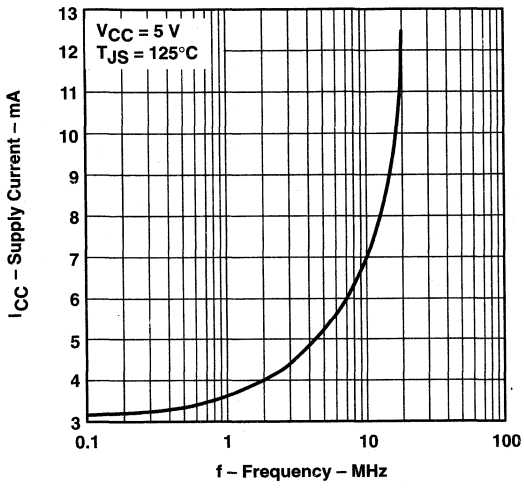


Figure 8

MAXIMUM PWM CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

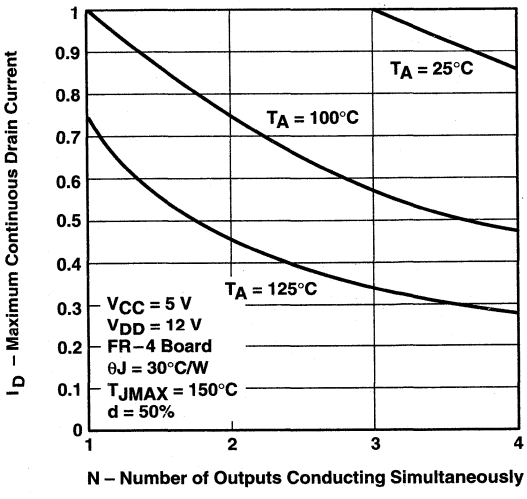


Figure 9

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

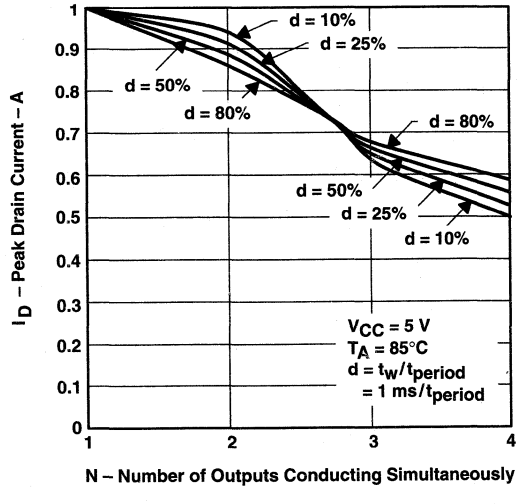


Figure 10

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

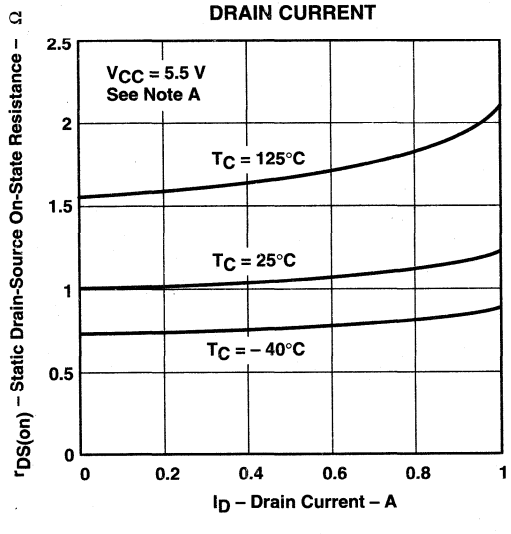


Figure 11

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE
ON-STATE RESISTANCE
vs
LOGIC SUPPLY VOLTAGE

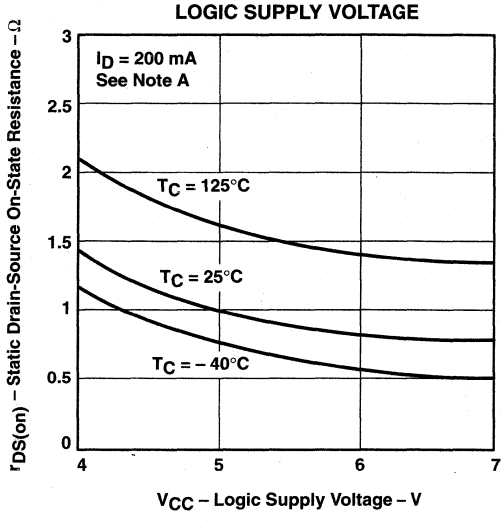


Figure 12

SWITCHING TIME
vs
FREE-AIR TEMPERATURE

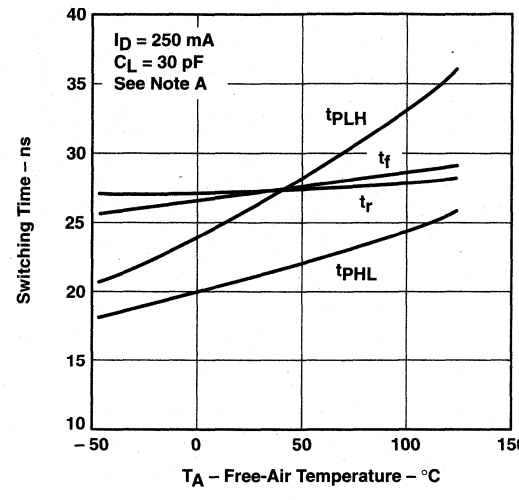


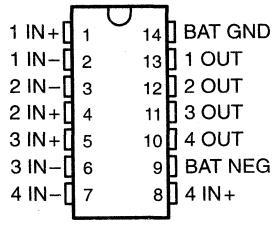
Figure 13

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

3 Peripheral Drivers/Actuators

- **Designed for –52-V Battery Operation**
- **50-mA Output Current Capability**
- **Input Compatible With TTL and CMOS**
- **High Common-Mode Input Voltage Range**
- **Very Low Input Current**
- **Fail-Safe Disconnect Feature**
- **Built-in Output Clamp Diode**
- **Direct Replacement for National DS3680 and Fairchild μA3680**

D OR N PACKAGE
(TOP VIEW)

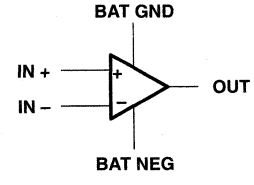


description

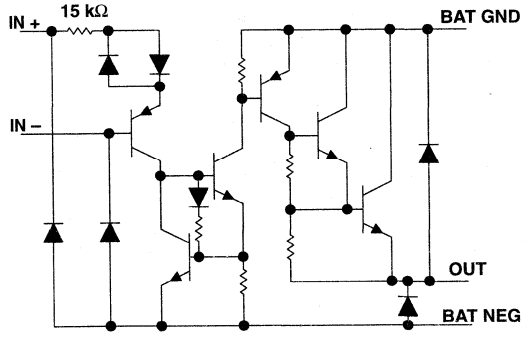
The DS3680 telephone relay driver is a monolithic integrated circuit designed to interface –48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard –52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output is off as a fail-safe condition when either output is open.

The DS3680 is characterized for operation from 0°C to 70°C.

symbol (each driver)



schematic diagram (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{BAT-} (see Note 1) ..... −70 V to 0.5 V
Input voltage range with respect to BAT GND ..... −70 V to 20 V
Input voltage range with respect to BAT NEG ..... −0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) ..... ±20 V
Output current, I_O: Resistive load ..... −100 mA
Inductive load ..... −50 mA
Inductive output load ..... 5 H
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds ..... 260°C

NOTES: 1. All voltages are with respect to BAT GND, unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{BAT-}	−10	−60	V
Input voltage, either input	−20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	−20†	0.8	V
Operating free-air temperature, T_A	0	70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{BAT-} = −52 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	V_{ID} = 2 V			40	100	µA
		V_{ID} = 7 V			375	1000	
I_{IL}	Low-level input current (into IN+)	V_{ID} = 0.4 V			0.01	5	µA
		V_{ID} = −7 V			−1	−100	
$V_{O(on)}$	On-stage output voltage	I_O = 50 mA,	V_{ID} = 2 V		−1.6	−2.1	V
$I_{O(off)}$	Off-stage output current	$V_O = V_{BAT-}$	V_{ID} = 0.8 V		−2	−100	µA
			Inputs open		−2	−100	
I_R	Clamp diode reverse current	V_O = 0			2	100	µA
V_{OK}	Output clamp voltage	I_O = 50 mA			0.9	1.2	V
		I_O = −50 mA,	V_{BAT-} = 0		−0.9	−1.2	
$I_{BAT(on)}$	On-state battery current	All drivers on			−2	−4.4	mA
$I_{BAT(off)}$	Off-state battery current	All drivers off			−1	−100	µA

‡ All typical values are at T_A = 25°C.

switching characteristics V_{BAT-} = –52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse, R_L = 1 kΩ, L = 1 H, See Figure 2		1	10	μs
t_{off}	Turn-off time			1	10	μs

PARAMETER MEASUREMENT INFORMATION

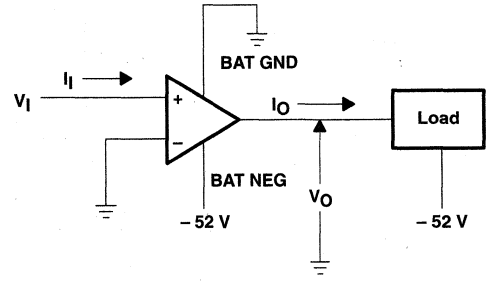


Figure 1. Generalized Test Circuit, Each Driver

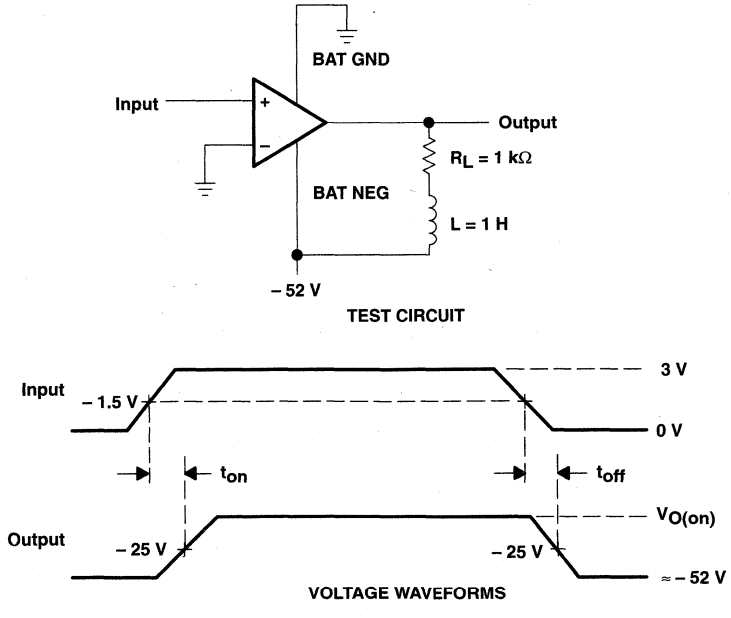


Figure 2. Test Circuit and Voltage Waveforms, Each Driver

APPLICATION INFORMATION

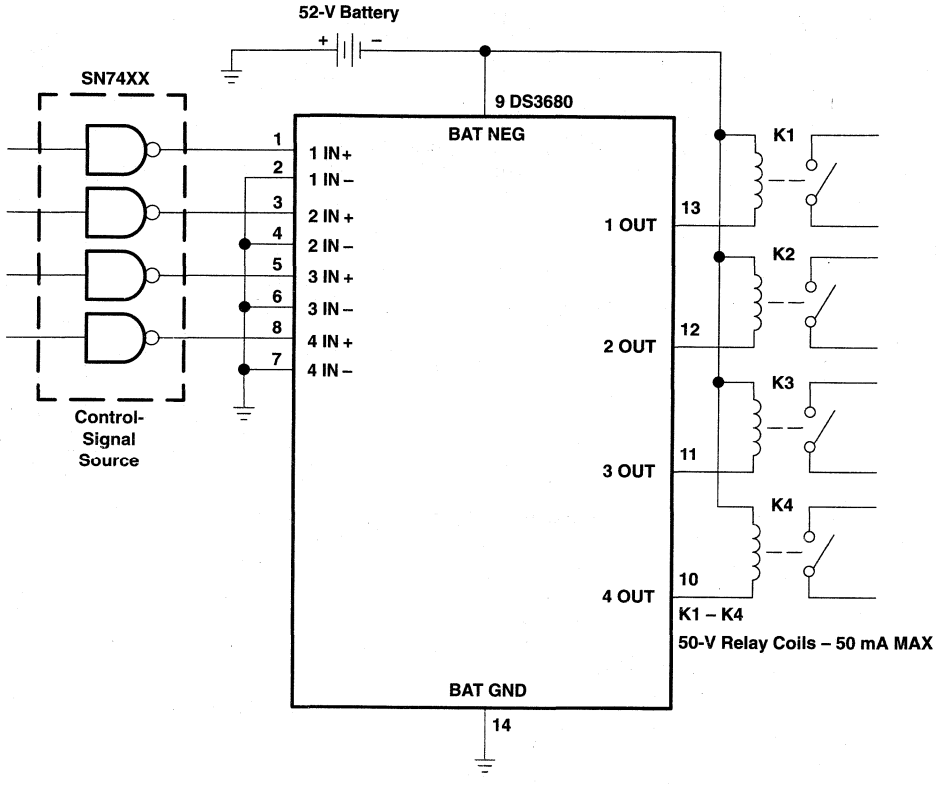


Figure 3. Relay Driver

SLRS005 – SEPTEMBER 1986 – REVISED MAY 1990

- **1-A Output Current Capability Per Driver**
- **Pulsed Current 2-A Driver**
- **Wide Supply Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **NE Package Designed for Heat Sinking**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **High-Noise-Immunity Inputs**
- **Functional Replacement for SGS L293**

description

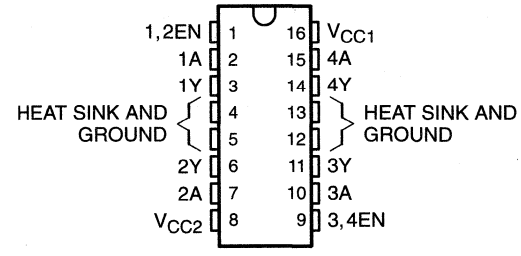
The L293 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

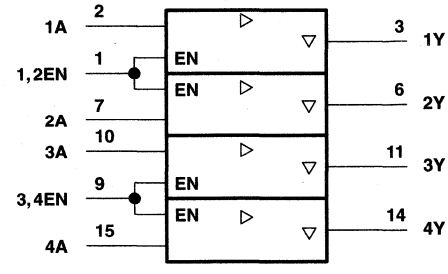
External high-speed output clamp diodes should be used for inductive transient suppression. A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

The L293 is designed for operation from 0°C to 70°C.

NE PACKAGE
(TOP VIEW)

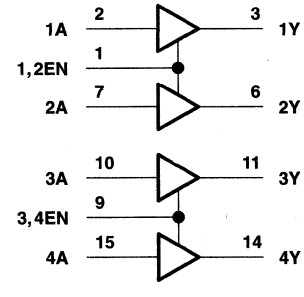


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram

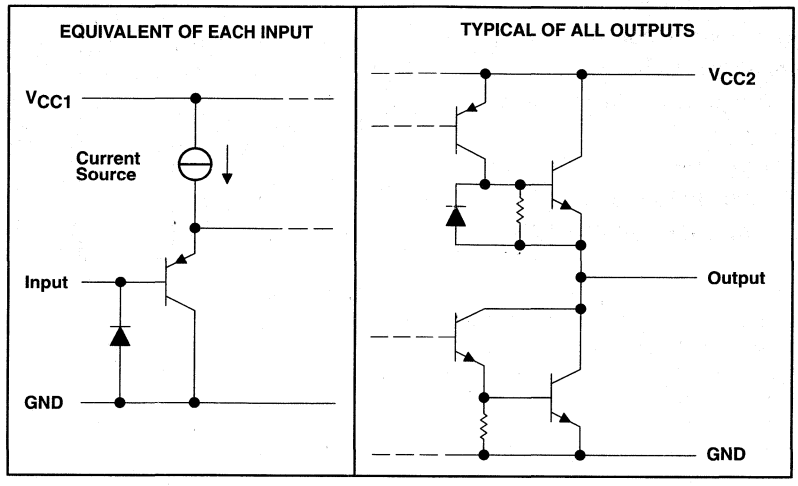


FUNCTION TABLE
(each driver)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level,
X = irrelevant, Z = high-impedance (off)
‡ In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 36 V
Output supply voltage range, V_{CC2} . . . . . 36 V
Input voltage range, V_I . . . . . 7 V
Output voltage range, V_O . . . . . -3 V to $V_{CC2} + 3$ V
Peak output current, I_O (nonrepetitive, $t \leq 5$ ms) . . . . . ± 2 A
Continuous output current, I_O . . . . . ± 1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) . . . . . 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range, T_A . . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}			36	V
High-level input voltage, V_{IH}	$V_{CC1} \leq 7$ V	2.3		V
	$V_{CC1} \geq 7$ V	2.3	7	
Low-level output voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

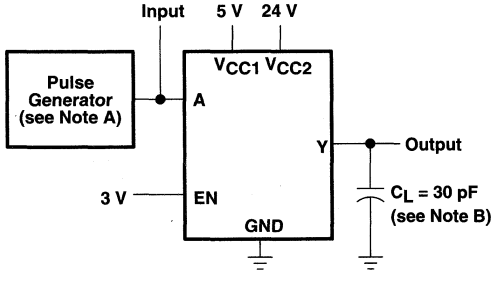
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 1 A			1.2	1.8	V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	µA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	µA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

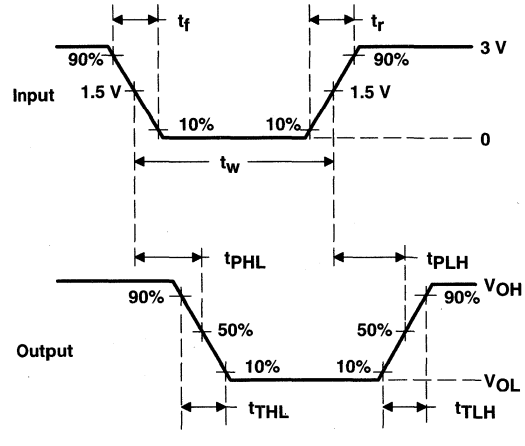
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 10 µs, PRR = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

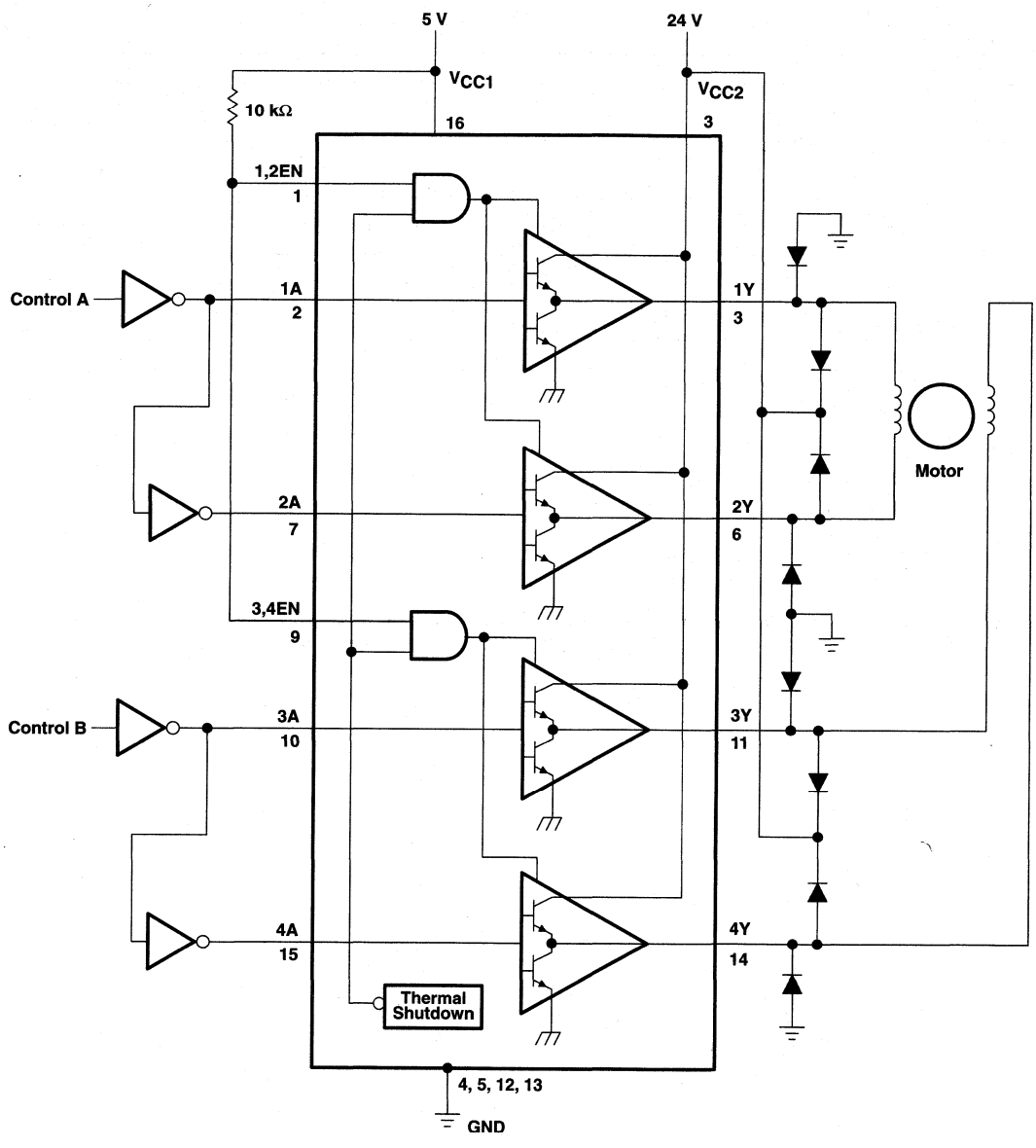
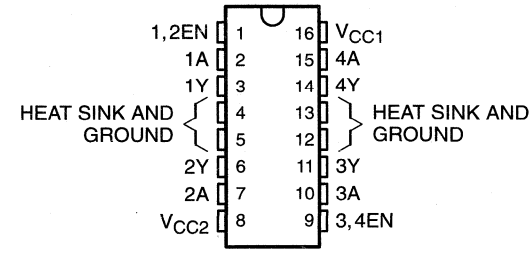


Figure 2. Two-Phase Motor Driver

- **600-mA Output Current Capability Per Driver**
- **Pulsed Current 1.2-A Per Driver**
- **Output Clamp Diodes for Inductive Transient Suppression**
- **Wide Supply Voltage Range 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **High-Noise-Immunity Inputs**
- **Functional Replacement for SGS L293D**

NE PACKAGE
(TOP VIEW)



description

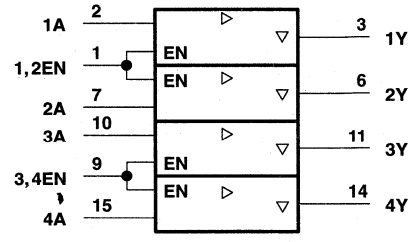
The L293D is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs are active and in phase with their inputs. External high-speed output clamp diodes should be used for inductive transient suppression. When the enable input is low, those drivers are disabled, and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

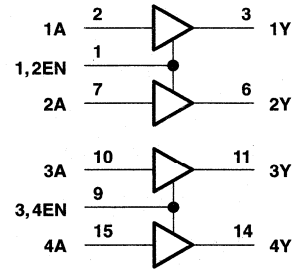
The L293D is designed for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

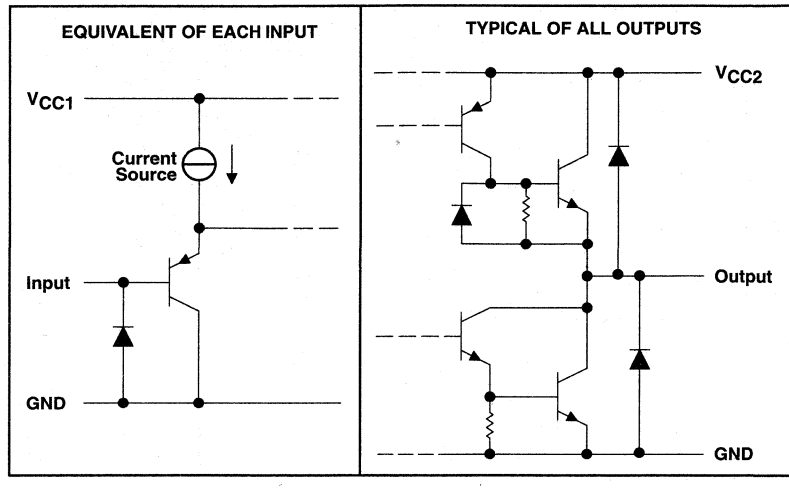


FUNCTION TABLE
(each driver)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low level,
X = irrelevant, Z = high-impedance (off)
‡ In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) ..... 36 V
Output supply voltage range, V_{CC2} ..... 36 V
Input voltage range, V_I ..... 7 V
Output voltage range, V_O ..... −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, t ≤ 100 µs) ..... ±1.2 A
Continuous output current, I_O ..... ±600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) ..... 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) ..... 5000 mW
Operating case or virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		V_{CC1}	36	V
High-level input voltage, V_{IH}	$V_{CC1} \leq 7$ V	2.3	V_{CC1}	V
	$V_{CC1} \geq 7$ V	2.3	7	
Low-level input voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

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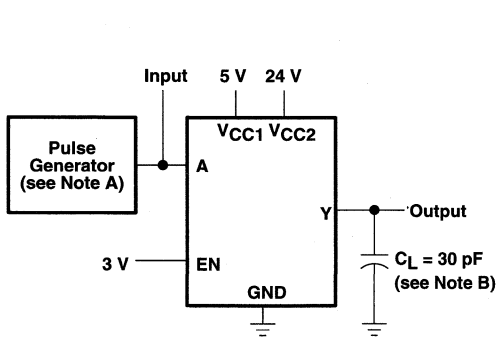
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −0.6 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		I_{OK} = −0.6 A			V_{CC2}+1.3		V
V_{OKL}	Low-level output clamp voltage		I_{OK} = −0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	µA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	µA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

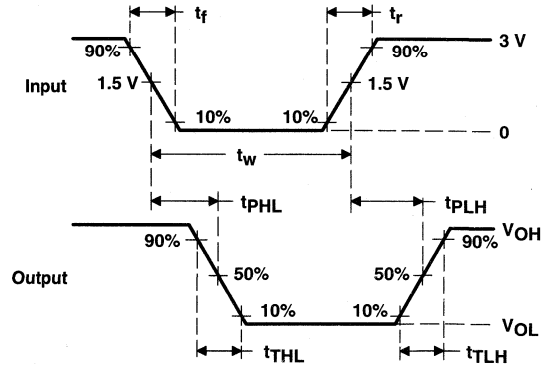
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 10 µs, PRR = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

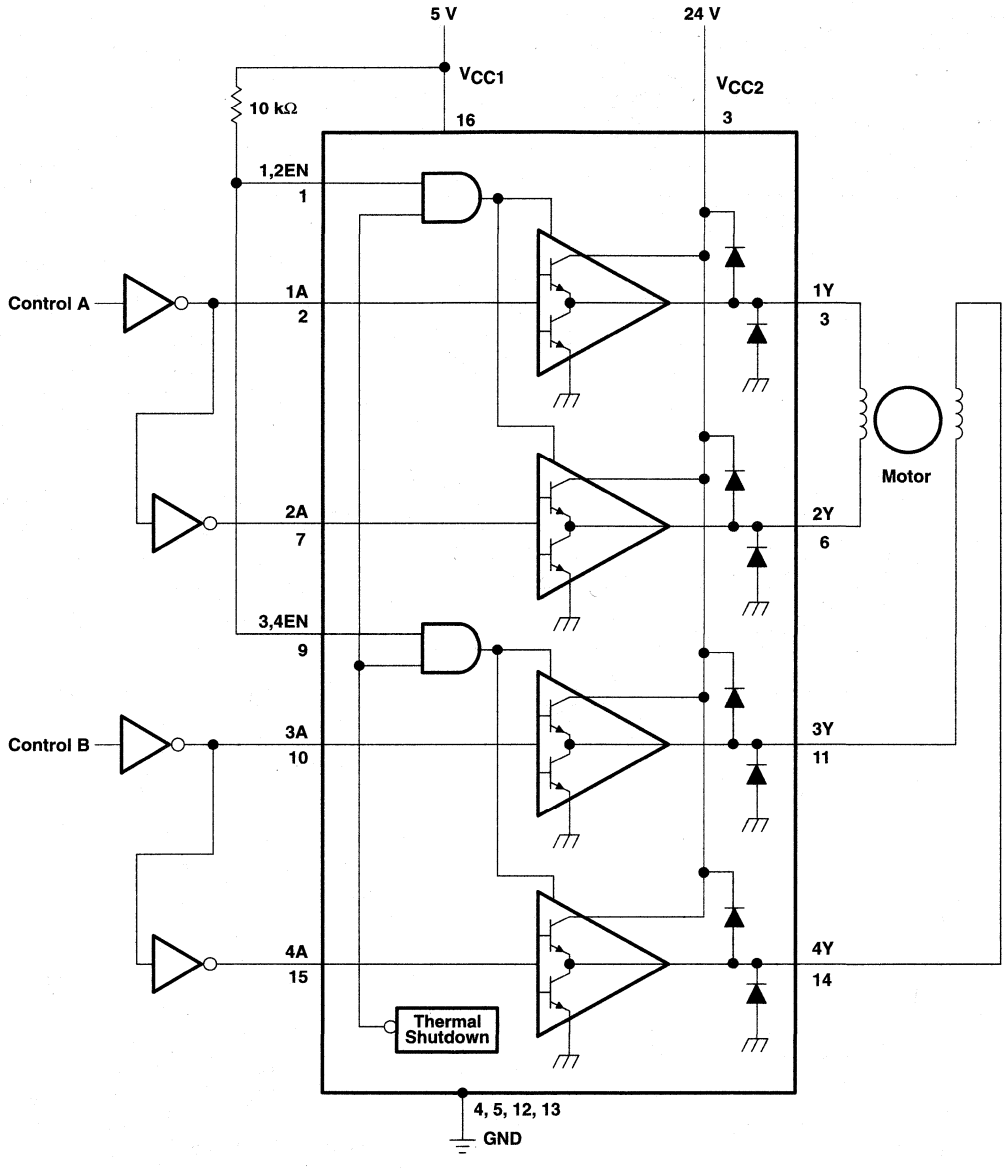


Figure 2. Two-Phase Motor Driver

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

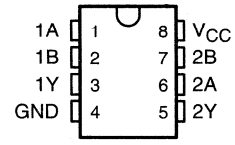
- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 20 V (After Conducting 300 mA)**
- **High-Speed Switching**
- **Circuit Flexibility for Varied Applications**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SUMMARY OF DEVICES

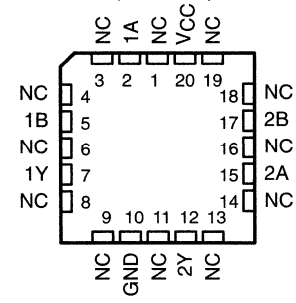
DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55451B	AND†	FK, JG
SN55452B	NAND	JG
SN55453B	OR	FK, JG
SN55454B	NOR	JG
SN75451B	AND	D, P
SN75452B	NAND	D, P
SN75453B	OR	D, P
SN75454B	NOR	D, P

† With output transistor base connected externally to output of gate

SN55451B, SN55452B, SN55453B, SN55454B . . . JG PACKAGE
SN75451B, SN75452B, SN75453B, SN75454B . . . D OR P PACKAGE
(TOP VIEW)



SN55451B, SN55452B
SN55453B, SN55454B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55451B through SN55454B and SN75451B through SN75454B are dual peripheral drivers designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the devices is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

The SN55' drivers are characterized for operation over the full military range of −55°C to 125°C. The SN75' drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I		5.5	5.5	V
Inter-emitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage, V_O		30	30	V
Continuous collector or output current, I_{OK} (see Note 3)		400	400	mA
Peak collector or output current, I_I ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to network GND, unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

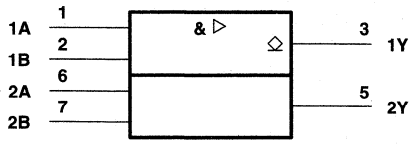
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

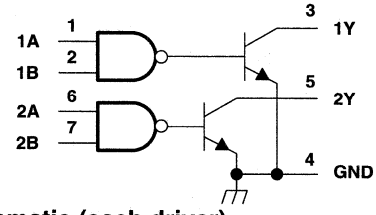
Pin numbers shown are for the D, JG, and P packages.

FUNCTION TABLE (each driver)

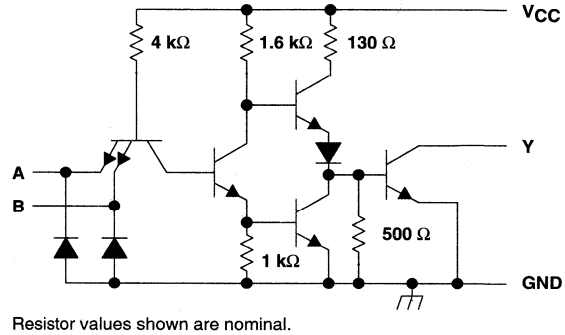
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
$Y = AB$ or $\overline{\overline{A}+\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

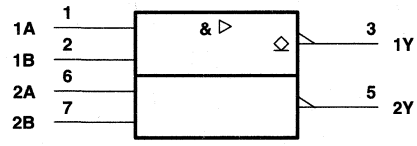
PARAMETER		TEST CONDITIONS‡	SN55451B			SN75451B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		52	65		52	65	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				18	25	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55451B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2		V_S−6.5		mV
		SN75451B			V_S−6.5		

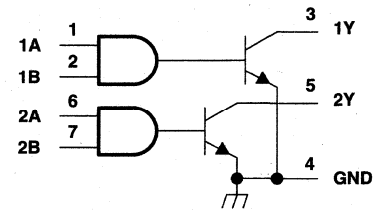
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

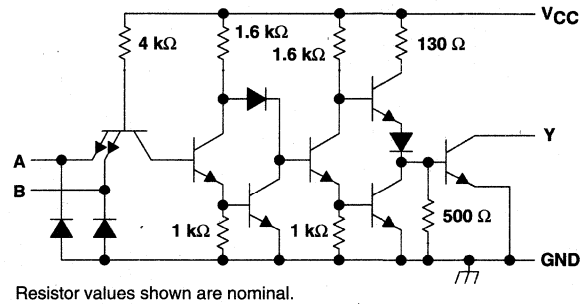


FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A}+\overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

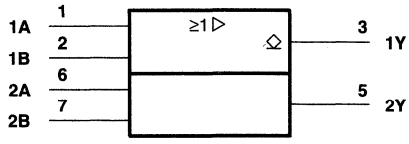
PARAMETER		TEST CONDITIONS‡	SN55452B			SN75452B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		11	14		11	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		56	71		56	71	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

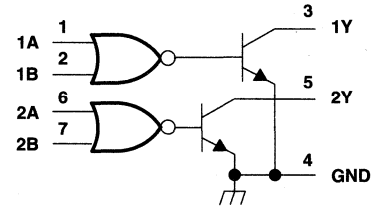
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55452B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2		V_S−6.5		mV
		SN75452B			V_S−6.5		

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

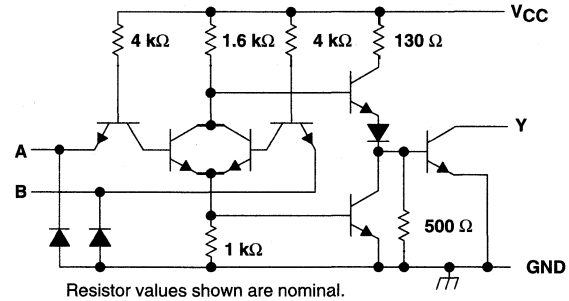


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic: $Y = A+B$ or $\overline{A}\,\overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

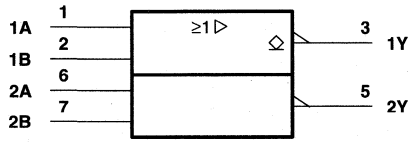
PARAMETER		TEST CONDITIONS‡	SN55453B			SN75453B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		54	68		54	68	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

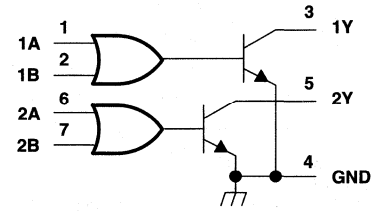
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output					18	25	
t_{TLH}	Transition time, low-to-high-level output					5	8	
t_{THL}	Transition time, high-to-low-level output					7	12	
V_{OH}	High-level output voltage after switching	SN55453B	V_S = 20 V, See Figure 2	$I_O \approx$ 300 mA,	V_S−6.5			mV
		SN75453B			V_S−6.5			

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

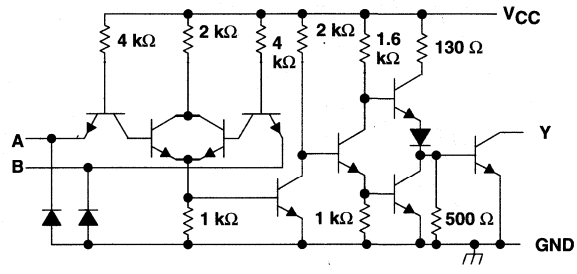


FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
$Y = \overline{A+B}$ or $\overline{AB}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

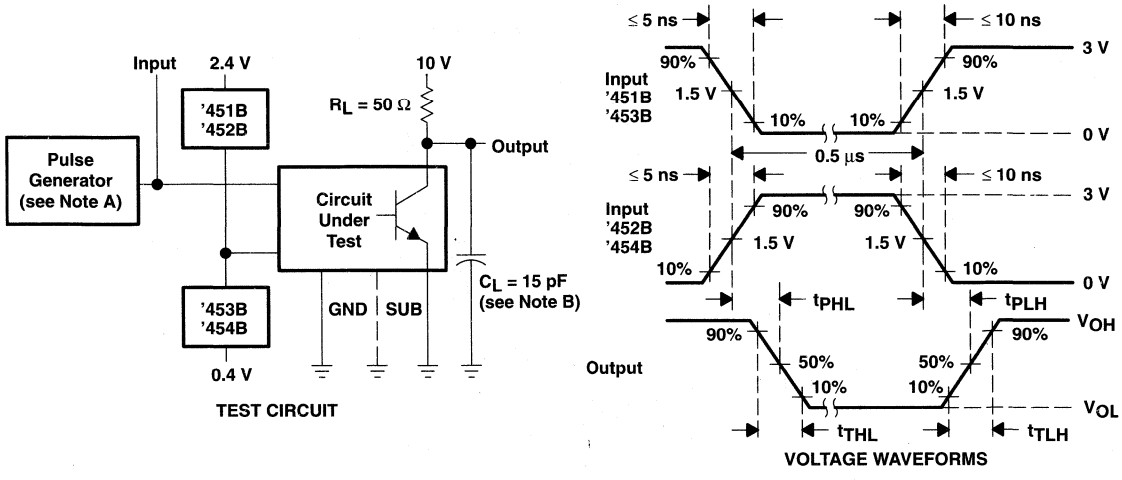
PARAMETER		TEST CONDITIONS‡	SN55454B			SN75454B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	79		61	79	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

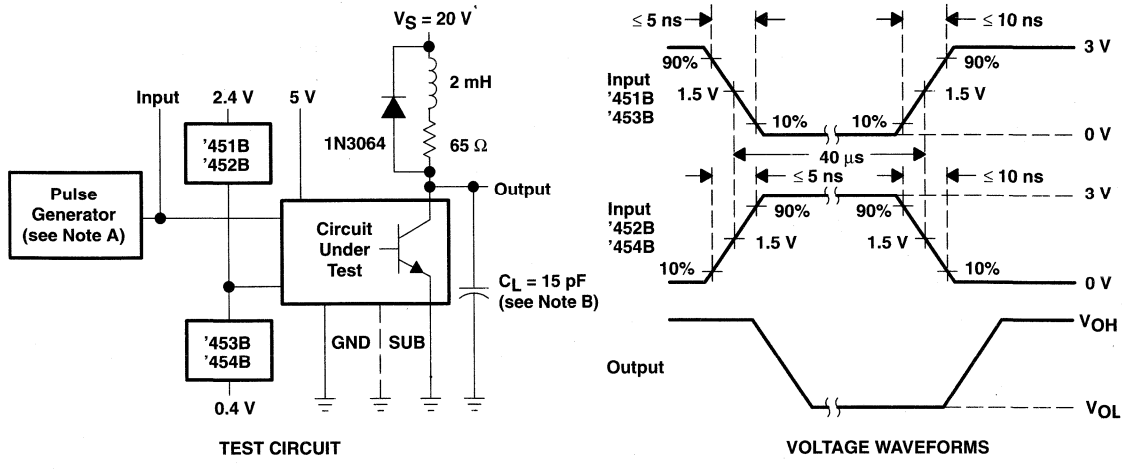
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55454B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2		V_S−6.5		mV
		SN75454B			V_S−6.5		

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

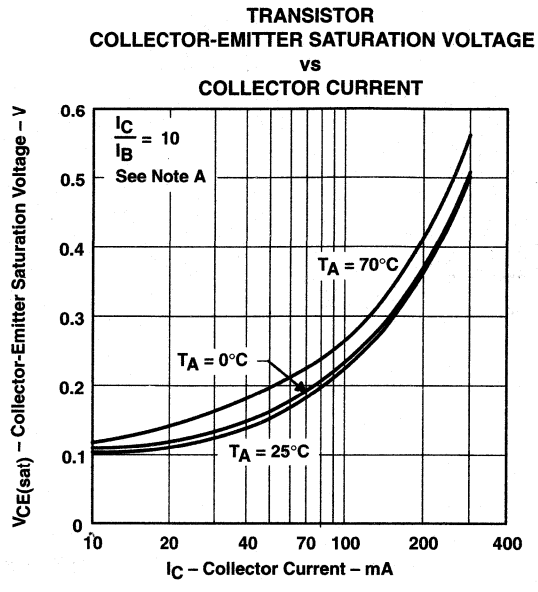
Figure 1. Test Circuit and Voltage Waveforms, Complete Drivers



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test of Complete Drivers

TYPICAL CHARACTERISTICS



NOTE A: These parameters must be measured using pulse techniques, t_w = 300 µs, duty cycle ≤ 2%.

Figure 3

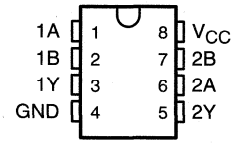
PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 30 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame for Cooler Operation and Improved Reliability**
- **Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

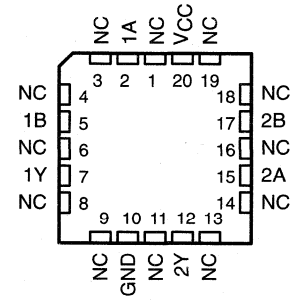
SUMMARY OF SERIES 55461/75461

DEVICE	LOGIC	PACKAGES
SN55461	AND	FK, JG
SN55462	NAND	FK, JG
SN55463	OR	FK, JG
SN75461	AND	D, P
SN75462	NAND	D, P
SN75463	OR	D, P

SN55461, SN55462, SN55463 . . . JG PACKAGE
SN75461, SN75462, SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462, SN55463 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55453B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, and SN55463/SN75463 are dual peripheral AND, NAND, and OR drivers respectively (assuming positive logic), with the output of the gates internally connected to the bases of the npn output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of −55°C to 125°C. Series SN75461 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I		5.5	5.5	V
Intermitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage, V_O		35	35	V
Continuous collector or output current (see Note 3)		400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds, T_C	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network GND unless otherwise specified.
2. This is the voltage between two emitters A and B.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

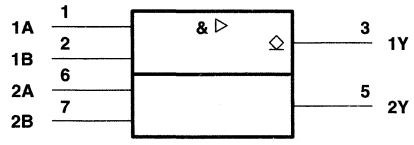
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	–

recommended operating conditions

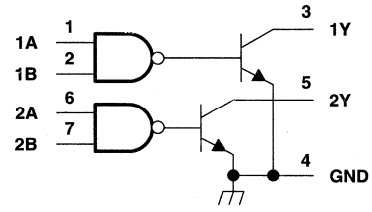
	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

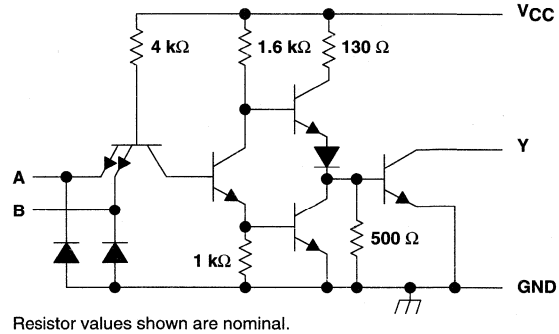


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic: $Y = AB$ or $\overline{\overline{A} + \overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

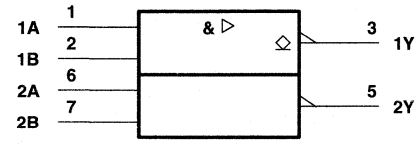
PARAMETER		TEST CONDITIONS†	SN55461			SN75461			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

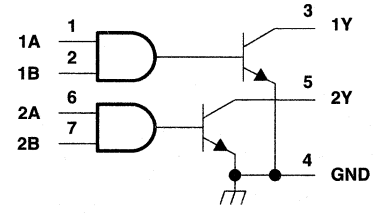
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	
t_{TLH}	Transition time, low-to-high-level output				8	20	
t_{THL}	Transition time, high-to-low-level output				10	20	
V_{OH}	High-level output voltage after switching	SN55461	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 2		V_S−10		mV
		SN75461			V_S−10		

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

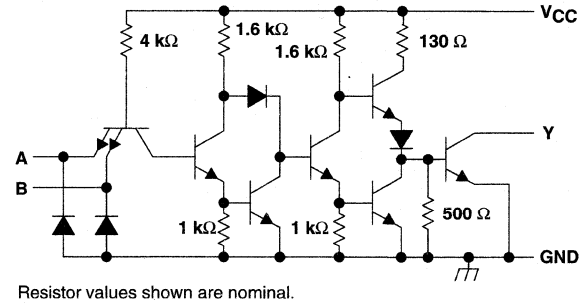


FUNCTION TABLE
(each driver)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

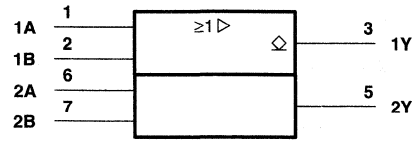
PARAMETER		TEST CONDITIONS†	SN55462			SN75462			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	76		61	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

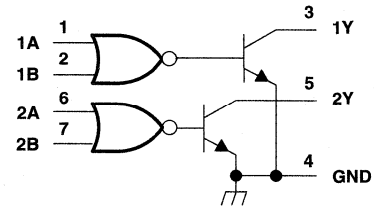
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	
t_{TLH}	Transition time, low-to-high-level output				13	25	
t_{THL}	Transition time, high-to-low-level output				10	20	
V_{OH}	High-level output voltage after switching	SN55462	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 2	V_S−10			mV
		SN75462		V_S−10			

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

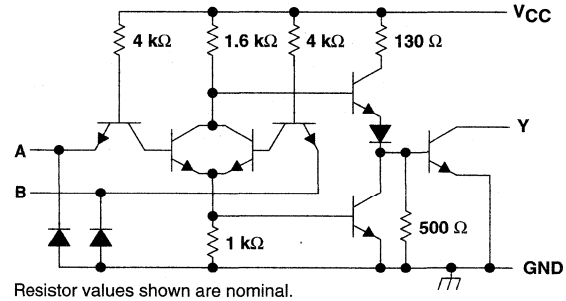


FUNCTION TABLE (each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

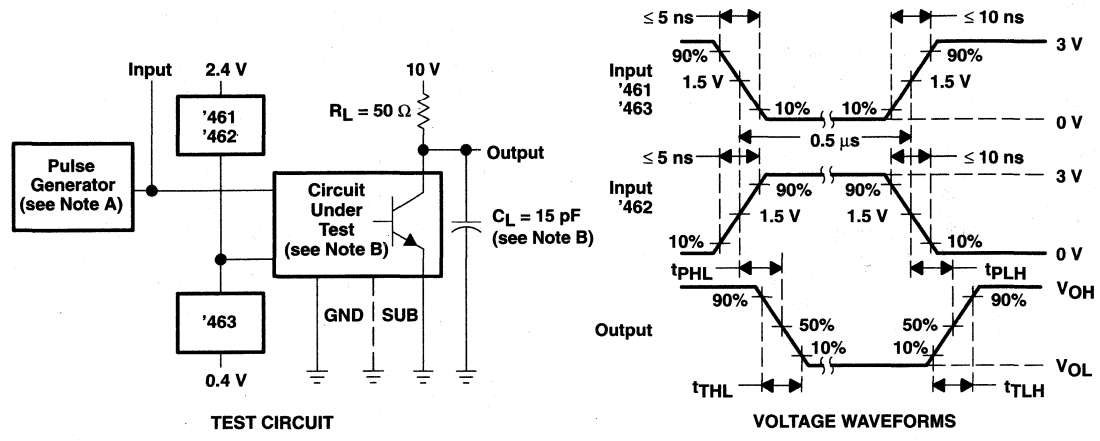
PARAMETER		TEST CONDITIONS†	SN55463			SN75463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		58	76		58	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

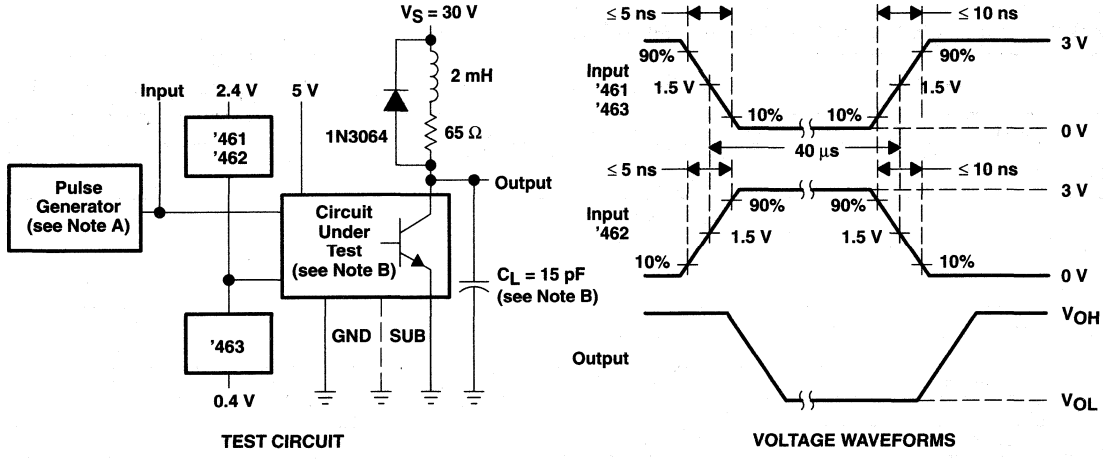
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	
t_{TLH}	Transition time, low-to-high-level output				8	25	
t_{THL}	Transition time, high-to-low-level output				10	25	
V_{OH}	High-level output voltage after switching	SN55463	V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S−10		mV
		SN75463			V_S−10		

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms for Switching Times

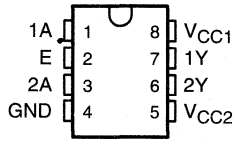


NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test

- **Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range up to 24 V**
- **Low Standby Power Dissipation**

D OR P PACKAGE
(TOP VIEW)

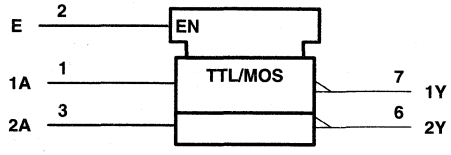


description

The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V_{CC1} of 5 V and a V_{CC2} of up to 24 V.

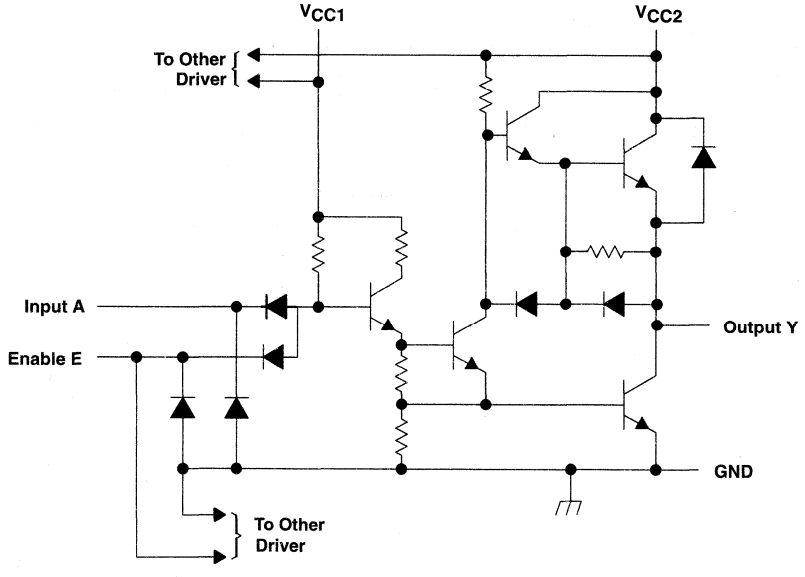
The SN75372 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC1} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, V_{CC2} ..... −0.5 V to 25 V
Input voltage, V_I ..... 5.5 V
Peak output current, V_O (t_w < 10 ms, duty cycle < 50%) ..... 500 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

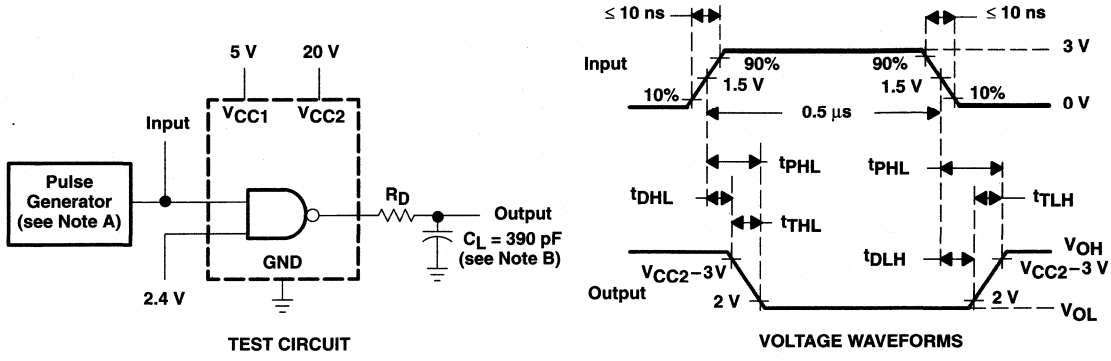
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA				−1.5	V
V_{OH}	High-level output voltage		V_{IL} = 0.8 V,	$I_{OH} = -50$ μA	$V_{CC2}-1.3$	$V_{CC2}-0.8$		V
			V_{IL} = 0.8 V,	$I_{OH} = -10$ mA	$V_{CC2}-2.5$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
			V_{CC2} = 15 V to 24 V, I_{OL} = 40 mA	V_{IH} = 2 V,		0.25	0.5	
V_F	Output clamp-diode forward voltage		V_I = 0,	I_F = 20 mA			1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V				40	μA
		Any E					80	
I_{IL}	Low-level input current	Any A	V_I = 0.4 V			−1	−1.6	mA
		Any E				−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high						0.5	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, All inputs at 5 V,	V_{CC2} = 24 V, No load		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low					7	13	mA
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, All inputs at 5 V,	V_{CC2} = 24 V, No load			0.5	mA

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, and T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		20	35	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

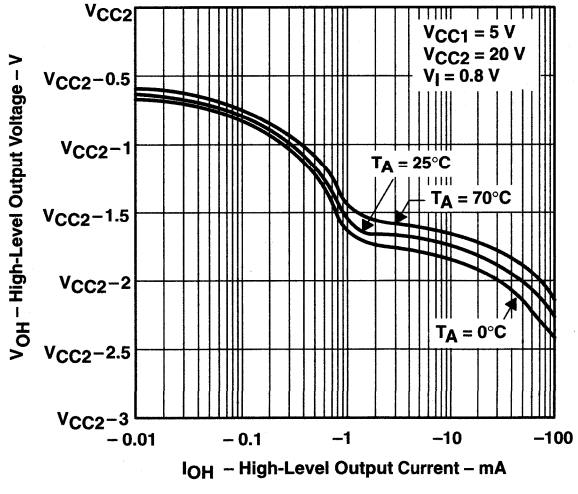


Figure 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

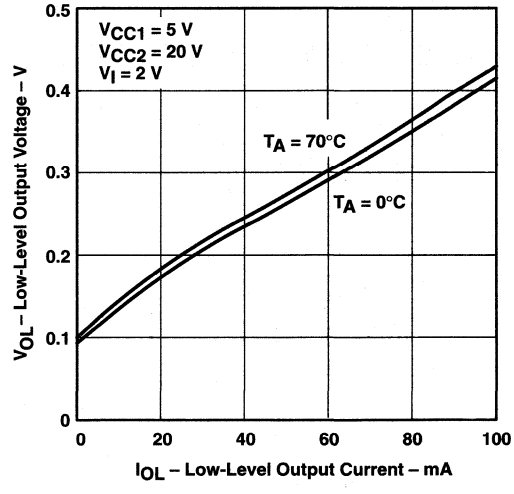


Figure 3

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

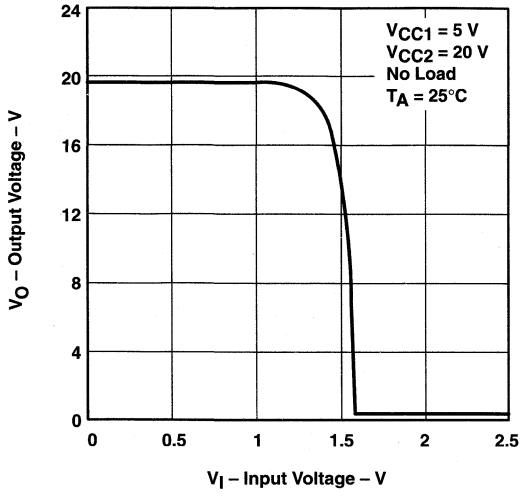


Figure 4

POWER DISSIPATION (BOTH DRIVERS)
vs
FREQUENCY

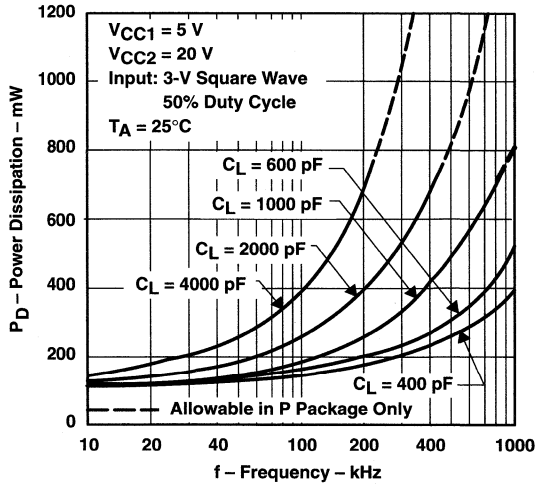


Figure 5

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

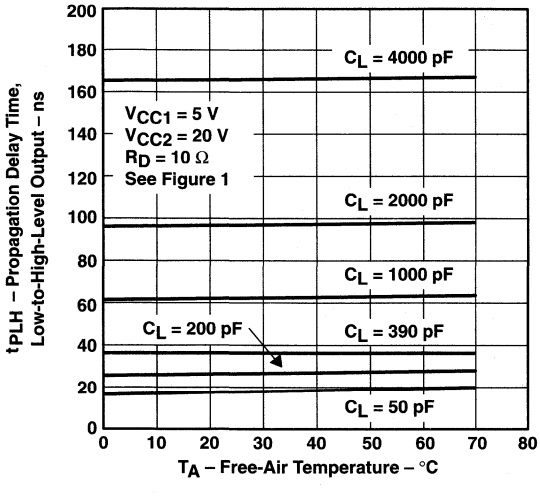


Figure 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

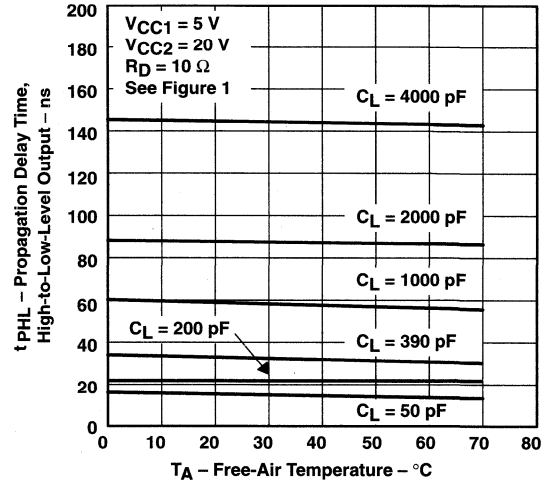


Figure 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

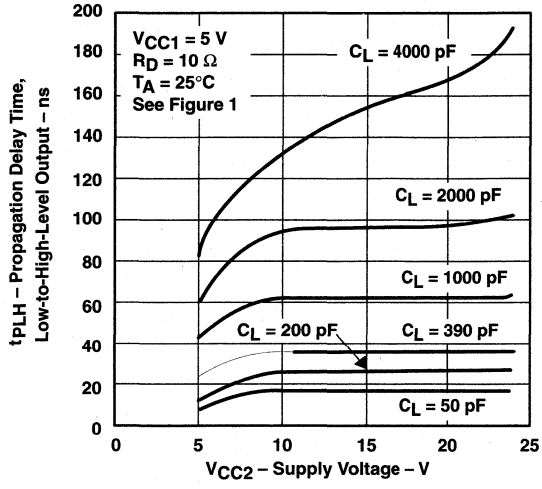


Figure 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

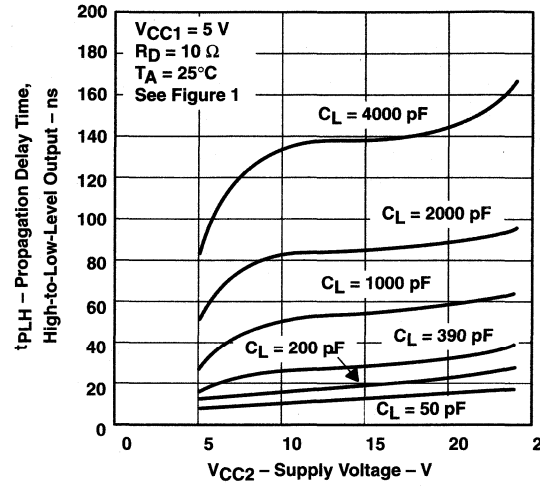


Figure 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

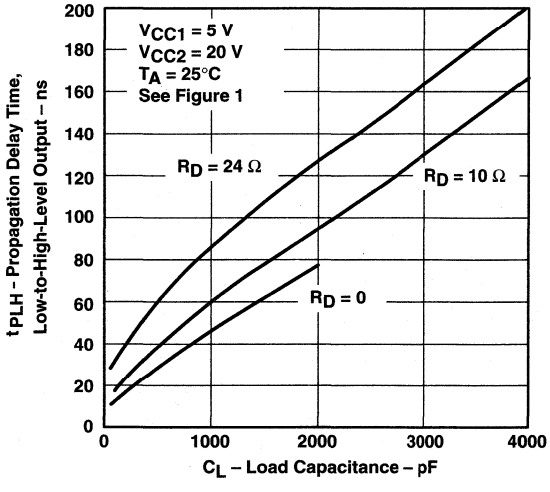


Figure 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

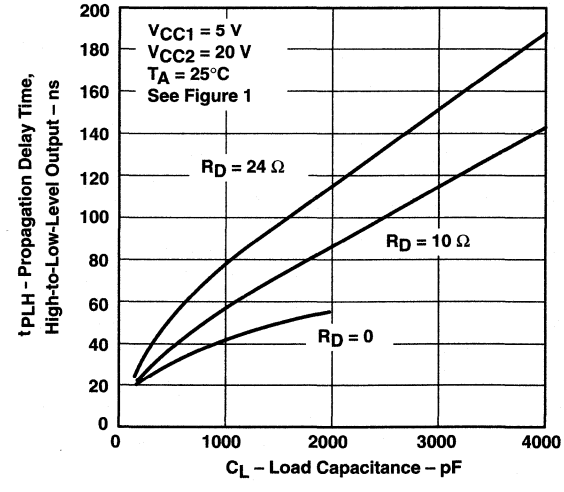


Figure 11

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} = P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load, and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C\, V_C^2\, f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 14.

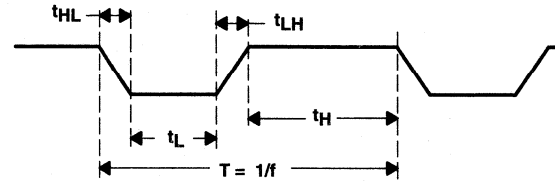


Figure 12. Output Voltage Waveform

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, both channels are operating under identical conditions: V_{OH} =19.2 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_C = 19.05 V, C = 1000 pF, and the duty cycle = 60%. At 0.5 MHz, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is high, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{2\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{16\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)} = (1000\text{ pF})\,(19.05\text{ V})^2\,(0.5\text{ MHz}) = 182\text{ mW}$ per channel

Total power for each driver is

$P_{T(AV)} = 47\text{ mW} + 182\text{ mW} = 229\text{ mW}$

and total package power is

$P_{T(AV)} = (229)\,(2) = 458\text{ mW}$.

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pullup resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of C_{iss} and the pullup resistor is shown in Figure 12(b).

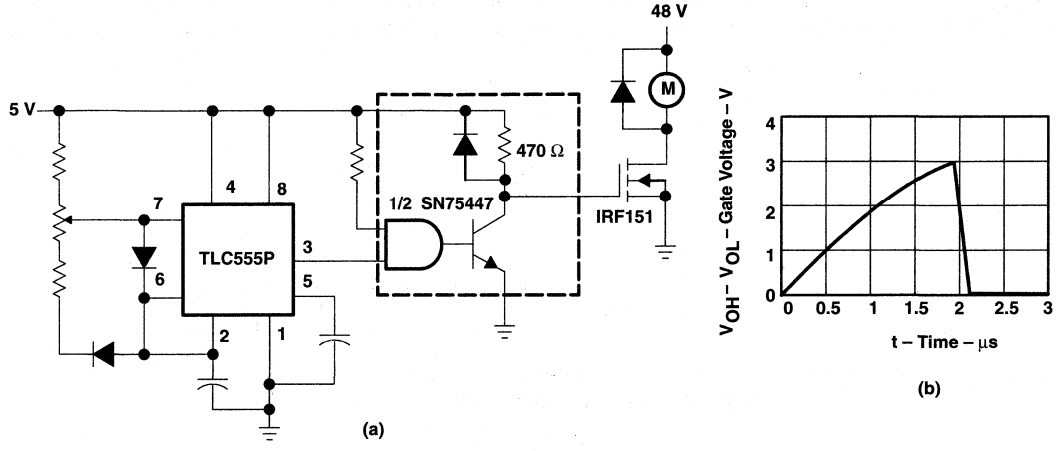


Figure 13. Power MOSFET Drive Using SN75447

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APPLICATION INFORMATION

A faster, more efficient drive circuit uses an active pullup as well as an active pulldown output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).

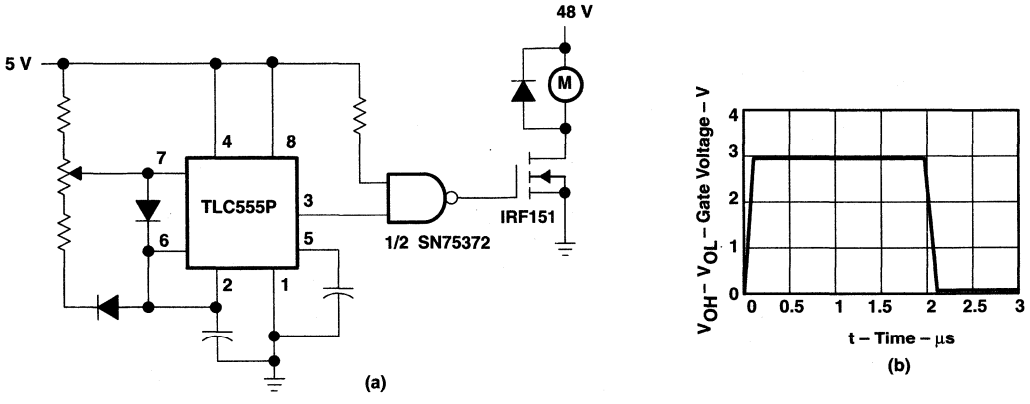


Figure 14. Power MOSFET Drive Using SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired drive time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-cast conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, the SN75374 quad MOSFET driver should be used.

- **Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range From 5 V to 24 V**
- **Low Standby Power Dissipation**
- **V_{CC3} Supply Maximizes Output Source Voltage**

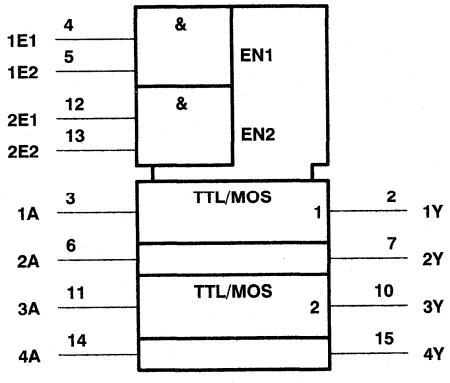
description

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. V_{CC3} can also be tied directly to V_{CC2} when the source voltage requirements are lower.

The SN75374 is characterized for operation from 0°C to 70°C.

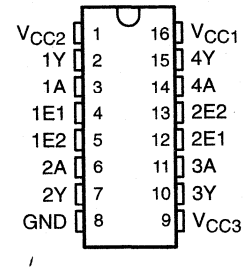
logic symbol†



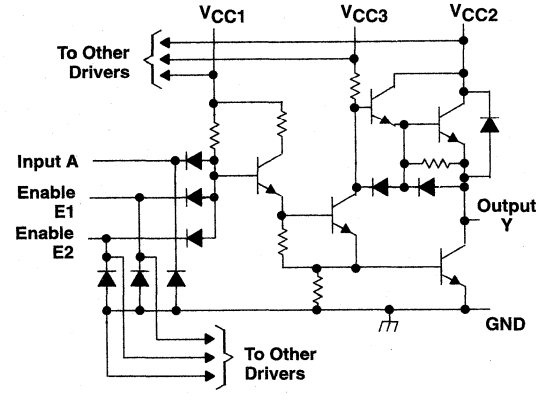
(7–48)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

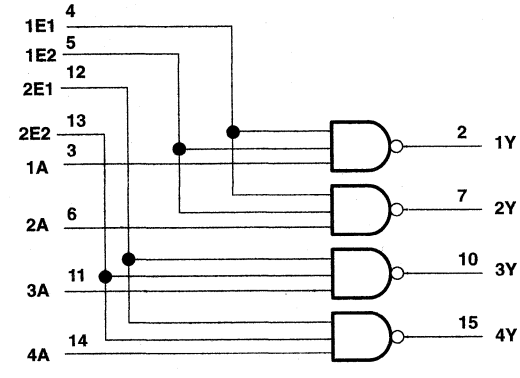
D OR N PACKAGE
(TOP VIEW)



schematic (each driver)



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range of V_{CC2} ..... −0.5 V to 25 V
Supply voltage range of V_{CC3} ..... −0.5 V to 30 V
Input voltage, V_I ..... 5.5 V
Peak output current, I_I (t_w < 10 ms, duty cycle < 50%) ..... 500 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3} - V_{CC2}$	0	4	10	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
High-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

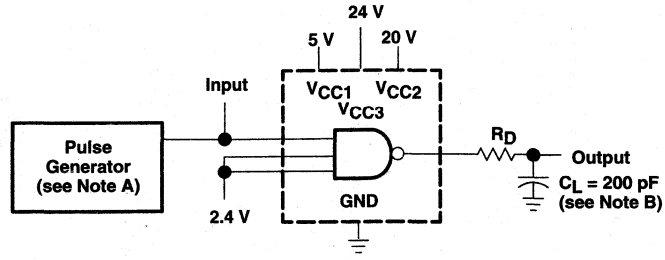
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA					−1.5	V
V_{OH}	High-level output voltage		$V_{CC3} = V_{CC2} + 3$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = -100$ μA	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
			$V_{CC3} = V_{CC2} + 3$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = -10$ mA	$V_{CC2}-1.3$	$V_{CC2}-0.9$		
			$V_{CC3} = V_{CC2}$,	$V_{IL} = 0.8$ V,	$I_{OH} = -50$ μA	$V_{CC2}-1$	$V_{CC2}-0.7$		
			$V_{CC3} = V_{CC2}$,	$V_{IL} = 0.8$ V,	$I_{OH} = -10$ mA	$V_{CC2}-2.5$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		$V_{IH} = 2$ V,	$I_{OL} = 10$ mA			0.15	0.3	V
			$V_{CC2} = 15$ V to 28 V,	$V_{IH} = 2$ V,	$I_{OL} = 40$ mA		0.25	0.5	
V_F	Output clamp-diode forward voltage		$V_I = 0$,	$I_F = 20$ mA				1.5	V
I_I	Input current at maximum input voltage		$V_I = 5.5$ V					1	mA
I_{IH}	High-level input current	Any A	$V_I = 2.4$ V					40	μA
		Any E						80	
I_{IL}	low-level input current	Any A	$V_I = 0.4$ V				−1	−1.6	mA
		Any E					−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		$V_{CC1} = 5.25$ V, All inputs at 0 V,	$V_{CC2} = 24$ V, No load	$V_{CC3} = 28$ V,		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high						−2.2	0.25	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high						2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		$V_{CC1} = 5.25$ V, All inputs at 5 V,	$V_{CC2} = 24$ V, No load	$V_{CC3} = 28$ V,		31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low							2	
$I_{CC3(L)}$	Supply current from V_{CC1}, all outputs low						16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high		$V_{CC1} = 5.25$ V, All inputs at 0 V,	$V_{CC2} = 24$ V, No load	$V_{CC3} = 24$ V,			0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high							0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		$V_{CC1} = 0$, All inputs at 0 V,	$V_{CC2} = 24$ V, No load	$V_{CC3} = 24$ V,			0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition							0.5	

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

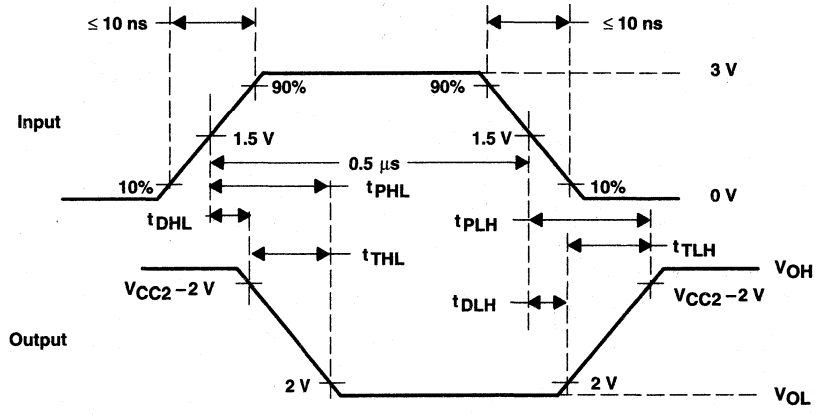
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	$C_L = 200$ pF, $R_D = 24\ \Omega$, See Figure 1		20	30	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

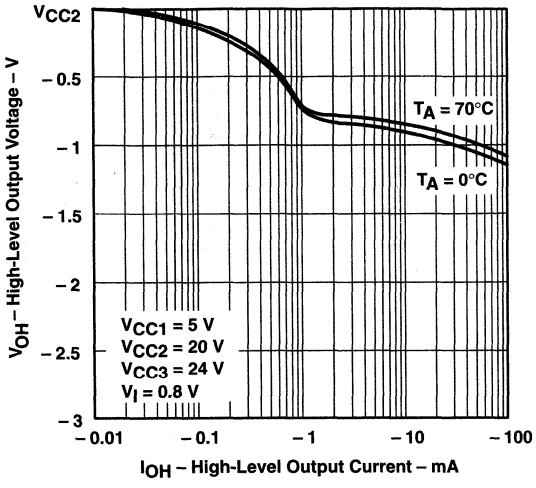


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

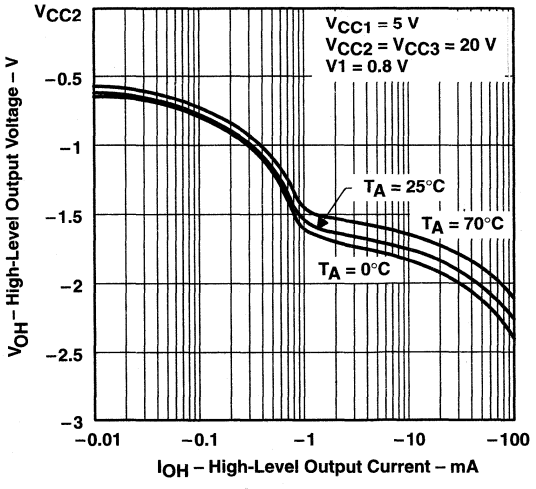


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

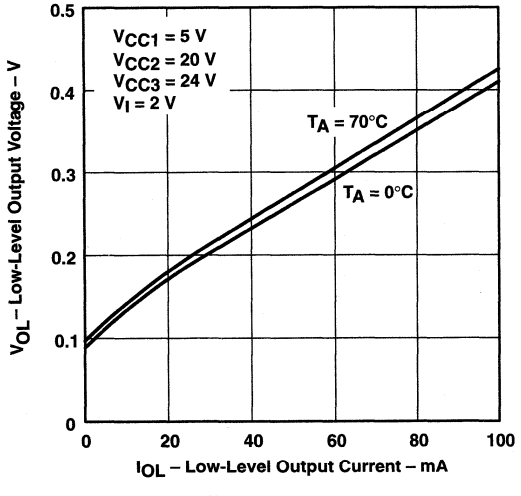


Figure 4

VOLTAGE TRANSFER CHARACTERISTICS

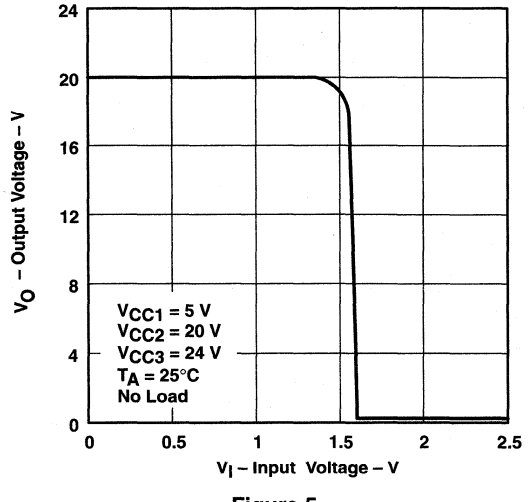


Figure 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

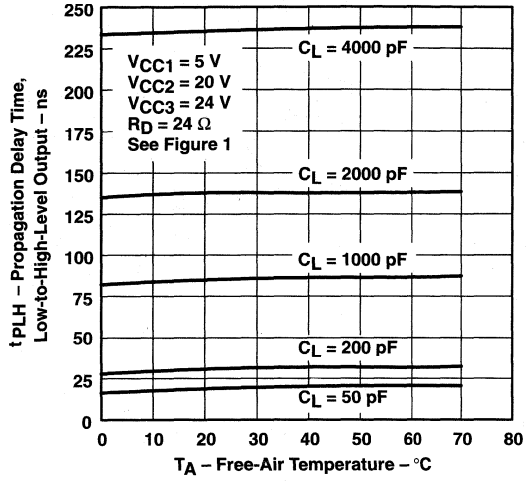


Figure 6

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

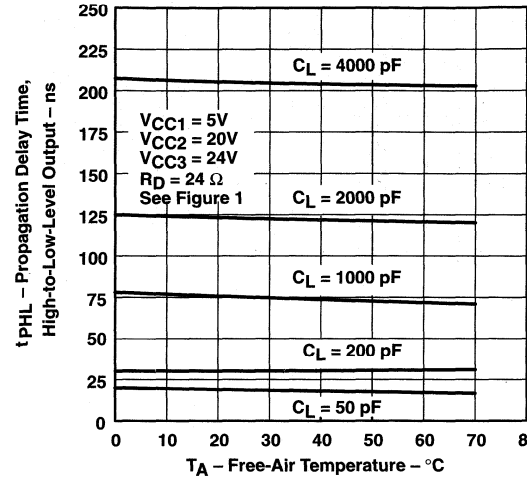


Figure 7

PROPAGATION DELAY TIME
LOW-TO-HIIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

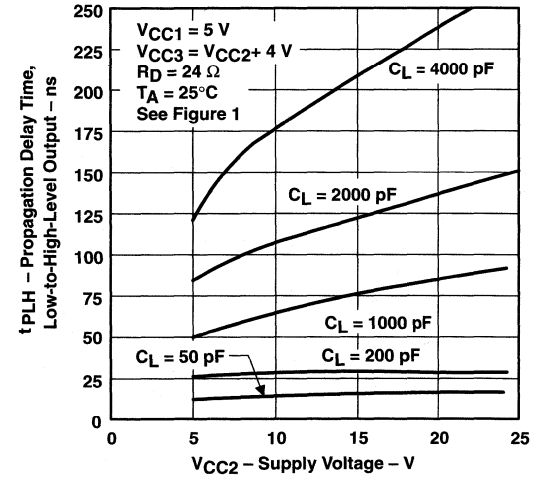


Figure 8

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

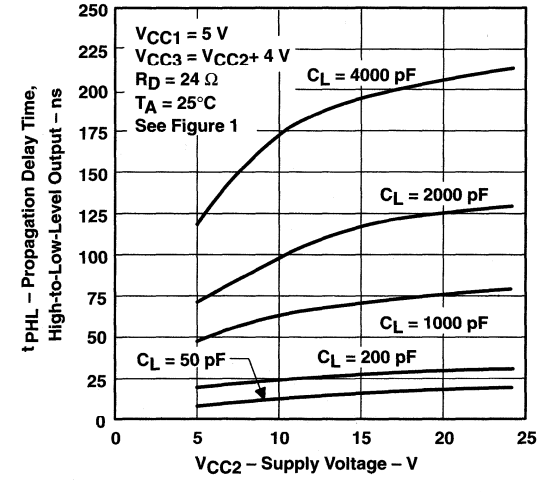


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

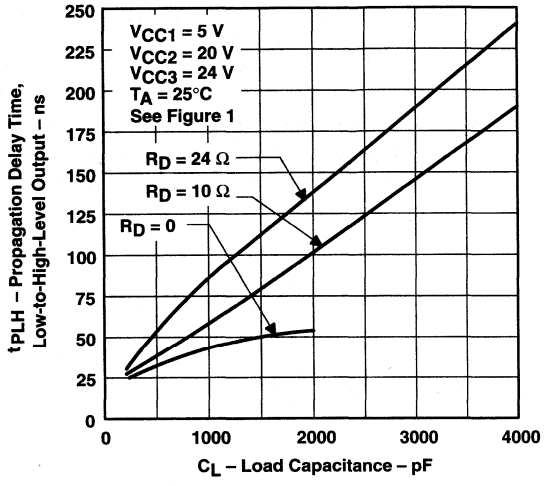


Figure 10

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

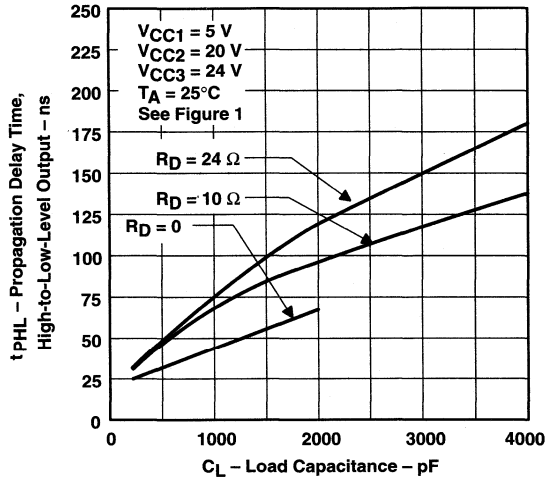


Figure 11

POWER DISSIPATION (ALL DRIVERS)
vs
FREQUENCY

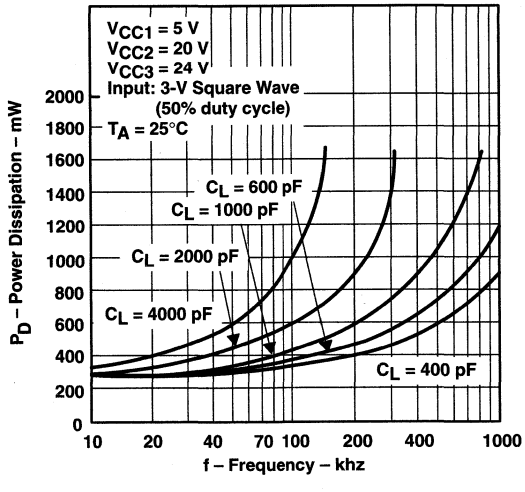


Figure 12

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C\, V_c^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

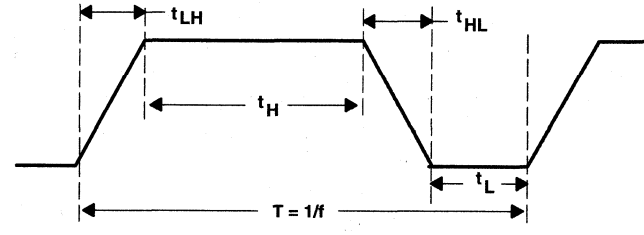


Figure 13. Output Voltage Waveform

where the times are as defined in Figure 15.

THERMAL INFORMATION

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, V_{OH} = 19.9 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_C = 19.75 V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for C_L < 2000 pF, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{4\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{-2.2\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) +$$

$$\left[(5\text{ V})\left(\frac{31\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58.2 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)} = (1000\text{ pF})\ (19.75\text{ V})^2\ (0.2\text{ MHz}) = 78\text{ mW per channel}$

Total power for each driver is

$P_{T(AV)}$ = 58.2 mW + 78 mW = 136.2 mW

The total package power is

$P_{T(AV)} = (136.2)\ (4) = 544.8\text{ mW}$

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 13(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pullup resistor. The input capacitance (C_{ISS}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the product of input capacitance and the pullup resistor is shown in Figure 13(b).

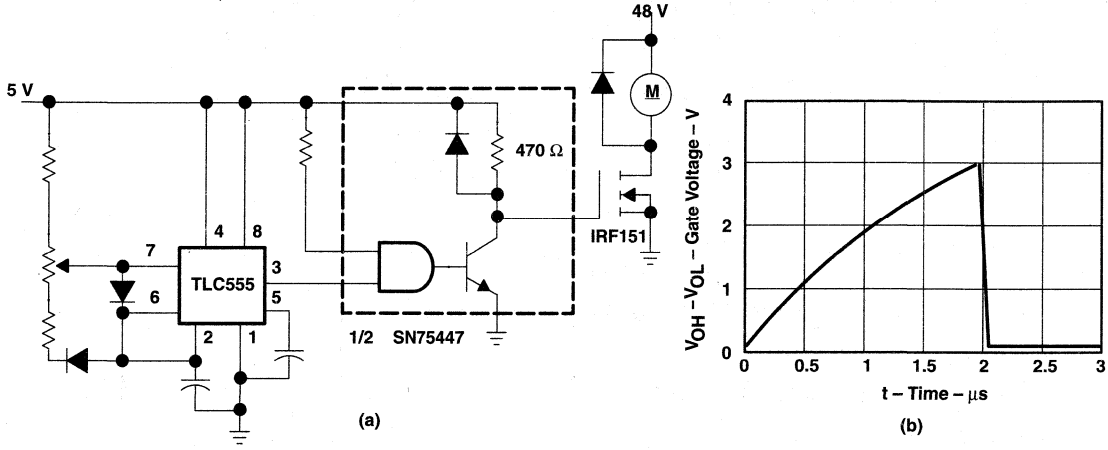


Figure 14. Power MOSFET Drive Using SN75447

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type, see Figure 14(a). The resulting faster switching speeds are shown in Figure 14(b).

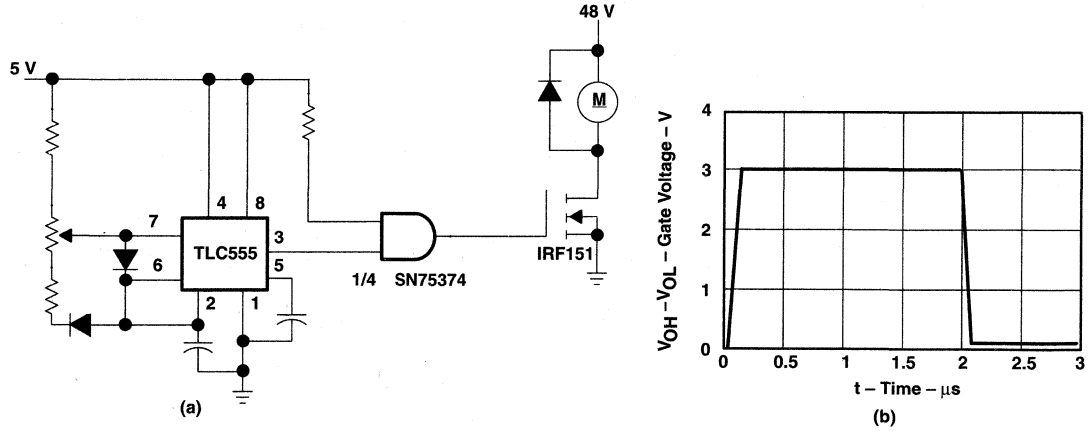


Figure 15. Power MOSFET Drive Using SN75374

APPLICATION INFORMATION

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{PK} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14(a) is

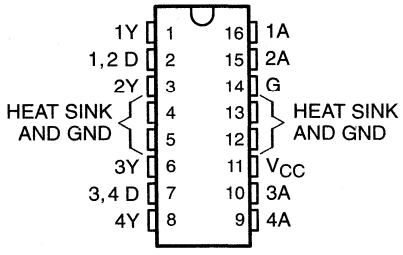
$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

- **Saturating Outputs With Low On-State Resistance**
- **High-Impedance Inputs Compatible With CMOS and TTL Levels**
- **Very Low Standby Power . . . 21 mW Max**
- **High-Voltage Outputs . . . 70 V Min**
- **No Power-Up or Power-Down Output Glitch**
- **No Latch-Up Within Recommended Operating Conditions**
- **Output-Clamp Diodes for Transient Suppression**
- **2-W Power Package**

NE PACKAGE
(TOP VIEW)

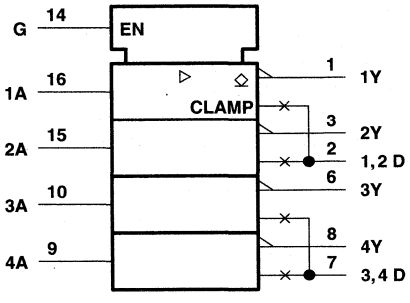


description

The SN75436 and SN75437A quadruple peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each device features four inverting open-collector outputs with a common-enable input that, when taken low, disables all four outputs. The envelope of 1-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

The SN75436 and SN75437A are offered in a 16-pin wide-body surface-mount (NE) package and is characterized for operation over the free-air temperature of 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

FUNCTION TABLE
(each NAND driver)

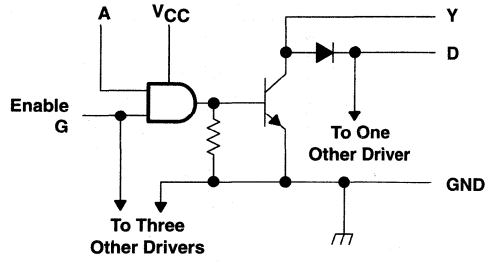
INPUTS		OUTPUT
A	G	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

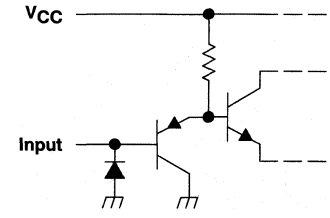
SELECTION GUIDE

FEATURE	SN75436	SN75437A	UNIT
Maximum recommended output current	0.5	0.5	A
Maximum V_{OL} at maximum I_{OL}	0.5	0.5	V
Maximum recommended output supply voltage in an inductive switching circuit, V_S	50	35	V

logic diagram (positive logic, each driver)



equivalent schematic of each input



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 30 V
Output current (see Note 1) ..... 0.75 A
Output clamp-diode current, I_{OK} ..... 1.25 A
Output voltage, V_O (off state) ..... 70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 2075 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds ..... 260°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

recommended operating conditions

PARAMETER	SN75436			SN75437A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Output supply voltage in inductive switching circuit (see Figure 2), V_S			50			35	V
Output current, I_O			0.5			0.5	A
Operating free-air temperature, T_A	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

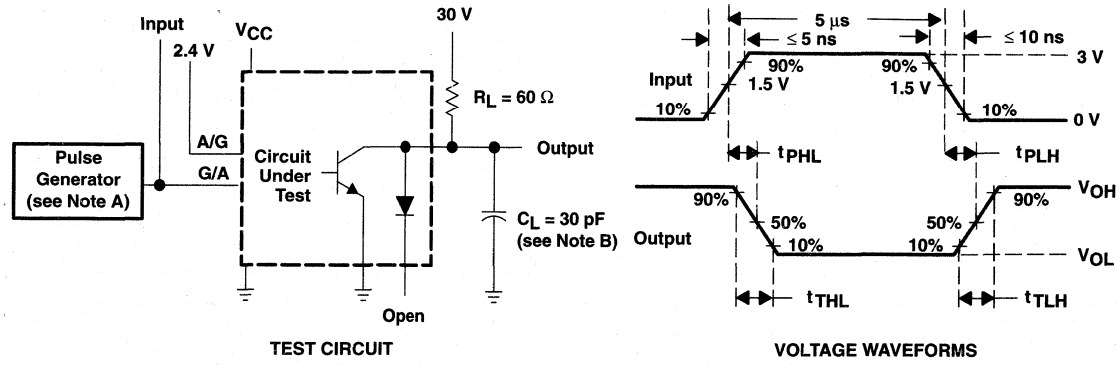
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA			−0.9	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 250 mA		0.14	0.25	V
			I_{OL} = 500 mA		0.28	0.5	
$V_{R(K)}$	Output clamp-diode reverse voltage	V_{CC} = 4.75 V, I_R = 100 µA		70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage	I_F = 500 mA			1	1.6	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	µA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 5.25 V			0.1	10	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.8 V			−0.25	−10	µA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 0			1	4	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 5 V			45	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

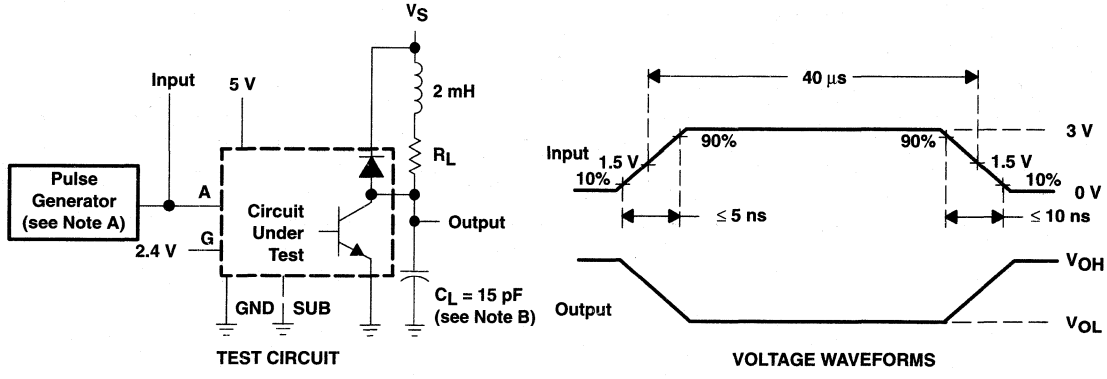
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 30 pF, See Figure 1	R_L = 60 Ω,		1950	5000	ns
t_{PHL}	Propagation delay time, high-to-low-level output					150	500	ns
t_{TLH}	Transition time, low-to-high-level output					40		ns
t_{THL}	Transition time, high-to-low-level output					36		ns
V_{OH}	High-level output voltage after switching	SN75436	V_S = 50 V, R_L = 100 Ω,	I_O ≈ 500 mA, See Figure 2	V_S−10			mV
		SN75437A	V_S = 35 V, R_L = 70 Ω,	I_O ≈ 500 mA, See Figure 2	V_S−10			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

SLRS013A – MAY 1988 – REVISED NOVEMBER 1989

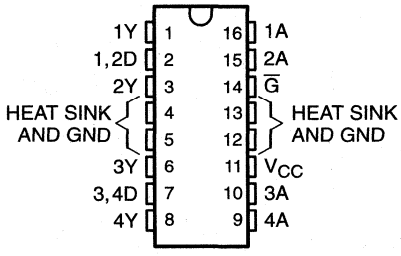
- **1.3-A Current Capability Each Channel**
- **Saturating Outputs With Low On-State Resistance**
- **Two Inverting and Two Noninverting Driver Channels With Common Active-Low Enable Input**
- **Key Application Is as a Complete Full-Step 4-Phase DC Stepper Motor Driver Using Only Three Directly Connected Logic Control Signal Lines From Standard Microprocessors**
- **High-Impedance Inputs Compatible With TTL or CMOS Levels**
- **Very Low Standby Power . . . 10 mW Typ**
- **50-V Noninductive Switching Voltage Capability**
- **40-V Inductive Switching Voltage Capability**
- **Output Clamp Diodes for Inductive Transient Protection**
- **2-W Power Package**

description

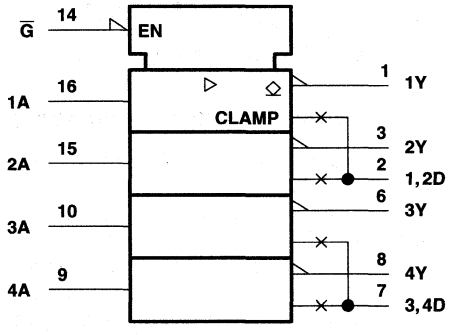
The SN75439 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. The device features two inverting and two noninverting open-collector outputs with a common-enable input that, when taken high, disables all four outputs. By pairing each inverting channel with a corresponding noninverting channel (such as channel 1 paired with channel 2 and channel 3 paired with channel 4), the device may be used as a complete full-step 4-phase dc stepper-motor driver using only two input logic control signals plus the enable signal, as shown in Figure 3. Other applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand loads.

The SN75439 is characterized for operation from 0°C to 70°C.

NE PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

Function Tables

EACH CHANNEL 1 OR CHANNEL 4 DRIVER

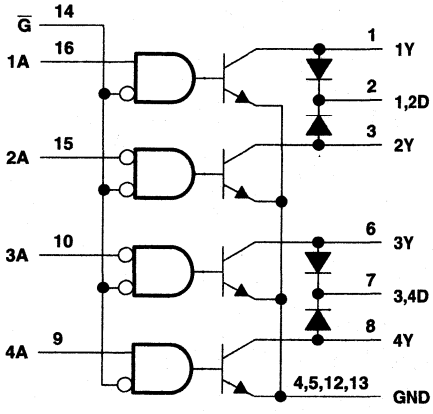
INPUTS		OUTPUT
A	$\overline{G}$	Y
H	L	L
L	X	H
X	H	H

EACH CHANNEL 2 OR CHANNEL 3 DRIVER

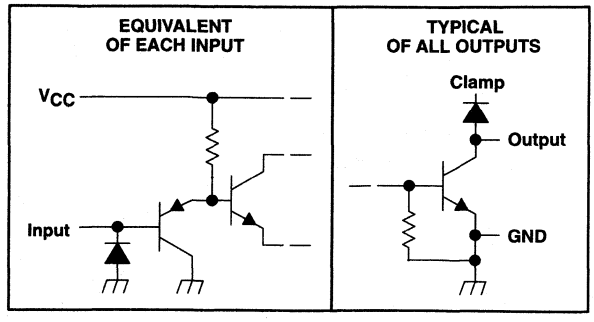
INPUTS		OUTPUT
A	$\overline{G}$	Y
L	L	L
H	X	H
X	H	H

H = high level, L = low level X = irrelevant

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −0.3 V to 52 V
Output voltage, V_O (inductive load) ..... 43 V
Output clamp-diode terminal voltage range, V_{OK} ..... −0.3 V to 52 V
Input current, I_I ..... −15 mA
Peak sink output current, I_{OM} (nonrepetitive, $t_w \le 0.1$ ms) (see Note 2) ..... 1.5 A
(repetitive, $t_w \le 10$ ms, duty cycle ≤ 50%) ..... 1.4 A
Continuous sink output current, I_O (see Note 2) ..... 1.3 A
Peak output clamp diode current, I_{OKM} (nonrepetitive, $t_w \le 0.1$ ms) (see Note 2) ..... 1.5 A
(repetitive, $t_w \le 10$ ms, duty cycle ≤ 50%) ..... 1.3 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) ..... 2075 mW
Continuous total dissipation at (or below) 65°C case temperature (see Note 3) ..... 5000 mW
Operating case or virtual junction temperature range ..... −55°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network GND (unless otherwise specified).
2. All four channels of this device may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation range.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. For operation above 65°C case temperature, derate linearly at the rate of 59 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Output supply voltage in inductive switching circuit, V_S (see Figure 2)			40	V
High-level input voltage, V_{IH}	2		5.25	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Low-level output current, I_{OL}			1.3	A
Operating free-air temperature, T_A	0	25	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A	See Note 4		0.2	0.35	V
		I_{OL} = 1 A			0.4	0.7	
		I_{OL} = 1.3 A			0.5	0.9	
$V_{F(K)}$	Output clamp-diode forward voltage	I_F = 0.5 A	See Note 4		1.1	1.9	V
		I_F = 1 A			1.3	2.2	
		I_F = 1.3 A			1.4	2.4	
I_{OH}	High-level output current	V_{OH} = 50 V,	V_{OK} = 50 V			100	µA
I_{IH}	High-level input current	$V_I = V_{IH}$				10	µA
I_{IL}	Low-level input current	V_I = 0 to 0.8 V				−10	µA
$I_{R(K)}$	Output clamp-diode reverse current (at Y output)	V_R = 50 V,	V_O = 0			100	µA
I_{CC}	Supply current	All outputs at high level (off)			2	8	mA
		All outputs at low level (on)			140	200	
		Two outputs at high level (off) and two outputs at low level (on)			70	110	

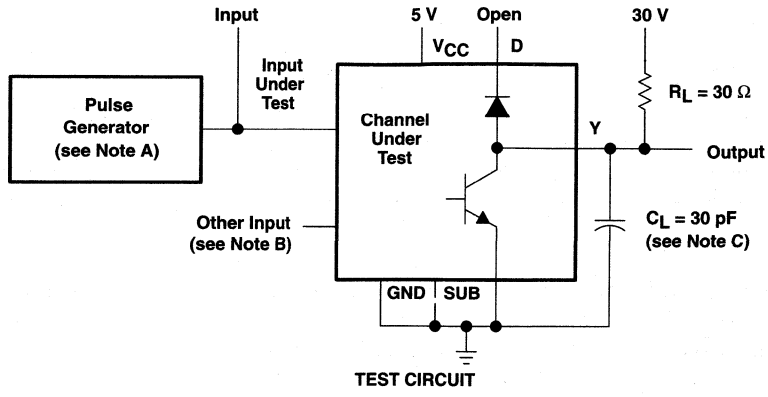
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: These parameters must be measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 10%.

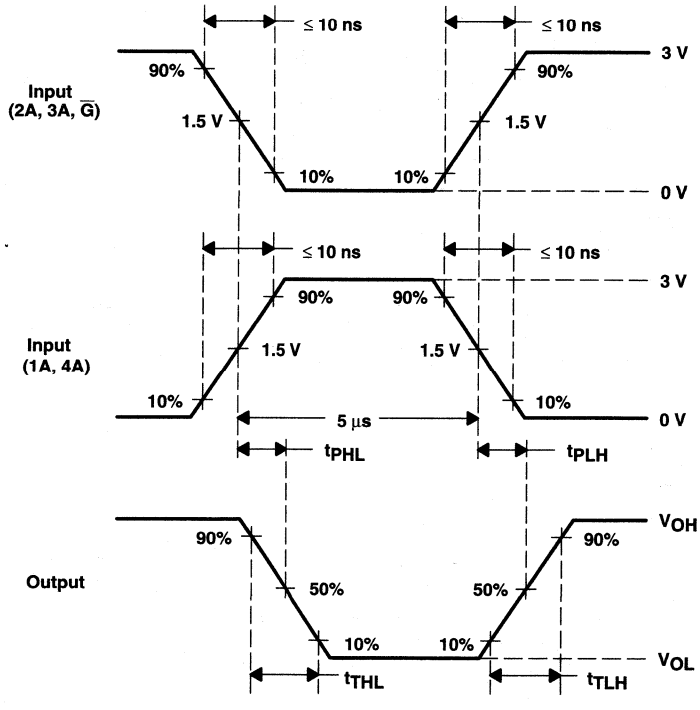
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_{OL} ≈ 1 A, R_L = 30 Ω,	C_L = 30 pF, See Figure 1		1500		ns
t_{PHL}	Propagation delay time, high-to-low-level output				100		ns
t_{TLH}	Transition time, low-to-high-level output				170		ns
t_{THL}	Transition time, high-to-low-level output				50		ns
V_{OH}	High-level output voltage (after switching inductive load)	V_S = 40 V, R_L = 31 Ω,	I_O ≈ 1.3 A, See Figure 2	V_S − 100			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

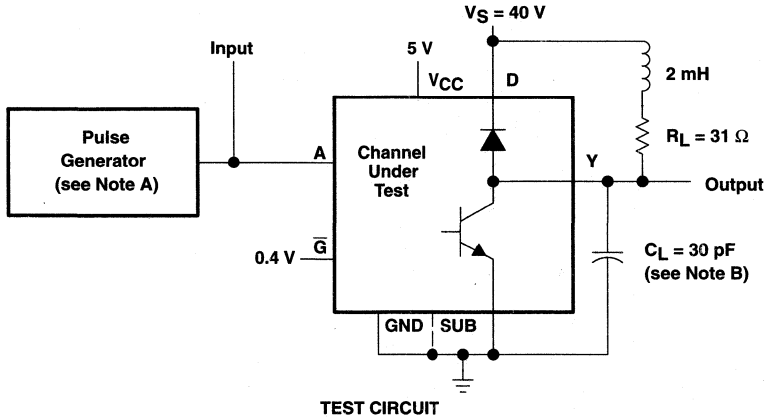


VOLTAGE WAVEFORMS

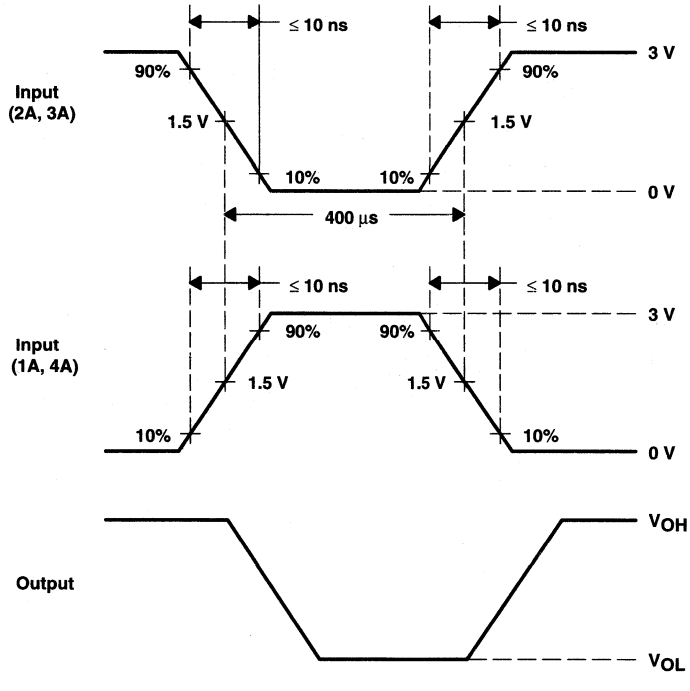
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1 %, Z_O = 50 Ω.
B. Enable input $\overline{G}$ is at 0 V if input A is used as the switching input. When $\overline{G}$ is used as the switching input, the corresponding A input is at 0 V if testing channel 2 or channel 3 or at 3 V if testing channel 1 or channel 4.
C. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

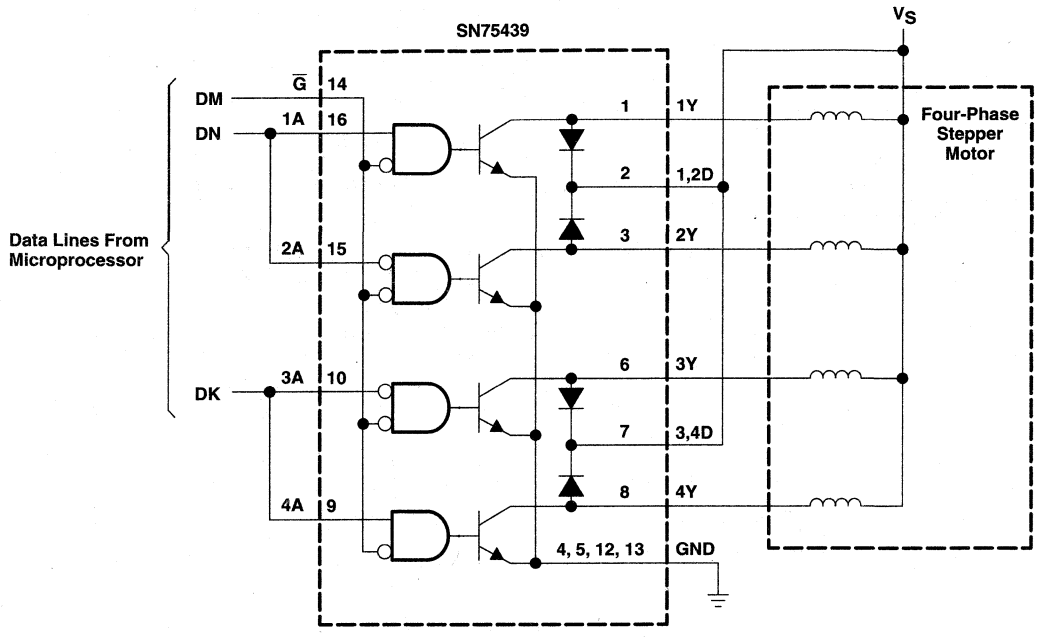


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1 %, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Output Latch-Up Test Circuit and Voltage Waveforms

APPLICATION INFORMATION



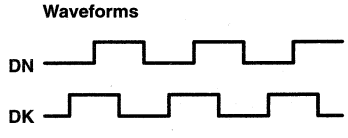
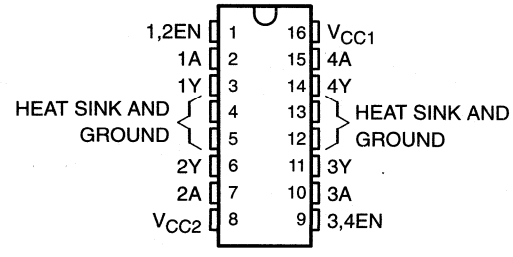


Figure 3. Full-Step Four-Phase Stepper-Motor Driver

SLRS007B – NOVEMBER 1986 – REVISED NOVEMBER 1995

- **1-A Output-Current Capability Per Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Designed for Positive-Supply Applications**
- **Wide Supply-Voltage Range of 4.5 V to 36 V**
- **TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs**
- **Separate Input-Logic Supply**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **Input Hysteresis Improves Noise Immunity**
- **3-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **No Output Glitch During Power Up or Power Down**
- **Improved Functional Replacement for the SGS L293**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each driver)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

description

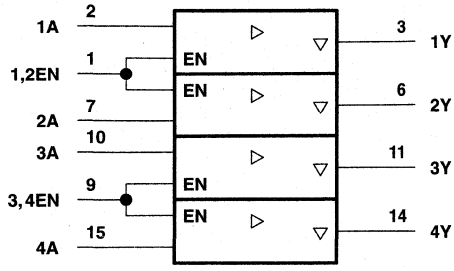
The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL-and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits.

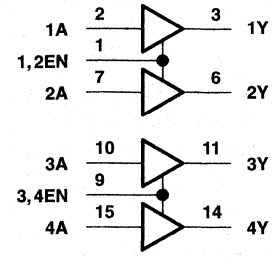
The SN754410 is designed for operation from −40°C to 85°C.

logic symbol†

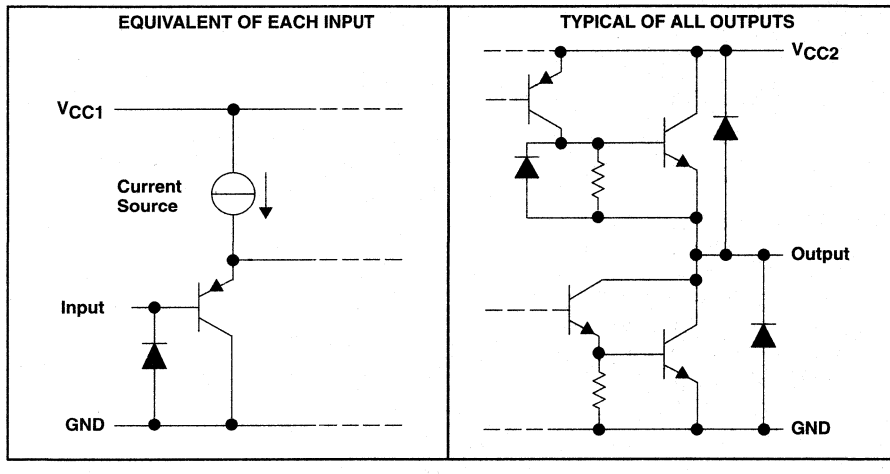


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Output supply voltage range, V_{CC1} (see Note 1) ..... −0.5 V to 36 V
Output supply voltage range, V_{CC2} ..... −0.5 V to 36 V
Input voltage, V_I ..... 36 V
Output voltage range, V_O ..... −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms) ..... ±2 A
Continuous output current, I_O ..... ±1.1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 2075 mW
Operating free-air temperature range, T_A ..... −40°C to 85°C
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Output supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3‡	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -12$ mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	$I_{OH} = -0.5$ A		$V_{CC2}-1.5$	$V_{CC2}-1.1$		V
		$I_{OH} = -1$ A		$V_{CC2}-2$			
		$I_{OH} = -1$ A, $T_J = 25°C$		$V_{CC2}-1.8$	$V_{CC2}-1.4$		
V_{OL}	Low-level output voltage	$I_{OL} = 0.5$ A			1	1.4	V
		$I_{OL} = 1$ A				2	
		$I_{OL} = 1$ A, $T_J = 25°C$			1.2	1.8	
V_{OKH}	High-level output clamp voltage	$I_{OK} = -0.5$ A			$V_{CC2}+1.4$	$V_{CC2}+2$	V
		$I_{OK} = 1$ A			$V_{CC2}+1.9$	$V_{CC2}+2.5$	
V_{OKL}	Low-level output clamp voltage	$I_{OK} = 0.5$ A			−1.1	−2	V
		$I_{OK} = -1$ A			−1.3	−2.5	
$I_{OZ(off)}$	Off-state high-impedance-state output current	$V_O = V_{CC2}$				500	μA
		$V_O = 0$				−500	
I_{IH}	High-level input current	$V_I = 5.5$ V				10	μA
I_{IL}	Low-level input current	$V_I = 0$				−10	μA
I_{CC1}	Output supply current	$I_O = 0$	All outputs at high level			38	mA
			All outputs at low level			70	
			All outputs at high impedance			25	
I_{CC2}	Output supply current	$I_O = 0$	All outputs at high level			33	mA
			All outputs at low level			20	
			All outputs at high impedance			5	

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $T_A = 25°C$.

switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $C_L = 30$ pF, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, high-to-low-level output from A input	See Figure 1		400		ns
t_{d2}	Delay time, low-to-high-level output from A input			800		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns
t_r	Rise time, pulse input					
t_f	Fall time, pulse input					
t_w	Pulse duration					
t_{en1}	Enable time to the high level	See Figure 2		700		ns
t_{en2}	Enable time to the low level			400		ns
t_{dis1}	Disable time from the high level			900		ns
t_{dis2}	Disable time from the low level			600		ns

PARAMETER MEASUREMENT INFORMATION

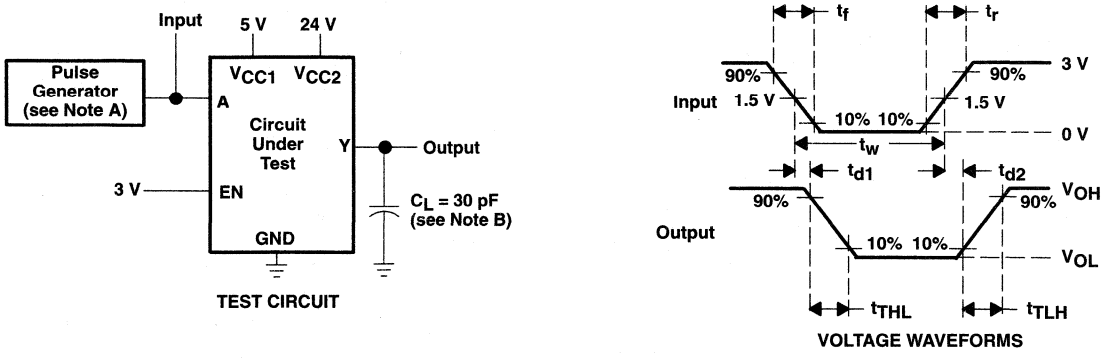


Figure 1. Test Circuit and Switching Times From Data Inputs

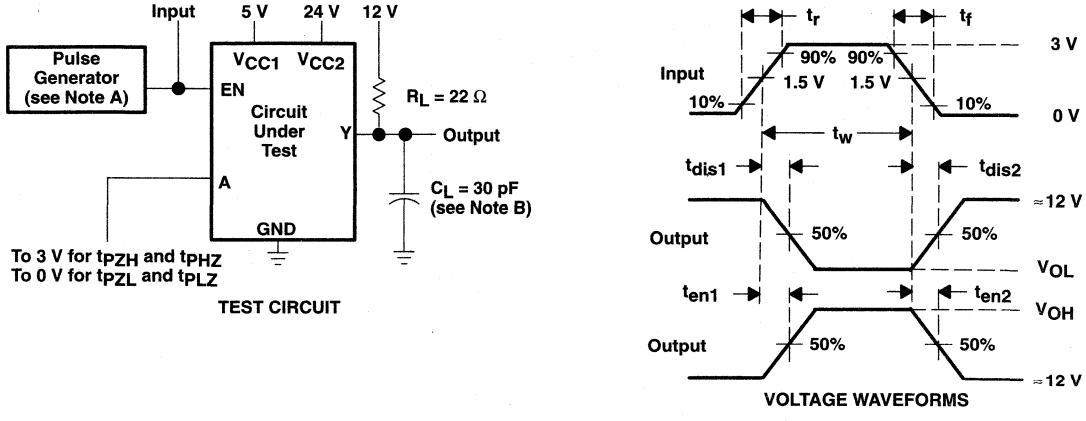


Figure 2. Test Circuit and Switching Times From Enable Inputs

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ µs, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

APPLICATION INFORMATION

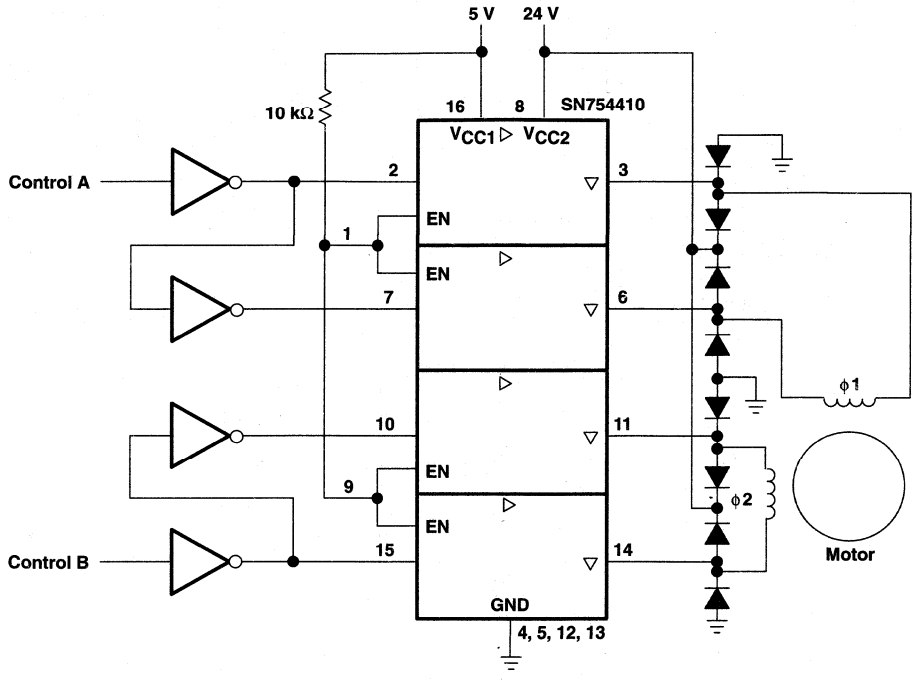


Figure 3. Two-Phase Motor Driver

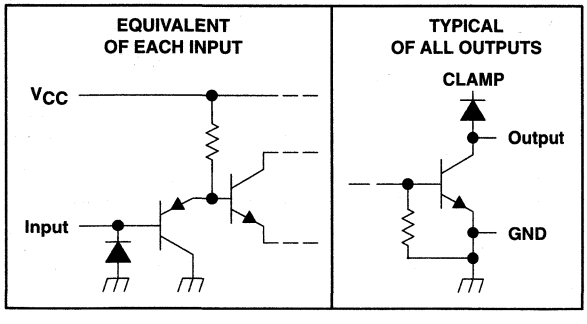
- **Very Low Power Requirements**
- **Very Low Input Current**
- **Characterized for Use to 350 mA**
- **No Output Latch-Up at 50 V (After Conducting 300 mA)**
- **High-Voltage Outputs (70 V Min)**
- **Output Clamp Diodes for Transient Suppression (350 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**

description

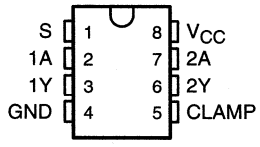
The SN75446 and SN75447 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446 and SN75447 provide AND and NAND drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

The SN75446 and SN75447 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



D OR P PACKAGE
(TOP VIEW)



Function Tables

SN75446
(each AND driver)

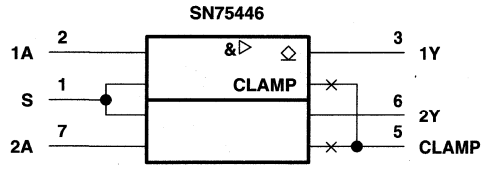
INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

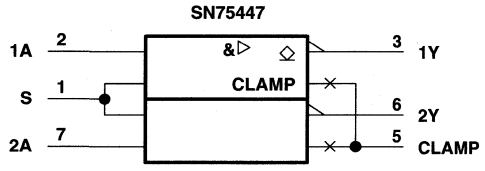
SN75447
(each NAND driver)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level
X = irrelevant

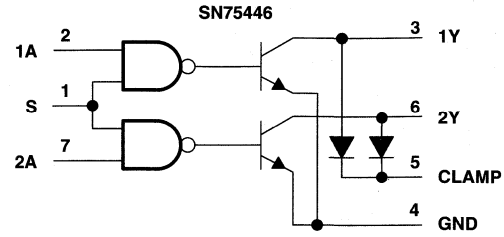
logic symbols†



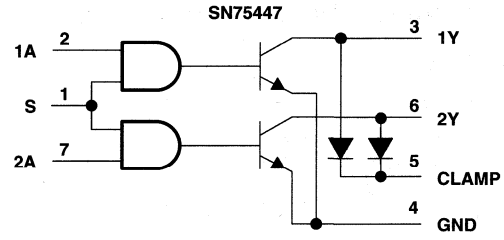


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagrams (positive logic)



Positive Logic: $Y = \overline{AS}$ or $\overline{\overline{A}+\overline{S}}$



Positive Logic: $Y = \overline{AS}$ or $\overline{\overline{A}+\overline{S}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Output current, I_O (see Note 2) ..... 400 mA
Output clamp-diode current ..... 400 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network GND.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

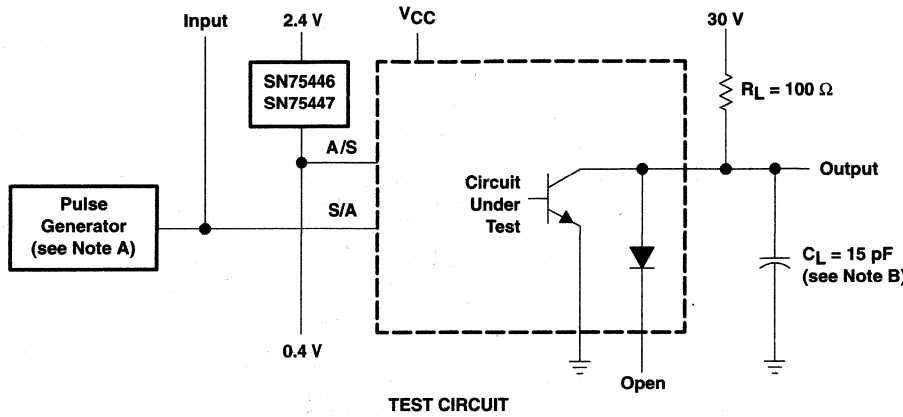
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−0.9	−1.5	V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 100 mA			0.1	0.3	V
				I_{OL} = 200 mA			0.22	0.45	
				I_{OL} = 300 mA			0.45	0.65	
				I_{OL} = 350 mA			0.55	0.75	
$V_{O(BR)}$	Output breakdown voltage		V_{CC} = 4.75 V,	I_{OH} = 100 µA		70	100		V
$V_{R(K)}$	Output clamp-diode reverse voltage		V_{CC} = 4.75 V,	I_R = 100 µA		70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage		V_{CC} = 4.75 V,	I_F = 350 mA		0.6	1.2	1.6	V
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V			1	100	µA
I_{IH}	High-level input current		V_{CC} = 5.25 V,	V_I = 5.25 V			0.01	10	µA
I_{IL}	Low-level input current	A input	V_{CC} = 5.25 V,	V_I = 0.8 V			−0.5	−10	µA
		S input					−1	−20	
I_{CCH}	Supply current, outputs high	SN75446	V_{CC} = 5.25 V	V_I = 5 V			11	18	mA
		SN75447		V_I = 0			11	18	
I_{CCL}	Supply current, outputs low	SN75446	V_{CC} = 5.25 V	V_I = 0			11	18	mA
		SN75447		V_I = 5 V			11	18	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

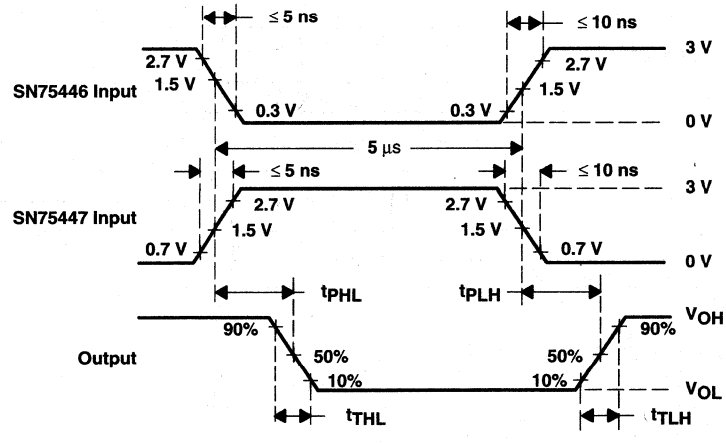
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1	R_L = 100 Ω,		300	750	ns
t_{PHL}	Propagation delay time, high-to-low-level output				200	500	ns
t_{TLH}	Transition time, low-to-high-level output				50	100	ns
t_{THL}	Transition time, high-to-low-level output				50	100	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 2	$I_O \approx$ 300 mA,	V_S−0.018			V

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

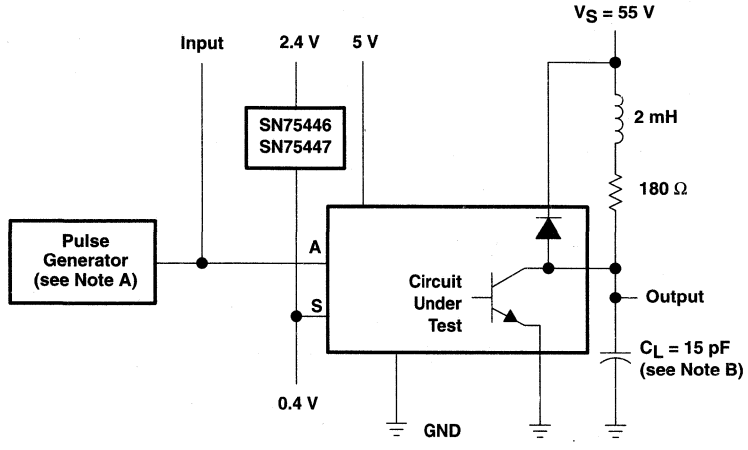


VOLTAGE WAVEFORMS

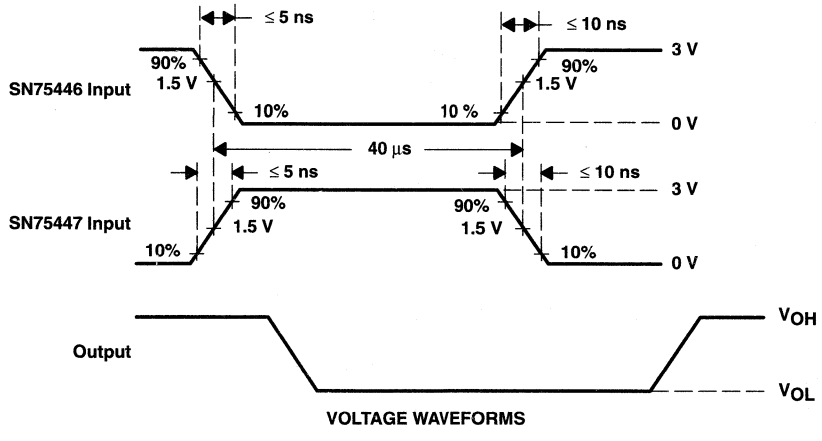
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

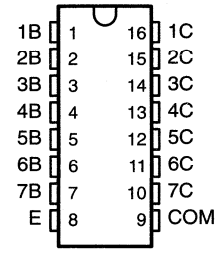
Figure 2. Latch-Up Test Circuit and Voltage Waveforms

SLRS023B – DECEMBER 1976 – REVISED SEPTEMBER 1995

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 100 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Higher-Voltage Versions of ULN2003A and ULN2004A, for Commercial Temperature Range**

D OR N PACKAGE
(TOP VIEW)

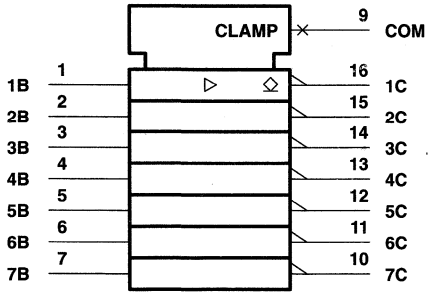


description

The SN75468 and SN75469 are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

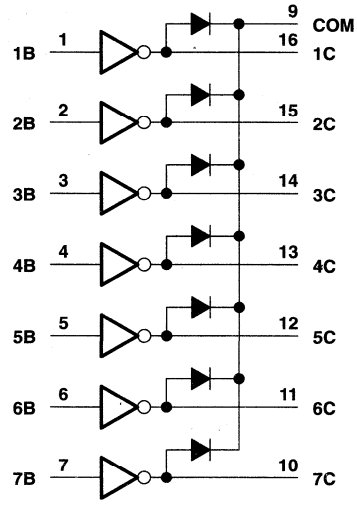
The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

logic symbol†

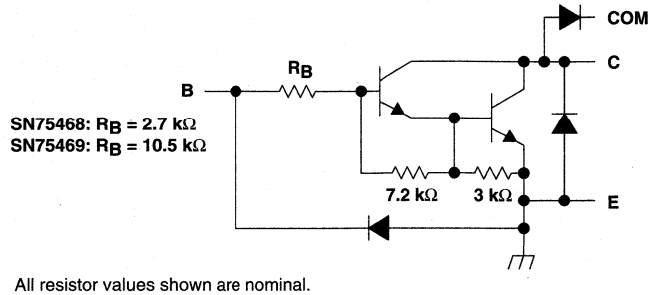


† This symbol is in accordance with ANSI/IEEE Std91-1984 and IEC publication 617-12.

logic diagram



schematic (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage, V_{CE} ..... 100 V
Input voltage, V_I (see Note 1) ..... 30 V
Peak collector current (see Figures 14 and 15) ..... 500 mA
Output clamp current, I_{OK} ..... 500 mA
Total emitter-terminal current ..... −2.5 A
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75468			SN75469			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp-diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0			50			50	µA
		2	V_{CE} = 100 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp-diode reverse current	7	V_R = 100 V				50			50	µA
			V_R = 100 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

switching characteristics, T_A = 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V, R_L = 163 Ω, C_L = 15 pF, See Figure 9		0.25	1	µs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 10	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

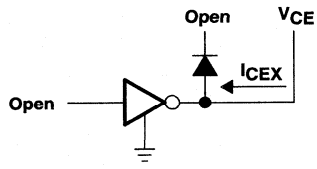


Figure 1. I_{CEX}

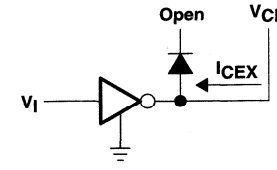


Figure 2. I_{CEX}

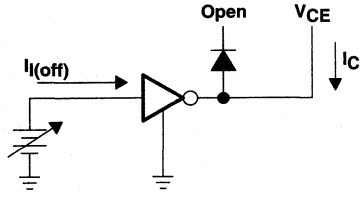


Figure 3. $I_{I(off)}$

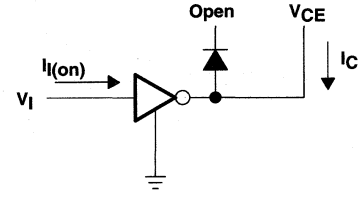


Figure 4. I_I

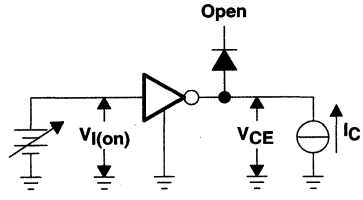
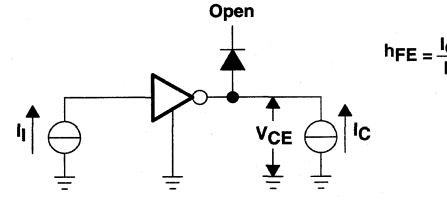


Figure 5. $V_{I(on)}$



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 6. h_{FE}, $V_{CE(sat)}$

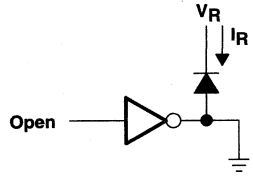


Figure 7. I_R

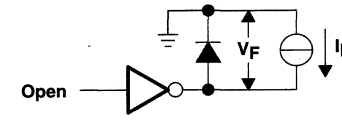


Figure 8. V_F

PARAMETER MEASUREMENT INFORMATION

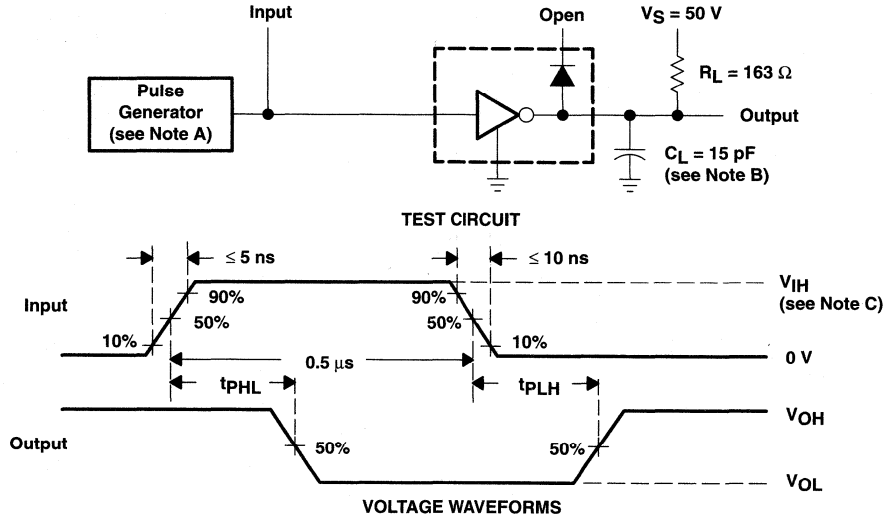


Figure 9. Test Circuit and Voltage Waveforms

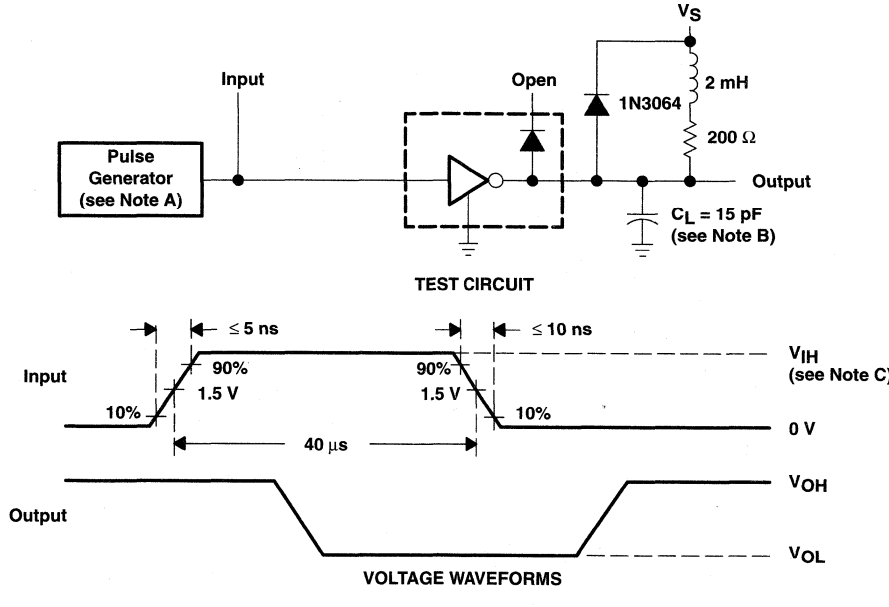


Figure 10. Latch-Up Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '468, V_{IH} = 3 V; for the '469, V_{IH} = 8 V.

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

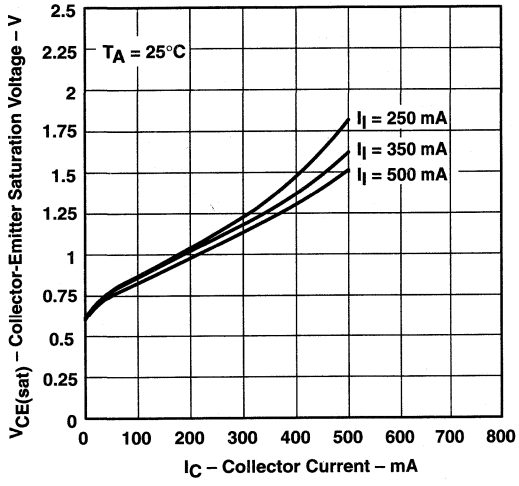


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

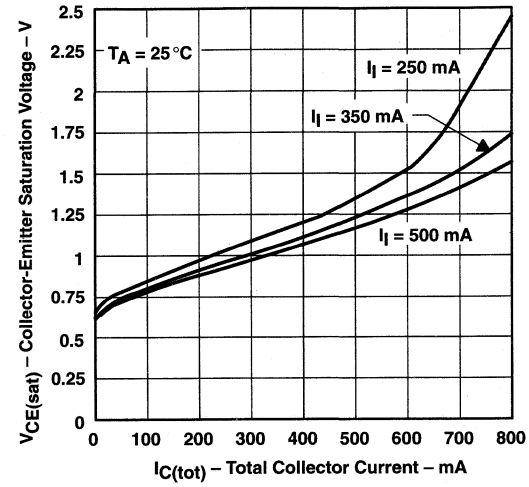


Figure 12

COLLECTOR CURRENT vs INPUT CURRENT

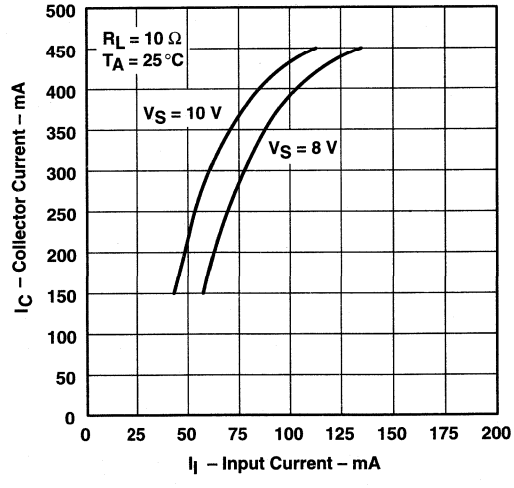


Figure 13

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

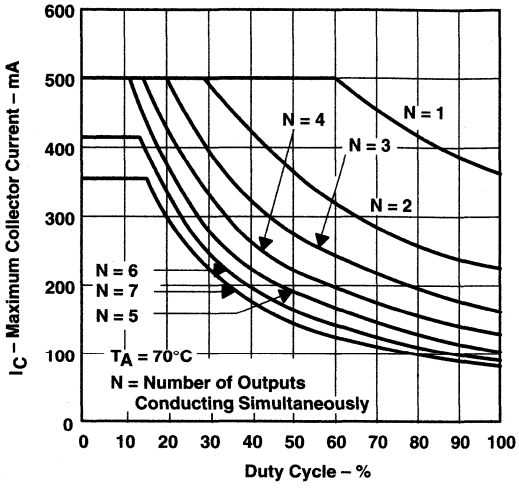


Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

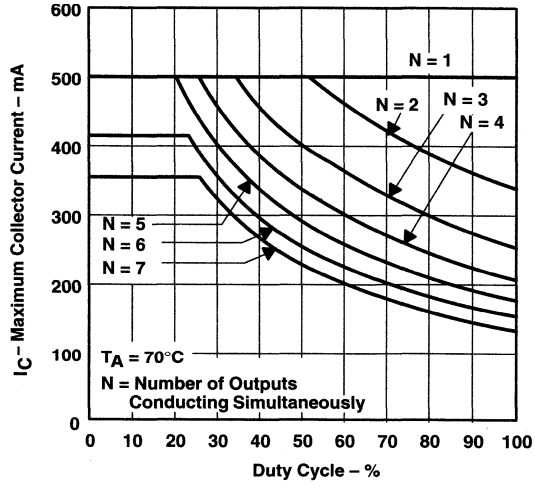


Figure 15

APPLICATION INFORMATION

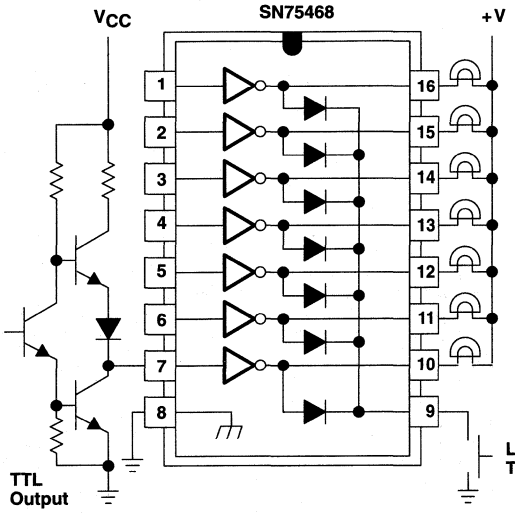


Figure 16. TTL to Load

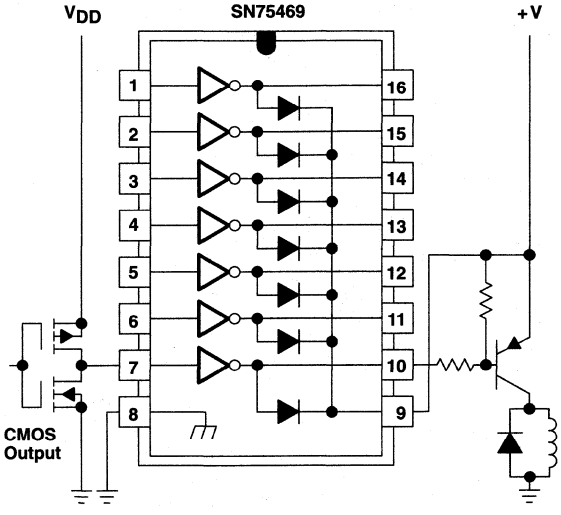


Figure 17. Buffer for Higher Current Loads

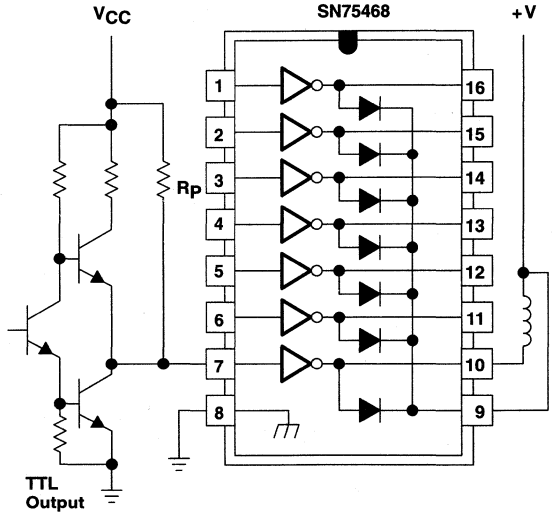


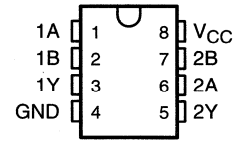
Figure 18. Use of Pullup Resistors to Increase Drive Current

SLRS024 – DECEMBER 1976 – REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE HIGH-CURRENT DRIVER APPLICATIONS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability**

D OR P PACKAGE
(TOP VIEW)



SUMMARY OF SERIES SN75471

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN75471	AND	D, P
SN75472	NAND	D, P
SN75473	OR	D, P

description

Series SN75471 dual peripheral drivers are functionally interchangeable with series SN75451B and series SN75461 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than series 75451B (limits are the same as series SN75461). Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN75471, SN75472, and SN75473 are dual peripheral AND, NAND, and OR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

Series SN75471 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Inter-emitter voltage (see Note 2) ..... 5.5 V
Off-state output voltage, V_O ..... 70 V
Continuous collector or output current (see Note 3) ..... 400 mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3) ..... 500 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to the network GND, unless otherwise specified.
2. This is the voltage between two emitters, A and B.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

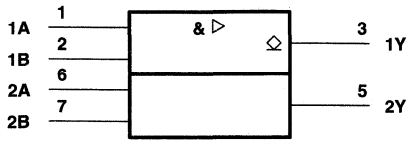
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

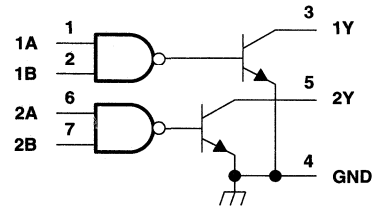
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

SN75471 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN75471 logic diagram (positive logic)

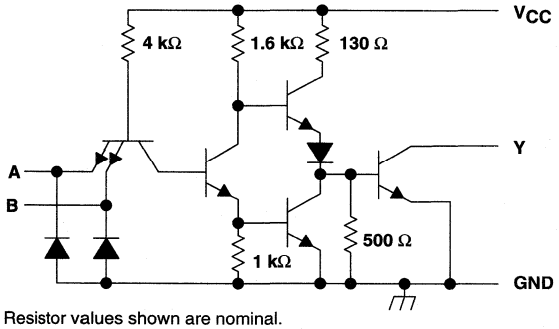


SN75471 FUNCTION TABLE (each driver)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
$Y = AB$ or $\overline{A} + \overline{B}$

SN75471 schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

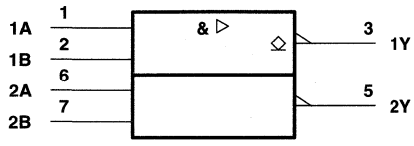
PARAMETER		TEST CONDITIONS			SN75471 MIN	SN75471 TYP‡	SN75471 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V,	V_{IH} = 2 V,	V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 5 V			7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 0			52	65	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

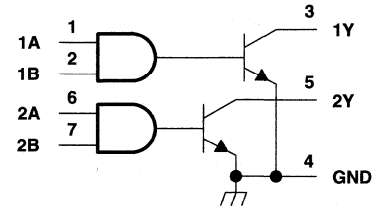
PARAMETER		TEST CONDITIONS			SN75471 MIN	SN75471 TYP	SN75471 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, R_L = 50 Ω,		C_L = 15 pF, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output					25	40	
t_{TLH}	Transition time, low-to-high-level output					8	20	
t_{THL}	Transition time, high-to-low-level output					10	20	
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 2		$I_O \approx$ 300 mA,	V_S−18			mV

SN75472 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN75472 logic diagram (positive logic)

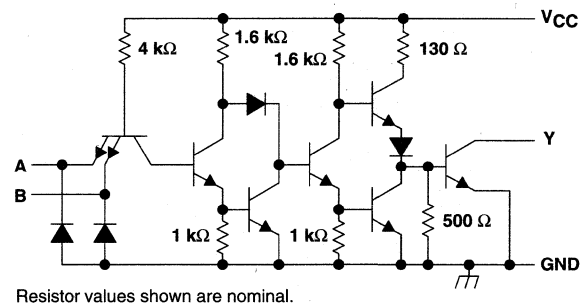


SN75472 FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

SN75472 schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

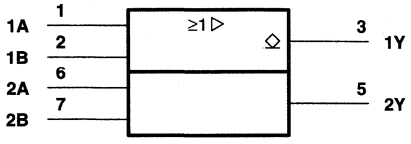
PARAMETER		TEST CONDITIONS			SN75472 MIN	SN75472 TYP‡	SN75472 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V,	V_{IH} = 2 V,	V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 5 V			13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 0			61	76	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

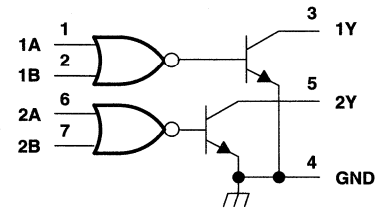
PARAMETER		TEST CONDITIONS			SN75472 MIN	SN75472 TYP	SN75472 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1			45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output					30	50	
t_{TLH}	Transition time, low-to-high-level output					13	25	
t_{THL}	Transition time, high-to-low-level output					10	20	
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 2	I_O ≈ 300 mA,		V_S−18			mV

SN75473 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN75473 logic diagram (positive logic)

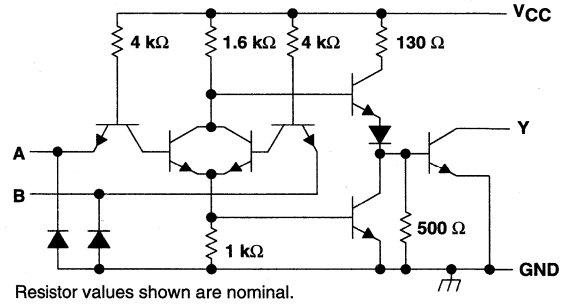


SN75473 FUNCTION TABLE (each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{A}\,\overline{B}$

SN75473 schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

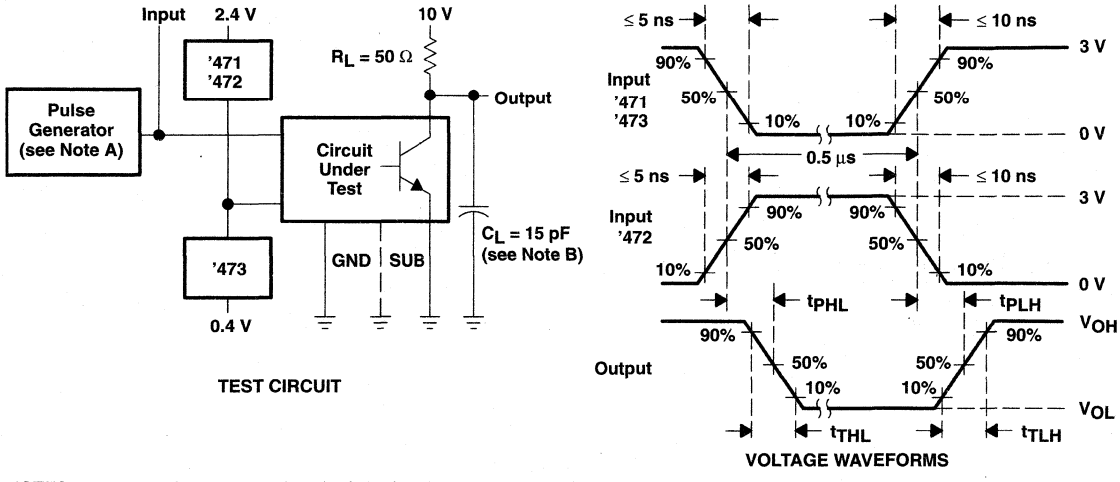
PARAMETER		TEST CONDITIONS			SN75473 MIN	SN75473 TYP‡	SN75473 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V,	V_{IH} = 2 V,	V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 5 V			8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 0			58	76	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

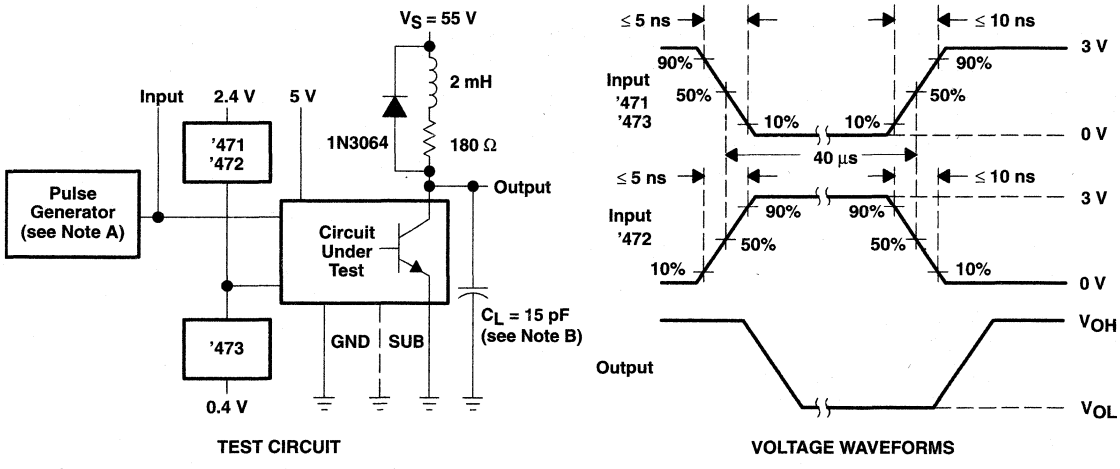
PARAMETER		TEST CONDITIONS			SN75473 MIN	SN75473 TYP	SN75473 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA,	C_L = 15 pF,			30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 50 Ω,	See Figure 1			25	40	
t_{TLH}	Transition time, low-to-high-level output					8	25	
t_{THL}	Transition time, high-to-low-level output					10	25	
V_{OH}	High-level output voltage after switching	V_S = 55 V,	I_O ≈ 300 mA,	See Figure 2	V_S−18			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Switching Times

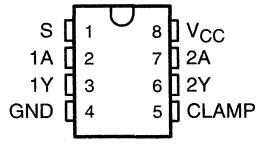


NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test

- **Characterized for Use to 300 mA**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **High-Voltage Outputs (100 V Typ)**
- **Output Clamp Diodes for Transient Suppression (300 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **pnp Transistor Inputs Reduce Input Current**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**
- **Plastic DIP (P) With Copper-Lead Frame Provides Cooler Operation and Improved Reliability**

D OR P PACKAGE
(TOP VIEW)

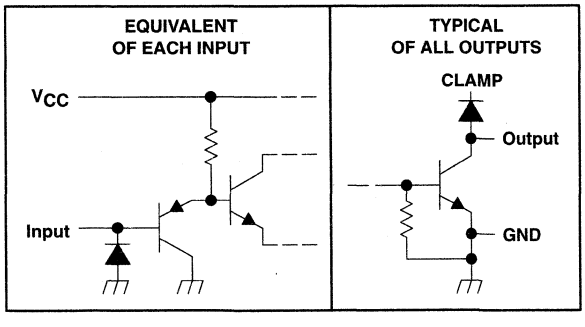


description

The SN75476 through SN75478 are dual peripheral drivers designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, and SN75478 provide AND, NAND, and OR drivers respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, and SN75478 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



Function Tables

SN75476
(each AND driver)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75477
(each NAND driver)

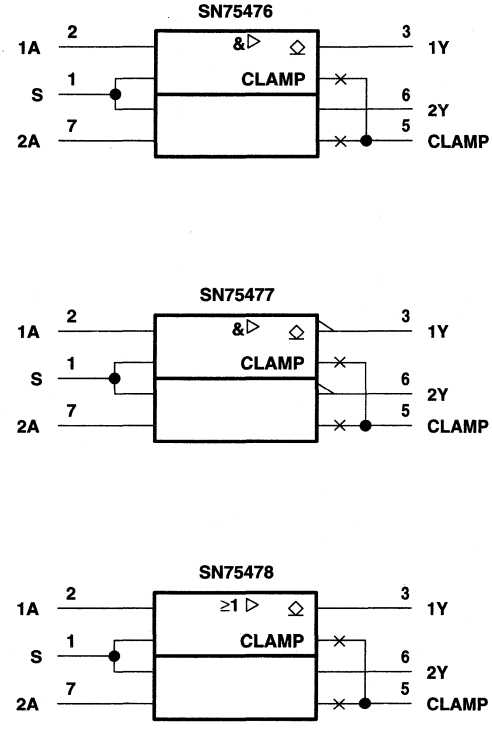
INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75478
(each OR driver)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

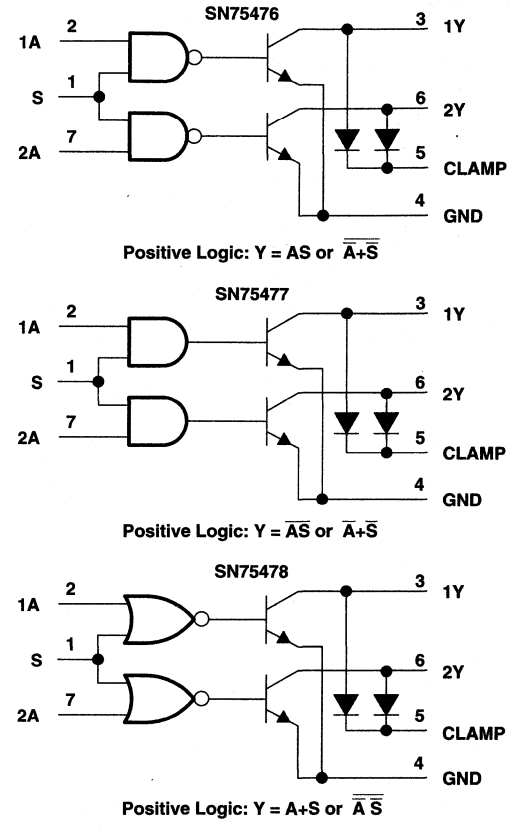
H = high level, L = low level
X = irrelevant

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagrams (positive logic)



Positive Logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$

Positive Logic: $Y = \overline{A}S$ or $\overline{A}+\overline{S}$

Positive Logic: $Y = A+S$ or $\overline{\overline{A}\,\overline{S}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 400 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$ . . . . . 500 mA
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp current, I_{OK} . . . . . 400 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous power dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

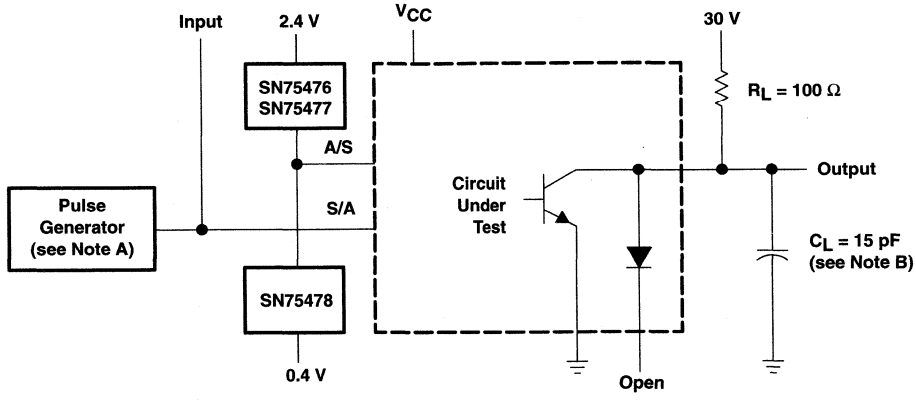
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –12 mA			–0.95	–1.5	V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 100 mA		0.16	0.3	V
				I_{OL} = 175 mA		0.22	0.5	
				I_{OL} = 300 mA		0.33	0.6	
$V_{O(BR)}$	Output breakdown voltage		V_{CC} = 4.5 V,	I_{OH} = 100 μA	70	100		V
$V_{R(K)}$	Output clamp reverse voltage		V_{CC} = 4.5 V,	I_R = 100 μA	70	100		V
$V_{F(K)}$	Output clamp forward voltage		V_{CC} = 4.5 V,	I_F = 300 mA	0.8	1.15	1.6	V
I_{OH}	High-level output current		V_{CC} = 4.5 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	μA
I_{IH}	High-level input current		V_{CC} = 5.5 V,	V_I = 5.5 V		0.01	10	μA
I_{IL}	Low-level input current	A input	V_{CC} = 5.5 V,	V_I = 0.8 V		–80	–110	μA
		S input				–160	–220	
I_{CCH}	Supply current, outputs high	SN75476	V_{CC} = 5.5 V	V_I = 5 V		10	17	mA
		SN75477		V_I = 0		10	17	
		SN75478		V_I = 5 V		10	17	
I_{CCL}	Supply current, outputs low	SN75476	V_{CC} = 5.5 V	V_I = 0		54	75	mA
		SN75477		V_I = 5 V		54	75	
		SN75478		V_I = 0		54	75	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

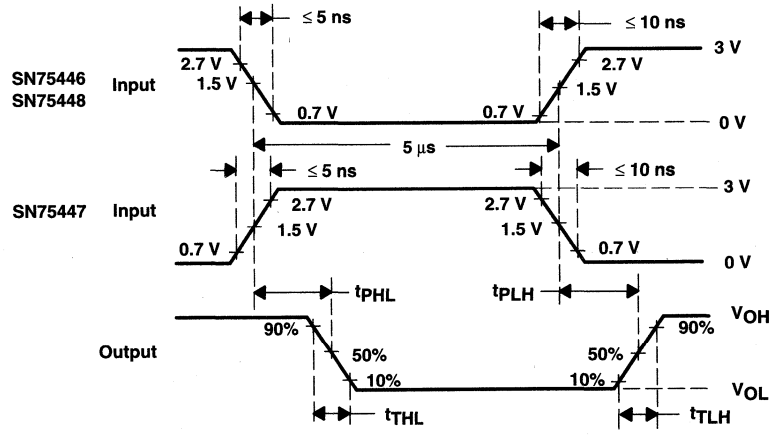
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Figure 1		200	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	350	ns
t_{TLH}	Transition time, low-to-high-level output			50	125	ns
t_{THL}	Transition time, high-to-low-level output			90	125	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O ≈ 300 mA, See Figure 2	V_S–18			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

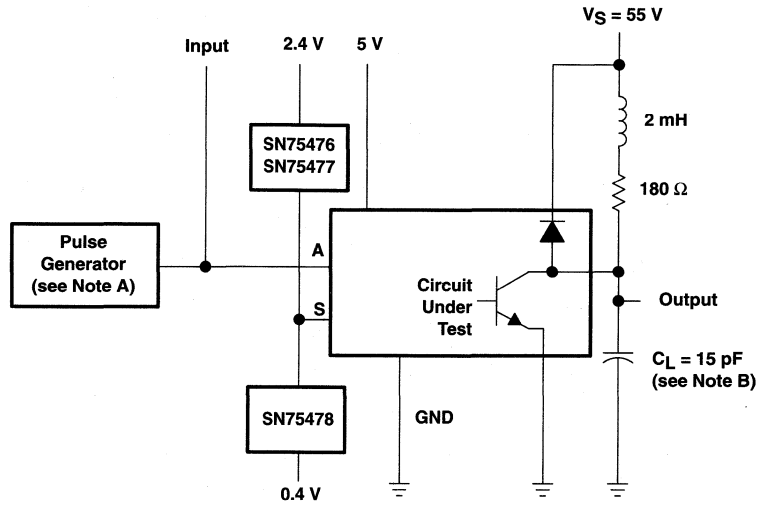


VOLTAGE WAVEFORMS

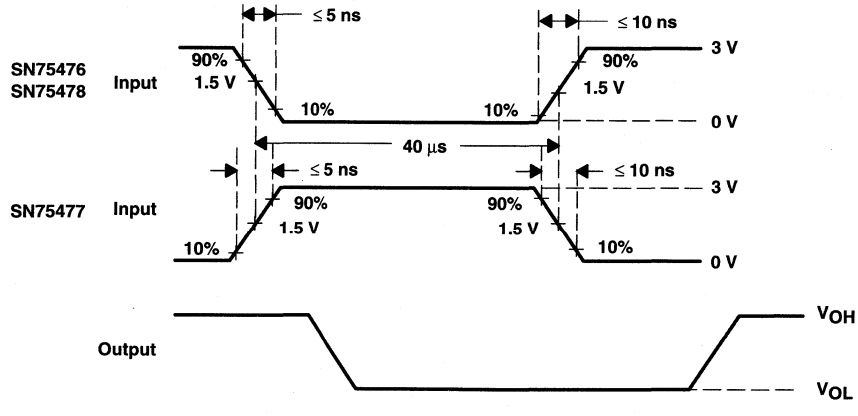
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

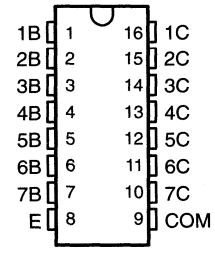
Figure 2. Latch-Up Test Circuit and Voltage Waveforms

SLRS027 – DECEMBER 1976 – REVISED APRIL 1993

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Designed to Be Interchangeable With Sprague ULN2001A Series**

D OR N PACKAGE
(TOP VIEW)

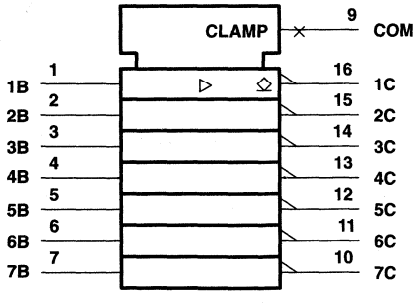


description

The ULN2001A, ULN2002A, ULN2003A, and ULN2004A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

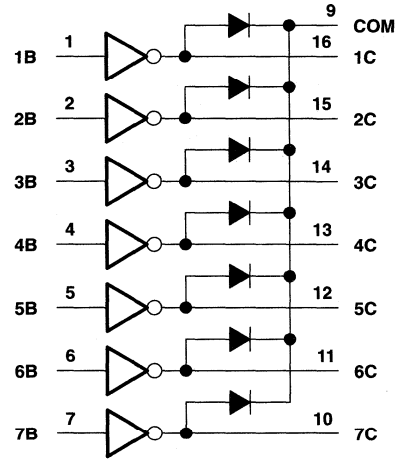
The ULN2001A is a general-purpose array and can be used with TTL and CMOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V PMOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A.

logic symbol†

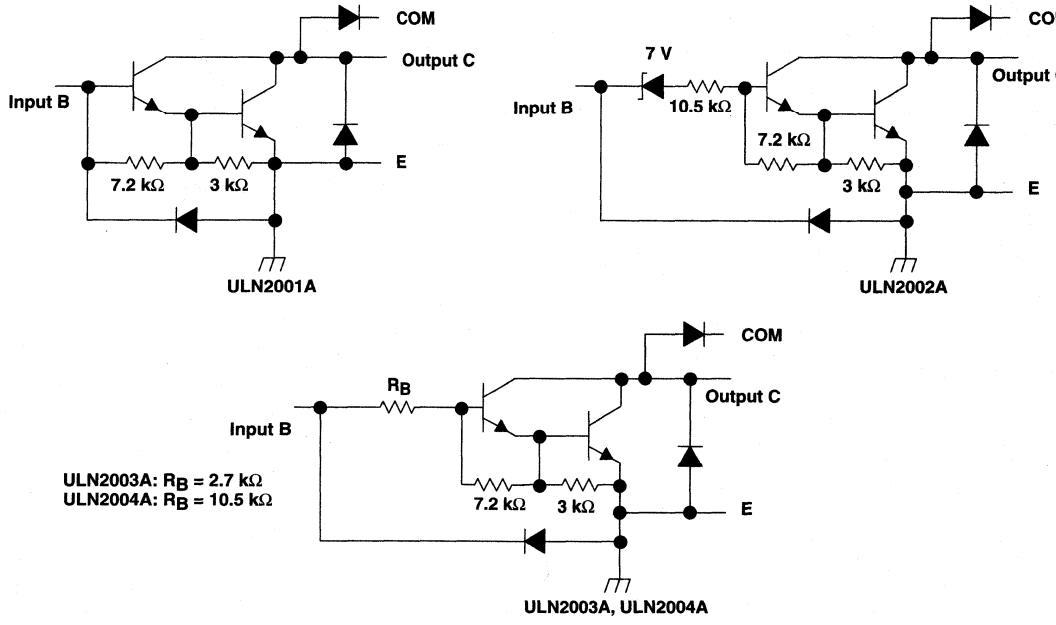


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	50 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−20°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2001A			ULN2002A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
I_R	Clamp reverse current	7	V_R = 50 V,	T_A = 70°C			100			100	µA
			V_R = 50 V				50			50	
h_{FE}	Static forward current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 1 V						500	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	7	V_R = 50 V				50			50	µA
			V_R = 50 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

switching characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	µs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, $I_O \approx$ 300 mA, See Figure 10	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

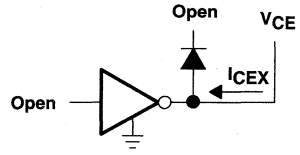


Figure 1. I_{CEX} Test Circuit

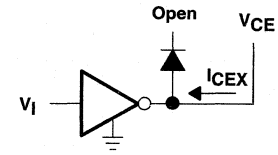


Figure 2. I_{CEX} Test Circuit

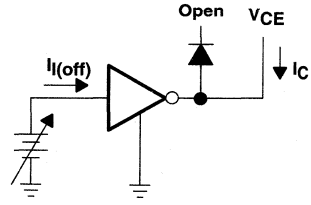


Figure 3. $I_{I(off)}$ Test Circuit

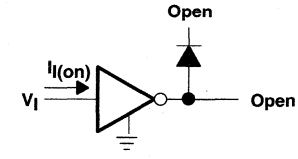
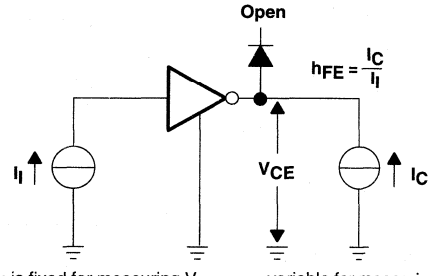


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

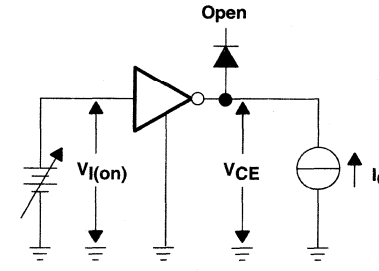


Figure 6. $V_{I(on)}$ Test Circuit

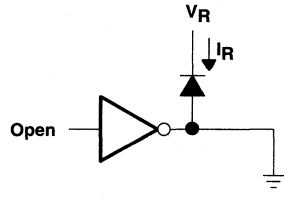


Figure 7. I_R Test Circuit

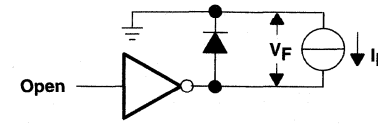
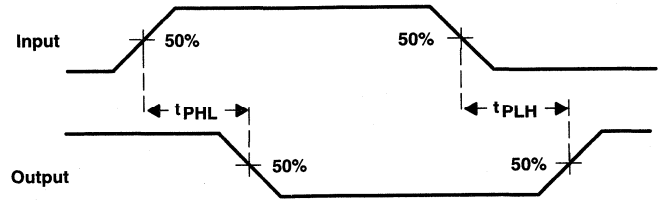


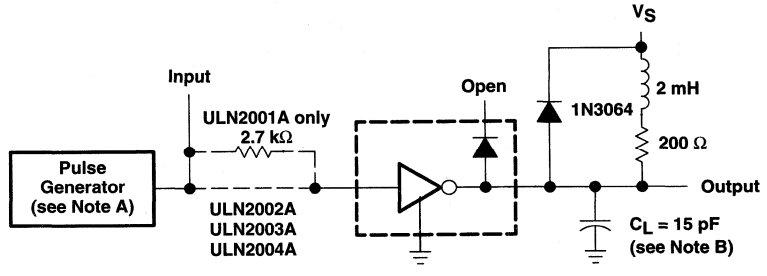
Figure 8. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION

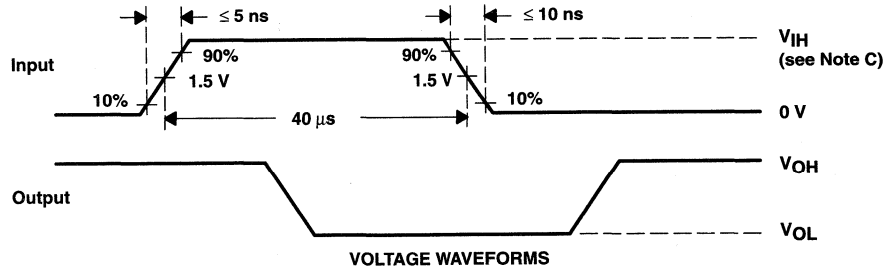


VOLTAGE WAVEFORMS

Figure 9. Propagation Delay Time Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A and the ULN2003A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
COLLECTOR CURRENT
(ONE DARLINGTON)

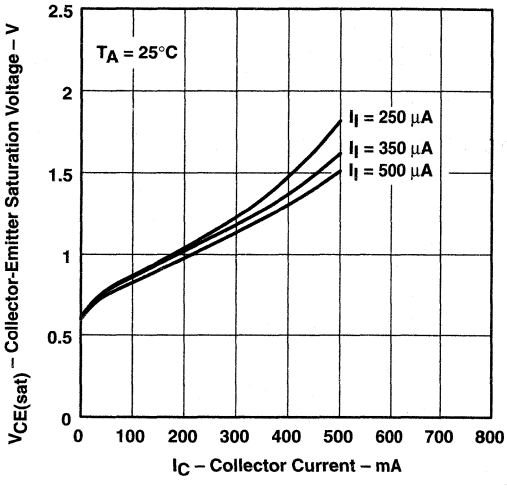


Figure 11

COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
TOTAL COLLECTOR CURRENT
(TWO DARLINGTONS PARALLELED)

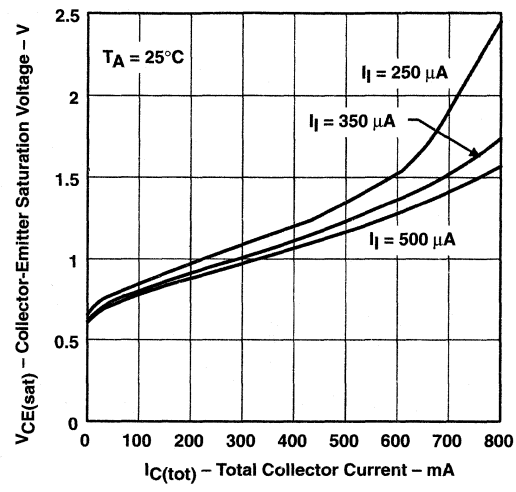


Figure 12

COLLECTOR CURRENT
vs
INPUT CURRENT

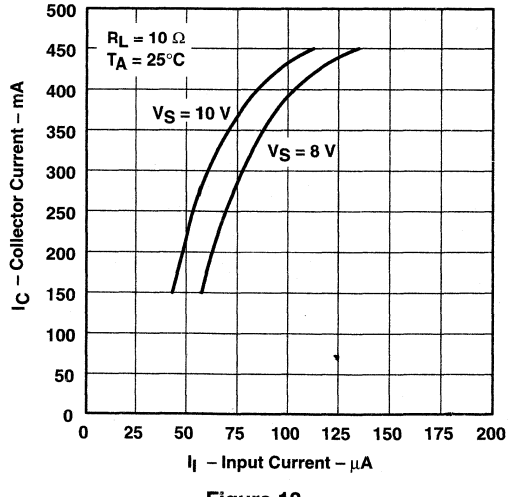


Figure 13

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

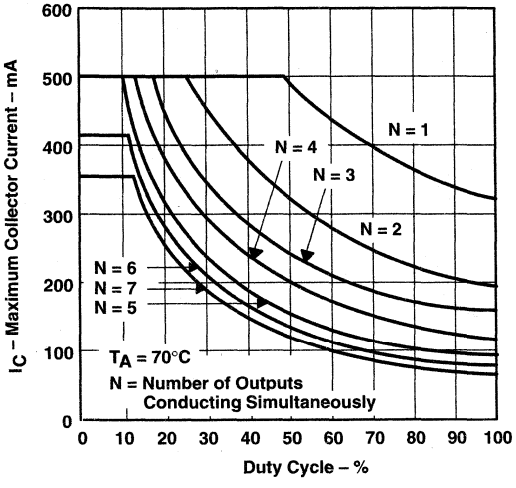


Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

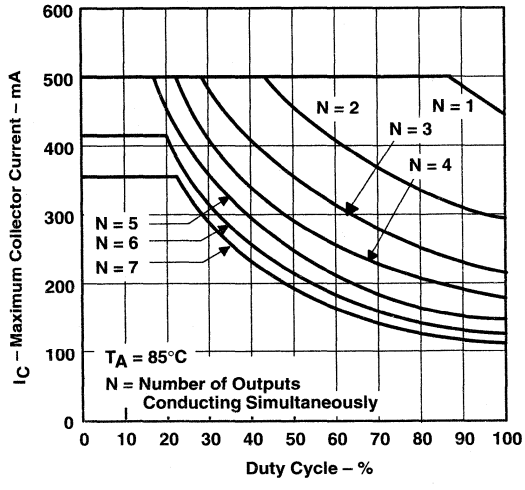


Figure 15

APPLICATION INFORMATION

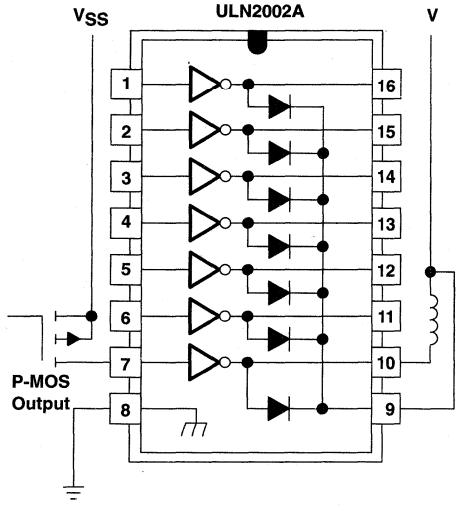


Figure 16. P-MOS to Load

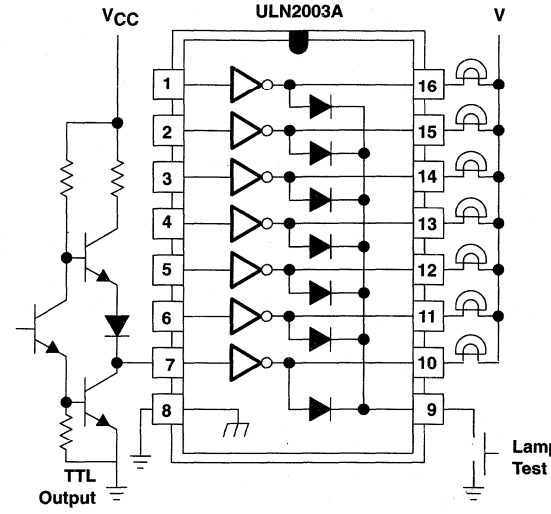


Figure 17. TTL to Load

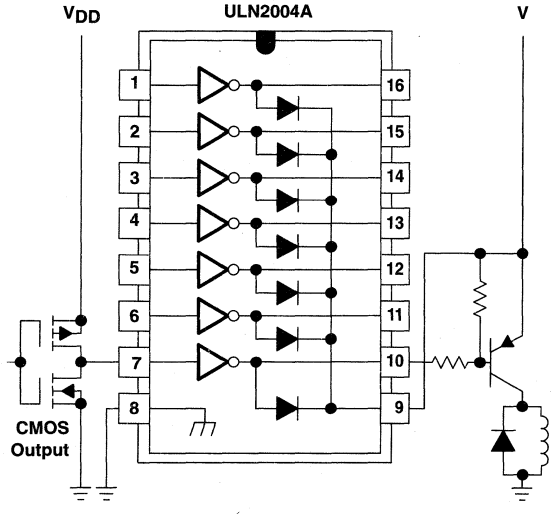


Figure 18. Buffer for Higher Current Loads

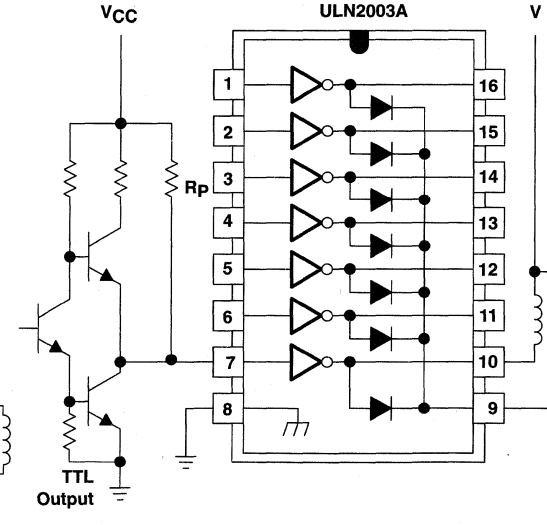


Figure 19. Use of Pullup Resistors to Increase Drive Current

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Power System

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Introduction

The output section of a control system serves as the interface between electrical control signals and the real world. The end product of the output section is the control of a real-world function such as motion, light, sound, or any number of other physical actions. Control systems vary greatly in their complexity from controlling a simple single action to complex interactive systems with multiple feedback signals, fault isolation, and adaptive software. Regardless of the system complexity, an output system is normally employed to complete the interface between the control system and the real world (see Figure 1).

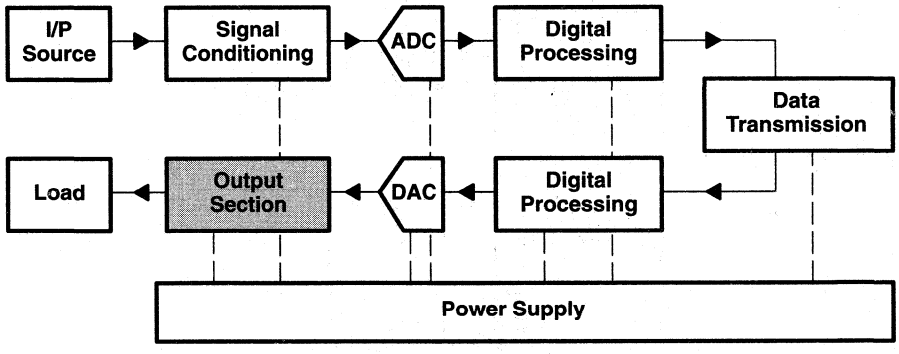


Figure 1. Output Section

Figure 2 represents a generalized output system consisting of a controller, an interface circuit, and a load. The design problem addressed is controlling the operation of a load with a small signal. Several typical loads such as motors, solenoids, speakers, and lamps are shown. For most of the loads, several signal paths exist from the controller through the interface circuits; each path represents a solution to one specific design problem. Although multiple solutions exist, they may not all be the best solution. The next section discusses the methodology for designing an output system that is well suited for a particular application.

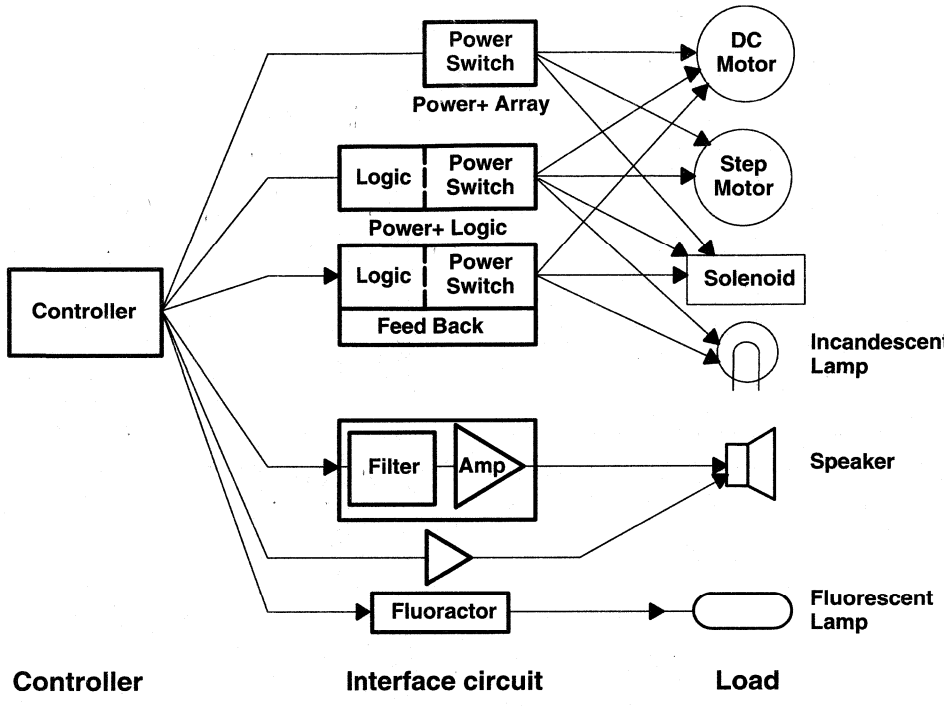


Figure 2. Generic Output Systems

Output System Design

Selection of a Load Device

The first step is to select a load. Selecting the load involves defining the type of output energy needed, selecting the proper class of load, and selecting the correct size load. Table 1 depicts some energy types with the corresponding load and output parameters. A dc motor, for example, usually has an output specification that is in terms of torque at a given speed. Matching the mechanical requirements for a particular application is outside the scope of this discussion. Assume a suitable load can be selected.

Table 1. Select a Load

ENERGY OUTPUT	LOAD	LOAD OUTPUT SPECIFICATIONS
Rotating Motion		
Continuous	DC Motor	HP – Torque – RPM
Incremental	Stepper Motor	Torque – Step Speed
Linear Motion	Solenoid	Ft-Lbs – Inches
Light	Incadescant Lamp	Watts – Lumens
	Fluorescent Lamp	Watts – Lumens
Sound	Loudspeaker	Watts – Hertz

The second step is evaluation of the input requirements for a particular load. Load input specifications address the voltage and current requirements during normal operation. Normal operation includes load switching (turn on, turn off, and accompanying transients). Often the behavior of a load during switching is not adequately specified and must be characterized for the specific application. Understanding load input requirements leads to the interface circuit requirements.

Interface Circuit Requirements

Assumed that the interface circuit is a switch, the following information can be used to select the correct switch.

Motors, solenoids, lamps, and other assorted loads are generally specified by operating voltage and current with a specified power output. The information provided is sufficient for operating at continuous duty cycle; however, in most applications, the load is switched on and off. When switching loads, the operating requirements, as well as transient conditions, must be considered. The power requirements are often further influenced by dynamic operating conditions.

Figure 3 shows an example of a load operating from a battery and controlled by a low-side switch. This helps to determine the need to design the switch and evaluate the system.

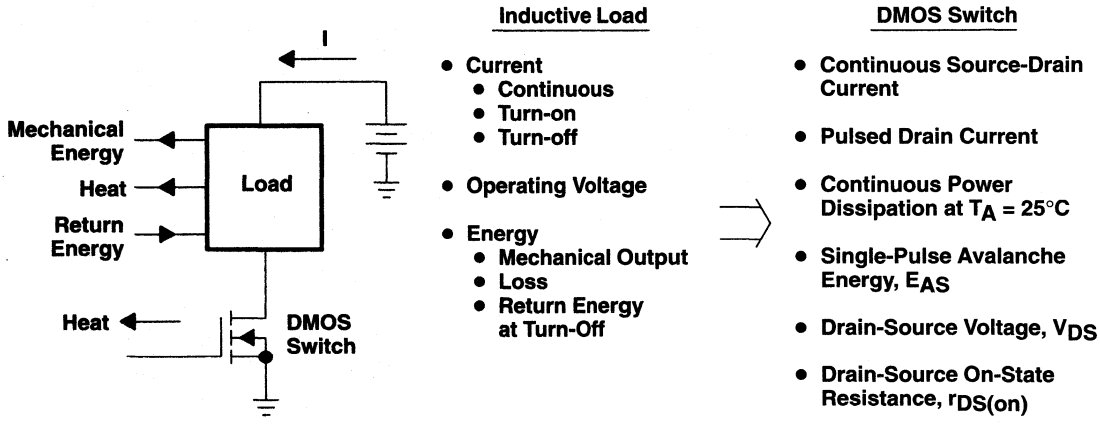


Figure 3. Inductive Load Switch Requirements

The system power supply and load choice determine:

- Current drawn from the battery, including transients when the switch is turned on and off
- Battery terminal voltage
- Energy output from the load (motion, sound, etc.)
- Energy dissipated from the load in the form of heat (IR loss, magnetic loss, friction)
- Energy returned to system (inductive, regeneration, cross coupling)

These system load requirements must then be used to determine the switch requirements:

- Continuous source-drain current
- Pulsed drain current
- Continuous power dissipation at $T_A = 25°C$
- Single-pulse avalanche energy, E_{AS} (energy returned to the device from back EMF)
- Drain-source voltage, V_{DS}
- Drain-source on-state resistance, $r_{DS(on)}$

Selecting or designing a switch is a three-step process; determine the total energy, current, and voltage required, select a switching device that accommodates the energy, and evaluate the system power dissipation to determine any heat-sinking requirements.

Determine Total Energy

Determining the total energy begins with evaluating load current during operation and switching. Figure 4 shows the current waveforms for an incandescent lamp, a solenoid, and a stepper motor. This diagram depicts steady-state and switching conditions, which must be considered in controlling a load.

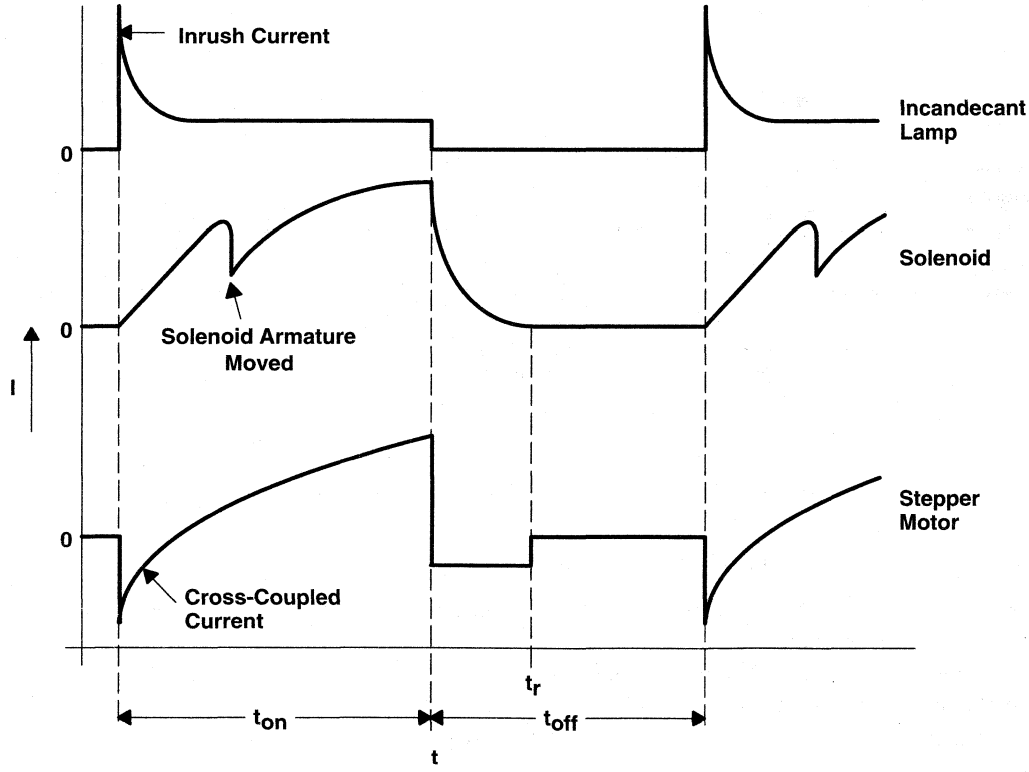


Figure 4. Switching Load Currents

The incandescent lamp current shows a high inrush value at turn on (t_{on}), decreasing to a steady current value; the current remains at this value until turn off (t_{off}). Upon t_{off}, the current drops to zero. The high inrush is due to the difference in filament resistance when cold and hot. A lamp control switch needs to withstand high peak currents or limit the current until the lamp filament warms up.

The solenoid current increases starting at t_{on} and continues to increase until t_{off}. Upon t_{off}, the current steadily drops until t_r. The change in current slope between t_{on} and t_{off} is caused by the solenoid armature moving closer to the coil and increasing the coil inductance. The current flow between t_{off} and t_r is a result of the magnetic field in the solenoid collapsing and returning energy to the system. A Solenoid switch must be capable of conducting the coil operating current and the system must provide a method for accommodating the energy returned to the system at turn off. Several methods are employed to deal with the returned energy. When this energy is dissipated in the switch, it is referred to as avalanche energy.

The stepper motor exhibits an exponential current increase characteristic of an inductive load. Return energy is a factor in stepper motor control. Additionally, stepper motor windings can produce currents as a result of cross coupling from adjacent motor windings. A control circuit for a stepper motor, such as one depicted in Figure 4, must accommodate for the transient energy at turn on and the returned energy at turn off.

Once the load characteristics are determined, energy calculations can follow.

Energy and Power Calculations for an Inductive Load

Power-on time MOSFET dissipation

$$P_{on} = \frac{1}{3}\left(I_P^2\right) r_{DS(on)}\, d$$

For

$$\frac{L}{R_L} > t_{on}$$

Back EMF energy

$$E_T = \frac{3\, L\, I_P^2\, V_{CL}}{6\left(V_{CL} - V_{SS}\right) + 4R_L I_P}$$

Power off dissipation

$$P_{off} = E_T\, f$$

Total average switch power dissipation

$$P_T = \left(P_{on} + P_{off}\right)n + P_{(quies)}$$

L	= Load inductance
I_P	= Peak drain current
V_{CL}	= Max output clamp voltage
V_{SS}	= Load supply voltage
R_L	= Inductor resistance
f	= Switching frequency
d	= Duty cycle (ratio)
$r_{DS(on)}$	= Drain-to-source on-resistance
n	= Total number of switches operating
$P_{(quies)}$	= Quiescent power dissipation of switch circuit
t_{on}	= Switch on time

The intent is to calculate the total power dissipated in the transistor switch.

During the power-on time, the inductor current approximates to a linear ramp assuming the inductor L/R_L time constant is greater than the turn-on time (t_{on}). This results in a mean square drain current of 1/3 I_P^2 with I_P equal to the peak drain current. Therefore, the average power dissipated in the output MOSFET (P_{on}) is equal to:

$$P_{on(av)} = \frac{1}{3} \cdot \left(I_P^2\right) \cdot r_{DS(on)} \cdot d$$

This assumption is applicable to the stepper motor waveform in Figure 4, but does not work for the solenoid. The solenoid time constant (L/R_L) is less than t_{on}; therefore, P_{on} is greater than that calculated above.

When the output MOSFET is turned off, the back EMF generated by the inductor raises the drain voltage, which must be clamped either externally or internally. External clamping is normally accomplished with a snubber diode; internal clamping is also accomplished with a zener diode. The clamp voltage (V_{CL}) is also called avalanche voltage.

The equation to define avalanche energy is:

$$E_T = \left(3 \cdot L \cdot I_P^2 \cdot V_{CL}\right) / \left[6 \cdot \left(V_{CL} - V_{SS}\right) + 4 \cdot R_L \cdot I_P\right] \text{ JEDEC Standard No. 10}$$

This equation assumes a linear decay of the current in the inductor. A more accurate E_T calculation can be accomplished by integrating the inductor current and clamp voltage in the load. The integration is taken from turn off (t_1) until the inductor current decays to zero. The calculation is as follows:

$$E_T = \int_0^{t_1} V_{CL} \cdot I_L \cdot dt$$

$$I_L = \left[I_P + \frac{\left(V_{CL} - V_{SS}\right)}{R_L}\right] \cdot e^{-\frac{R_L}{L}t} - \frac{\left(V_{CL} - V_{SS}\right)}{R_L}$$

$$I_P = \frac{V_{SS}}{R_L} \cdot \left[1 - e^{-\left(\frac{R_L}{L} \cdot \frac{d}{f}\right)}\right]$$

$$t_1 = \frac{L}{R_L} \cdot \ln\left[1 + \frac{I_P \cdot R_L}{\left(V_{CL} - V_{SS}\right)}\right]$$

$$E_T = V_{CL} \cdot \frac{L}{R_L} \cdot \left[I_P - \frac{\left(V_{CL} - V_{SS}\right)}{R_L} \cdot \ln\left[1 + \frac{I_P \cdot R_L}{\left(V_{CL} - V_{SS}\right)}\right]\right]$$

The power dissipated during the turn-off period (P_{off}) can be equated to the product of E_T and the frequency of switching.

$$P_{off} = E_T \cdot f$$

Hence, the total power (P_T) dissipated in an integrated switch with multiple output sections is:

$$P_{T(av)} = \left(P_{off} + P_{on}\right) \cdot n + P_{(quies)}$$

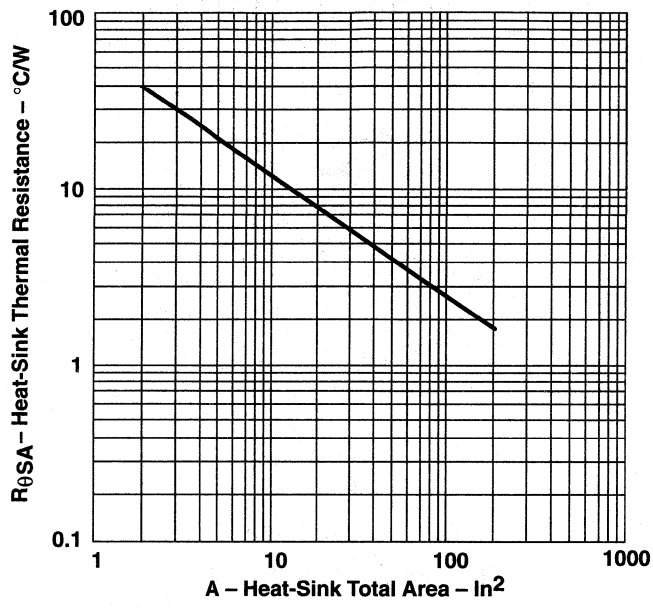
This is the average power dissipation for multiple sections whose duty cycles have a fixed time relationship to each other. For multiple outputs with variable duty cycles, the power calculation becomes more difficult.

Where:

E_T = Total turn-off transient energy absorbed
f = Switching frequency
d = Duty cycle
L = Load inductance
I_P = Peak output load current
n = Number of output switches operating
P_{off} = Turn-off power dissipation in each switch
P_{on} = On-state power dissipation in each switch
$P_{(quies)}$ = Interface device bias power dissipation
$P_{T(av)}$ = Average total power dissipation
R_L = Resistance of inductor
V_{CL} = Clamp voltage
V_{SS} = Load supply voltage

Thermal Considerations

When the total power dissipation for the device is calculated, thermal evaluation can proceed. The objective is to determine if external heat sinking is required. Figure 5 shows a standard heat sink curve.



Max Power Dissipation

$$P_{MAX} = \frac{\left(T_{J(max)} - T_A\right)}{R_{\theta JA}}$$

Thermal Resistance

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(av)}} - \left|R_{\theta JC} + R_{\theta CS}\right|$$

Where:

$R_{\theta SA}$ = Heat sink-to-ambient thermal resistance, °C/W
$R_{\theta JC}$ = Device junction-to-case thermal resistance,
= 3°C/W
$R_{\theta CS}$ = Case-to-heat sink thermal resistance,°C/W
= 0.5°C/W typical with thermal joint compound
$P_{T(av)}$ = Total average power dissipation, W
T_J = Junction operating temperature, °C
T_A = Operating ambient temperature, °C

Figure 5. Thermal Considerations for Power Switches

The requirement for external heat sinking is calculated based on the device's total average power dissipation, maximum junction temperature, and ambient operating temperature. The maximum power that can be dissipated in a device (P_D) can be determined as follows:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

Where:

T_J = Maximum device junction operating temperature, °C
T_A = Maximum ambient operating temperature, °C
$R_{\theta JA}$ = Junction-to-ambient thermal resistance, °C/W

T_J and $R_{\theta JA}$ are taken from the device specification and T_A is determined by the application environment.

Heat Sink Requirement

If the total power dissipated in the device (P_T) exceeds the maximum power dissipation (P_D), then a heat sink must be used or a different device must be selected.

A heat sink size can be determined by first calculating the required heat sink-to-ambient thermal resistance ($R_{\theta SA}$) as follows:

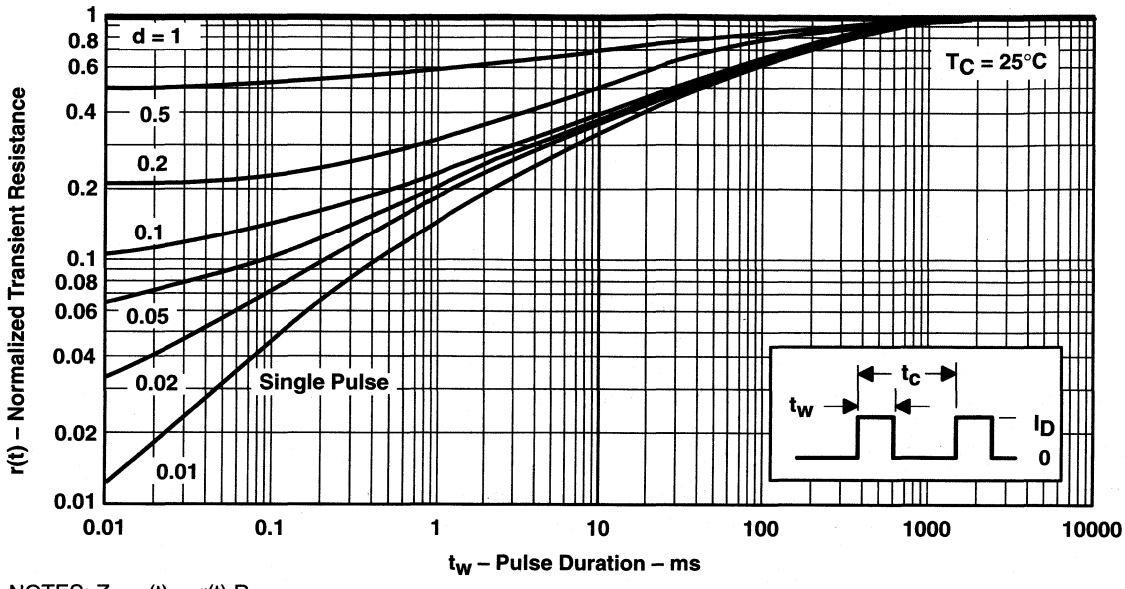
$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(av)}} - |R_{\theta JC} + R_{\theta CS}|$$

Where:

$R_{\theta JC}$ = Device junction-to-case thermal resistance, °C/W
$R_{\theta CS}$ = Case to-heat sink thermal resistance, °C/W
= 0.5°C/W typical with thermal joint compound
$P_{T(av)}$ = Total average power dissipation, W
T_J = Junction operating temperature, °C
T_A = Operating ambient temperature, °C

The $R_{\theta SA}$ required can now be compared to heat sink design specifications to determine the design type and size required.

The preceding thermal calculations are based on the assumption that the device average power is duty cycle dependent. This is true if the pulse widths are short in relation to the device thermal time constant. In the example of a switch that is on for one hour in every twenty four hours, the actual duty cycle is low but the system must be designed to accommodate 100% on time for the switch. The graph in Figure 6 gives the times associated with the Power+ Arrays.



NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_W = pulse duration
t_C = period
d = duty cycle = t_W/t_C

Figure 6. Power+ Arrays Thermal Impedance Characteristics

Conclusion

To summarize the process, begin with selection of a load based on the load output specifications. System energy can then be calculated based on the load characteristics and load input specifications. A switching device can then be selected based on power and energy calculations. A thermal analysis based on the selected device thermal specifications determine if additional heat sinking and external circuitry for back EMF energy dissipation is required.

The design of the switch section is complete when actual measurements from the system are used to verify the design. This design flow is summarized in Figure 7.

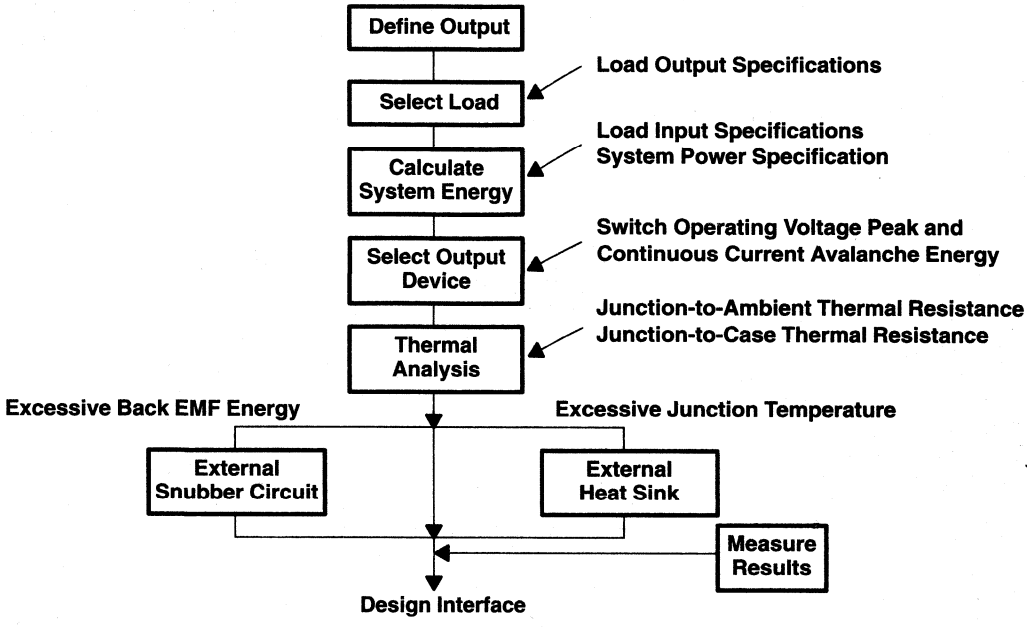


Figure 7. Output Switch Design Flow

Stepper Motor Application

Stepper motors are often chosen to provide incremental rotating motion. Some typical applications are printers, copiers, and industrial robots. Stepper motors present a multiple phase inductive load to the output circuit.

Figure 8 shows a block diagram of the application. The motor chosen has unipolar windings, which require a peak current of 1 A.

- **Control Signal Interface**
  - **Serial Bus From ASIC**
  - **CMOS Logic Levels**
- **Load Definition**
  - **Stepper Motor**
  - **Permanent Magnet Rotor**
  - **Unipolar Windings**
  - **Current 1-A Peak/Winding**
- **Design Considerations for Interface**
  - **Peak Current (1 A)**
  - **Recirculating Current**
  - **Power Dissipation**

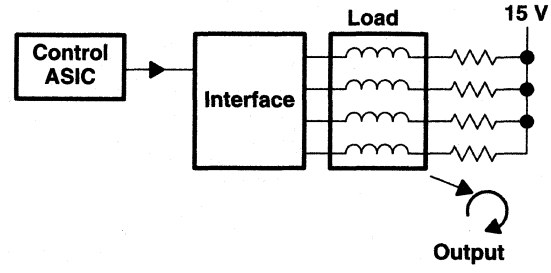


Figure 8. Stepper Motor Application

Load Description

The first consideration in designing this application is to consider the load, which in this case is a Superior Electric stepper motor. The permanent magnet rotor stepper motor has two forms of stator winding. The bipolar stepper motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar stepper motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by interface devices with open-drain outputs. The motor chosen for this application has unipolar windings. Due to the manner in which the windings are constructed when one winding is turned off, a back EMF voltage is induced both in the winding that was turned off and in the other bifilar winding.

Energy Calculations

Figure 9 shows a timing waveform of the stepper motor. The table in the lower right section shows the winding switching sequence. Additionally, at any step, two windings are energized. With the knowledge that the windings are driven two at a time and by observation of the current waveform, energy can be calculated. The value of back EMF energy remains the same as if it is all returned to one winding.

Observation of the timing diagram indicates t_{on} = 5 ms and that the winding current approximates a linear ramp ($L/R > t_{on}$). This indicates that the simplified formula is a good approximation.

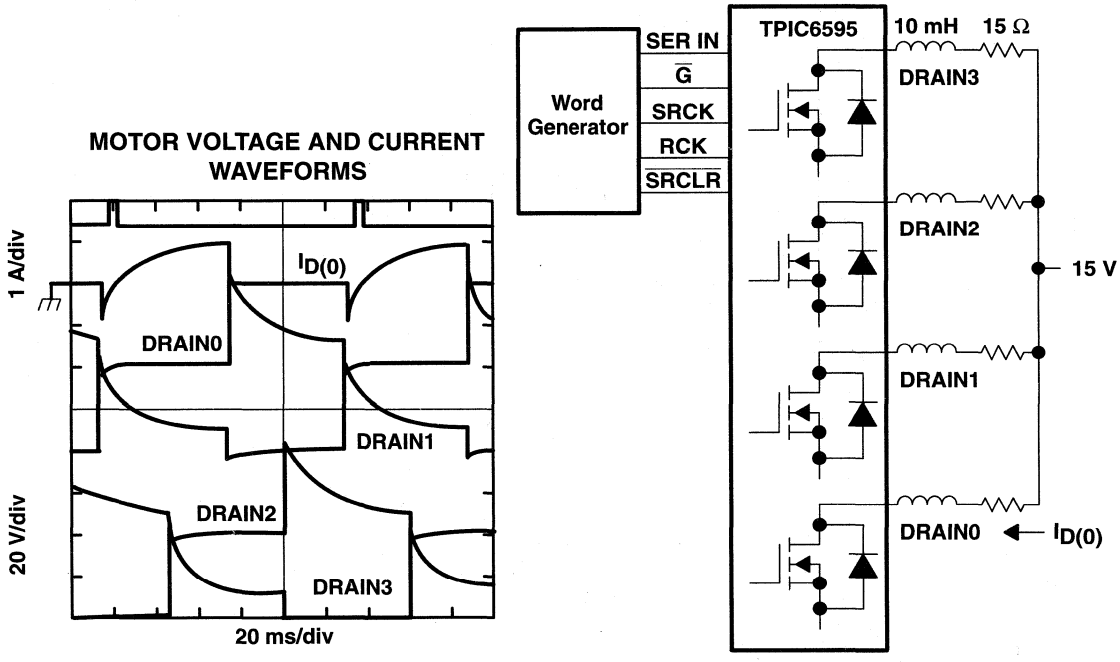
Therefore:

$$P_{on} = \frac{1}{3} \cdot \left(I_P{}^2\right) \cdot r_{DS(on)} \cdot d$$

Where:

d = 0.5 (each winding conducts twice in the four-step cycle)

In this example, if the motor is stopped, the current through each winding is a steady 1 A. The power calculations are based on an assumed operating frequency. If the motor is stopped, the individual drive currents may exceed the maximum continuous current rating of the switches. When calculating energy and power, worst-case assumptions must be considered.



Step	DRAIN0	DRAIN1	DRAIN2	DRAIN3
1	On	Off	On	Off
2	Off	On	On	Off
3	Off	On	Off	On
4	On	Off	Off	On

Figure 9. Stepper Motor Timing Waveforms

Choosing an Interface Circuit

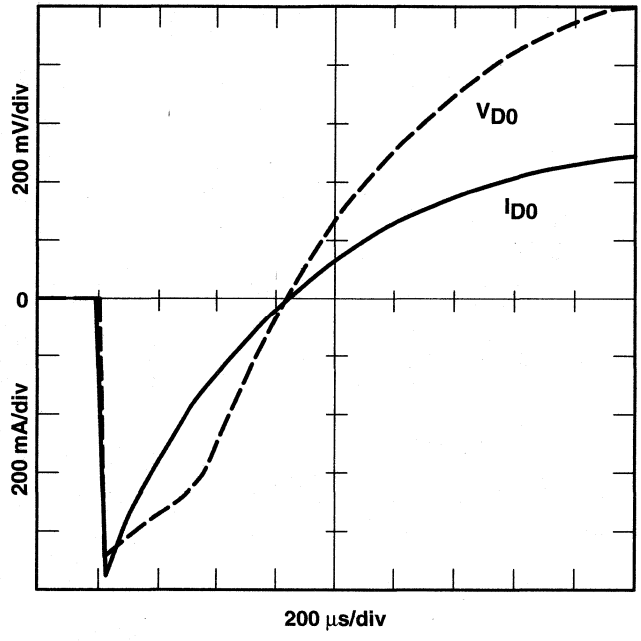
For the application in Figure 9, the TPIC6595 has been chosen. This device was chosen because it can meet the power requirements, can drive all four windings from a single integrated circuit, and includes interface logic.

Figure 9 shows the TPIC6595 driving the stepper motor. The motor is driven at its rated 1 A by operating two output DMOS transistors in parallel. In Figure 9, DRAIN0 is representative of output transistors 1 and 5 in parallel. Similarly, DRAIN1 is representative of output transistors 2 and 6, etc. Anti-parallel

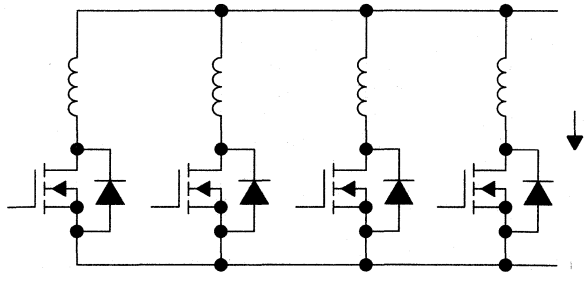
source-drain diodes are included for clarity. In this example, the input logic that would normally be provided by the system's microprocessor, is provided by a Hewlett Packard HP8180 A data generator.

The anti-parallel diodes are used to recirculate the current that is induced in the winding when the current through the previously activated winding on the pole is terminated. Hence, during each motor revolution, both positive and negative current flows through the power switches that control the winding.

Figure 10 shows an expansion of the waveforms of the negative current region of the winding pulse from the stepper motor application.



Current and Voltage Waveforms at Instant of Winding Turn on
(a) SUPERIOR ELECTRIC UNIPOLAR STEPPING MOTOR



- **Reverse current flows through windings at turn-on.**
- **DMOS power transistor conducts in reverse mode, reducing power dissipation.**
- **High peak reverse currents are possible.**

(b) STEPPER MOTOR WINDINGS AND DMOS DRIVERS

Figure 10. TPIC6595 Synchronous Rectification Characteristics

As previously mentioned, the anti-parallel diodes of the DMOS output allow the recirculation of current at winding turn on. It is the anti-parallel diode that allows the DMOS output to withstand high peak reverse currents. In contrast, a power bipolar structure does not benefit from an inherent anti-parallel diode; one must be physically added, either to the integrated circuit design or externally at the board level. If negative currents are required of a bipolar power switch that does not include such a diode, parasitic isolation diodes in the bipolar structure will conduct currents which may cause system malfunction. It is for this reason that a DMOS solution is often the most practical and economical for motor drive applications.

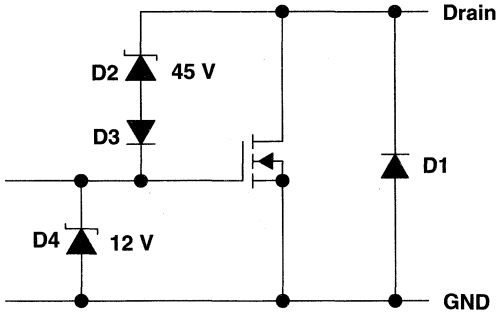
In the stepper motor example, as the winding turns on, the voltage drop across the output decreases. Once the voltage drop across the output ceases to be at least 0.7 V, the body-drain diode no longer conducts. At this point, the DMOS power transistor turns on in the reverse direction, allowing continued negative current flow to the inductor.

Once reverse conduction through the DMOS becomes the vehicle for negative current flow to the inductor, the power dissipation is given by the product of $r_{DS(on)}$ and the square of the drain current. Reverse conduction continues through the DMOS transistor until the current reaches zero.

Benefits of Choosing Power+ Logic

- The DMOS output structure is power efficient.
- The output structure can withstand high avalanche energy.
- System design is simpler than with discrete DMOS or bipolar transistors.

The TPIC6595 device has 8 power DMOS outputs with built-in 45-V clamps for enhanced inductive energy switching capability. Figure 11 shows the typical schematic of each output. When switching inductive loads, high voltage transients are seen at the device output when the output is placed in the high impedance state. The voltage generated by the inductive transient is limited by the breakdown mechanism of the output structure.



TYPICAL SCHEMATIC OF ALL DRAIN OUTPUTS

- **D1 is an integrated body-drain diode.**
- **D2 and D3 are added to provide improved unclamped energy capability.**
- **D4 is added to prevent gate-oxide damage.**

Figure 11. Power+ Logic Output Structure

For the Power+ Logic devices, the internal dynamic 45-V clamp circuit eventually conducts during switching of an unclamped inductive load, allowing current to charge up the gate of the transistor. Once the DMOS gate voltage exceeds the threshold voltage of the device, the DMOS turns back on, completely dissipating the energy from the inductor.

Thus, the entire active area of the DMOS transistor is used in the forward-bias mode to absorb energy from the inductive load. Without the internal clamp circuitry, the device output would be driven into avalanche breakdown and would operate in a much lower energy capability reverse-bias mode. The built-in voltage

clamps of the Power+ Logic devices allow the user to switch up to 75 mJ of avalanche energy without the use of external snubber circuitry.

Each DMOS output of the TPIC6595 can provide 250 mA of continuous current with all outputs turned on. Individually, the outputs can be pulsed to provide up to 1.5 A of current. Multiple outputs can be paralleled for increased current drive of up to 6 A of pulsed total load current. This rating is sufficient to drive the stepper motor when operating at the described duty cycle.

In describing the ruggedness of any power output, a key parameter is the avalanche energy capability. While the maximum energy capability is determined by thermal limitations of the silicon, the energy that can be dissipated during avalanche is not a constant, but varies with peak switching current and load inductance. Some power structures, however, may be prematurely limited by secondary breakdown and will have a constant energy rating. For an inductive switching pulse within the energy capability of the device, the energy dissipated in the output is proportional to the product of the current and voltage waveforms.

Figure 12 benchmarks the ruggedness of the Power+ Logic device against two low-side bipolar devices having comparable voltage capability. Device A has a breakdown voltage of 37 V, while Device B has a breakdown voltage of 50 V. Each bipolar device has approximately twice the output active area as the Power+ Logic device. The data in Figure 12 reflects the last point of output survival just prior to its destruction.

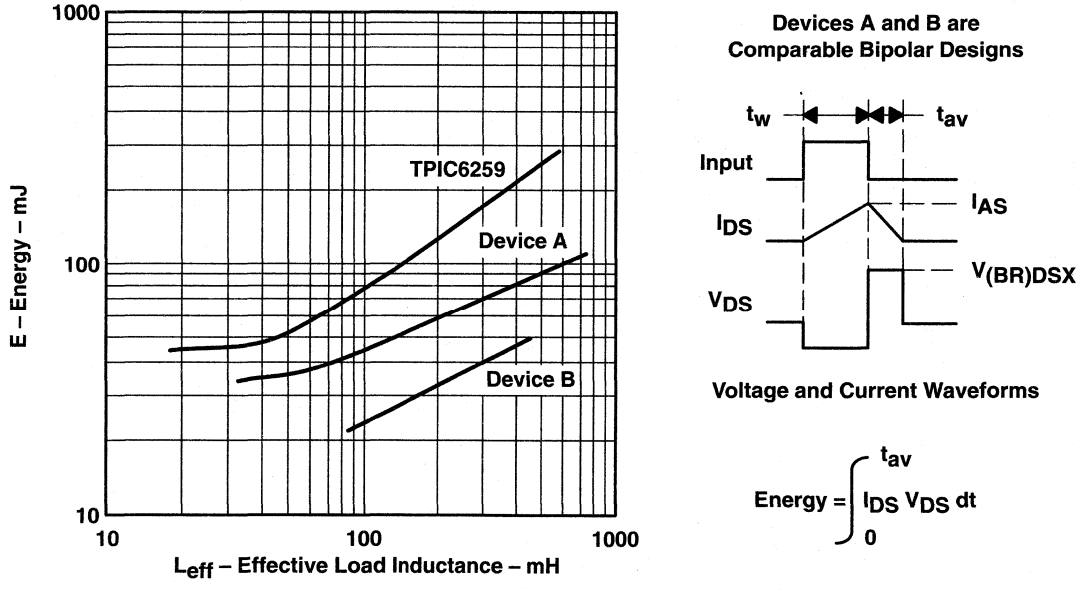


Figure 12. Power+ Logic Versus Bipolar Output Energy

It is evident that the Power+ Logic DMOS device is much more rugged than either of the bipolar structures. While switching a 350-mH inductor, the TPIC6259 dissipates 200 mJ prior to destruction, more than twice the energy of the bipolar devices. While the energy capability of the Power+ Logic device decreases to 45 mJ while switching a 30-mH load, this is still significantly more than comparable bipolar devices.

The following terms and definitions apply to Table 2:

I_{AS} = Peak current reached during device avalanche
t_{av} = Time duration of device in avalanche
L = Load inductance
L_{eff} = Effective load inductance; accounts for supply voltage
E = Energy absorbed by device under test $(L_{eff} \times I_{AS}^2)/2$
V_{DD} = Output supply voltage
V_{DSX} = Effective device avalanche voltage
T_c = Case temperature
T_m = Maximum junction rise that occurs in inductive switching
P_o = Power = $I_{AS} \times V_{DSX}$
K = 139.5 = A thermal constant where the area of active silicon
= 1k mils square.
= $2/(A\ (p\ kc)^{1/2})$

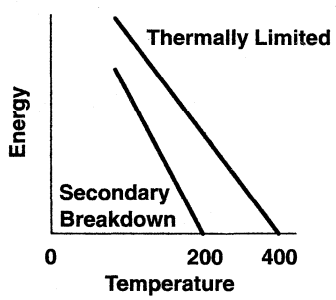
Where:

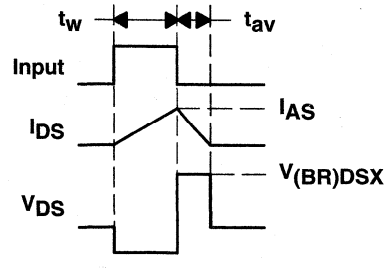
A = Area of power generation silicon
p = density of silicon
k = thermal conductivity of silicon
c = thermal capacity of silicon
T_m = $(2^{0.5})/3\ P_o\ k(t_{av})^{0.5}$
$T_{j(pk)}$ = Peak junction temperature at point of destruction = $T_m + T_c$

Table 2. Unclamped Inductive Switching Test Data†

DEVICE TYPE	I_{AS} (A)	t_{av} (ms)	V_{DSX} (V)	V_{DD} (V)	L_{eff} (mH)	L (mH)	E (mJ)	P_o (W)	K	T_m (°C)	$T_{j(pk)}$ (°C)
DMOS TPIC6259	2.1	0.8	50	15.1	19	13.2	42.2	105.5	269.0	378	403
	1.7	1.4	50	15.1	42	29.4	58.1	83.0	269.0	394	419
Bipolar Device A	1.3	1.5	37	9.0	41	30.7	35.4	48.8	139.5	122	147
	0.9	2.6	37	12.8	101	66.3	43.9	34.4	139.5	114	139
	0.8	5.0	37	19.0	247	120.0	69.4	27.8	139.5	129	154
Bipolar Device B	0.8	1.3	50	11.6	80	61.4	25.6	40.0	139.5	94	119
	0.7	1.8	50	9.5	125	101.0	30.6	35.0	139.5	96	121
	0.5	3.4	50	15.0	335	335.0	41.9	25.0	139.5	95	120

† Maximum energy capability prior to device destruction, T_j = starting junction temperature = 25°C.





Voltage and Current Waveforms

$$\text{Energy} = \int_0^{t_{av}} I_{DS}\ V_{DS}\ dt$$

In addition to peak switching current and load inductance, the energy capability of a power device varies with temperature. As the junction temperature of the device increases, energy capability decreases. This temperature-energy relationship has been exploited to further understand the avalanche energy capabilities of the Power+ Logic device.

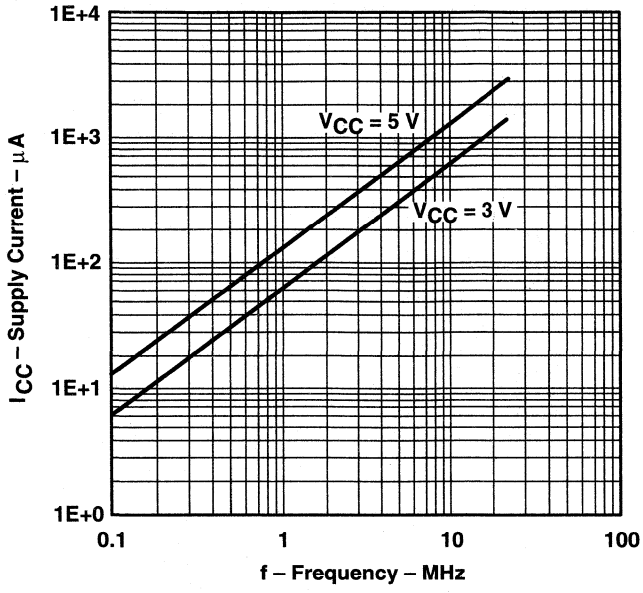
Unclamped inductive switching tests have been performed on the Power+ Logic device in which the junction temperature of the DMOS output was gradually raised by forcing the device to dissipate increasingly large amounts of energy. The virtual junction temperature of the device immediately prior to destruction was calculated. For the purposes of these tests, the 150°C maximum junction temperature specification of the Power+ Logic device was violated; these tests do not reflect recommended operation of the Power+ Logic device.

Assuming the mechanical limitations of the package are disregarded, the maximum avalanche energy capability of a power device operating in the forward-bias mode is limited by the thermal capabilities of the silicon. However, the actual avalanche energy dissipated by a given power structure may be prematurely limited by a secondary breakdown mechanism. In the case of the Power+ Logic outputs, the absence of forward secondary breakdown can be shown. The calculated virtual junction temperature of the Power+ Logic output structure at the point of device destruction is greater than 400°C. Since silicon is thermally limited at approximately 400°C, silicon thermal limitations are the probable cause of device destruction.

For comparison, similar tests have been performed on bipolar devices A and B. Bipolar device B (50-V clamp) had a calculated maximum virtual temperature of approximately 120°C immediately prior to destruction, clearly illustrating a secondary breakdown limitation. Bipolar device A (37-V clamp) had improved characteristics, but still clearly experienced secondary breakdown limitations with destruction temperatures ranging from approximately 140°C to 150°C.

The Power+ Logic devices integrate performance power output structures with high density sub-micron CMOS logic. Figure 13 shows I_{CC} versus SRCK frequency for the TPIC6595 with the outputs static and an alternating bit pattern on the SER IN pin. This example demonstrates the high logic frequency capability of the Power+ Logic devices, as well as the low V_{CC} power consumption. High logic speed capability allows the information to be transferred from the micro-processor interface very quickly even though the switch and load operation occur at a much slower repetition rate. This is especially important when cascading several devices for a large number of outputs all controlled by a single serial interface.

The power described in this graph is the term P_{quies} and is used in calculating the total average power dissipated in a device.



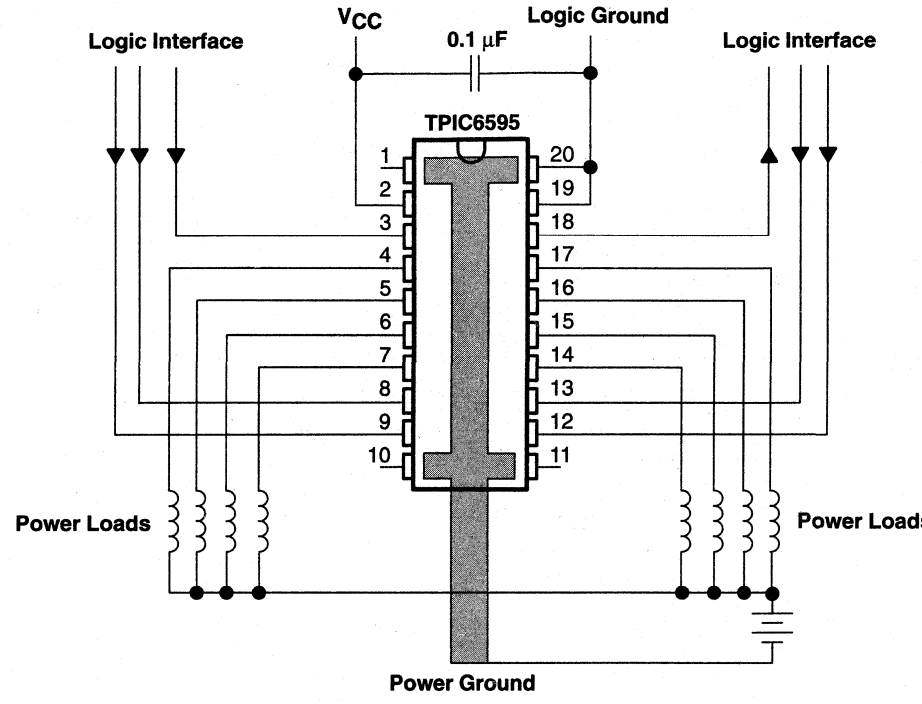
1-μm CMOS Logic Exhibits Extremely Low Power Supply Current Consumption

Figure 13. Power+ Logic Features Low Quiescent Current

When using the TPIC6595 or any of the Power+ Logic devices, there are several printed-circuit board (PCB) layout considerations that should be kept in mind. High frequency layout rules should be used when designing power switching systems. This is because mutual inductance (i.e. capacitance between the drive circuit and load circuit) can cause coupling of erroneous signals resulting in false operation. The following precautions are offered:

- Use of a power ground bus on the PCB to eliminate crosstalk between the power loads and input logic.
- Addition of a 0.1-μF bypass capacitor between V_{CC} and the logic ground line, placed close to the device to dampen any stray signals experienced by the drive circuit.
- Separate power and logic ground circuits.

Figure 14 shows the implementation on these board layout considerations using the TPIC6595.



- Creation of a power ground bus on the board which eliminates crosstalk between logic and power loads
- Bypass capacitor of 0.1 µF placed close to the device
- Separate logic ground circuit

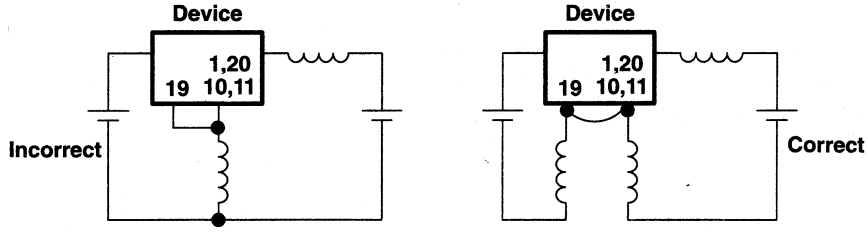


Figure 14. Layout Precautions for the TPIC6595

Bidirectional Motor Drive Application

DC motors play an important role in a wide variety of electronic systems. Efficient control of motor speed and torque is an important issue for many system designers.

Figure 15 shows a bidirectional dc motor being driven from a 14.5-V supply by two dual DMOS switch devices arranged in a full H-bridge configuration. This circuit uses 20-kHz PWM input signals that are 180 degrees out of phase. In most systems, these signals are supplied by a micro-controller. A 50% duty cycle on both input signals produces a net zero voltage across the motor, creating a stall condition. Control of the motor's speed and direction of rotation is achieved by varying the duty cycle of one of the input signals while keeping the other fixed at 50% duty cycle. This variation between the input signals results in a net dc voltage across the motor providing the drive current needed to meet the torque requirements of the motor.

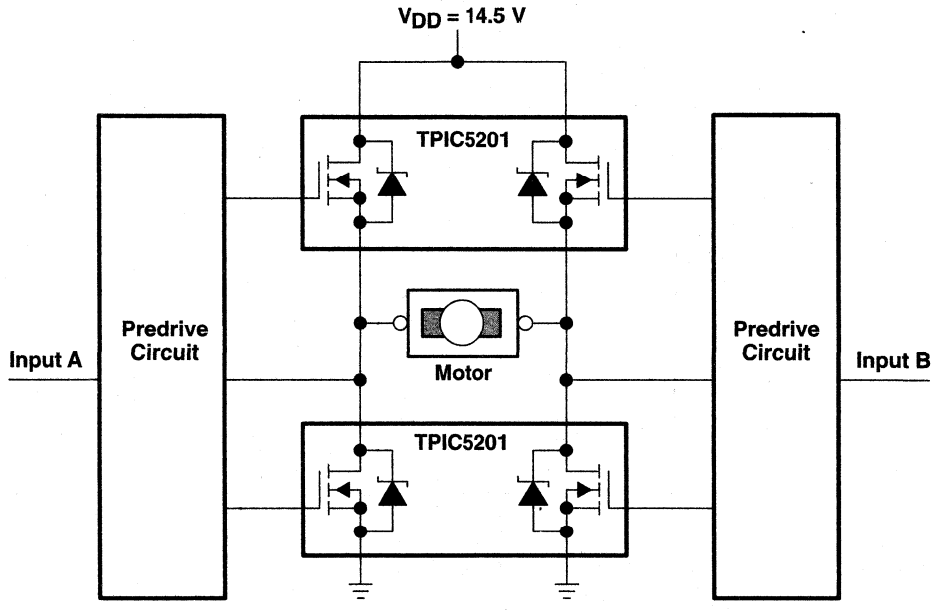
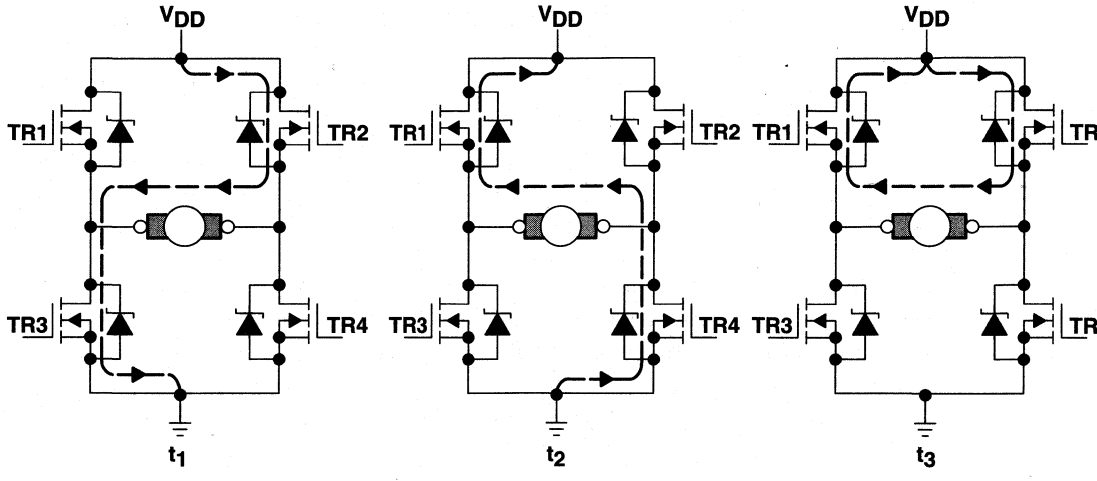


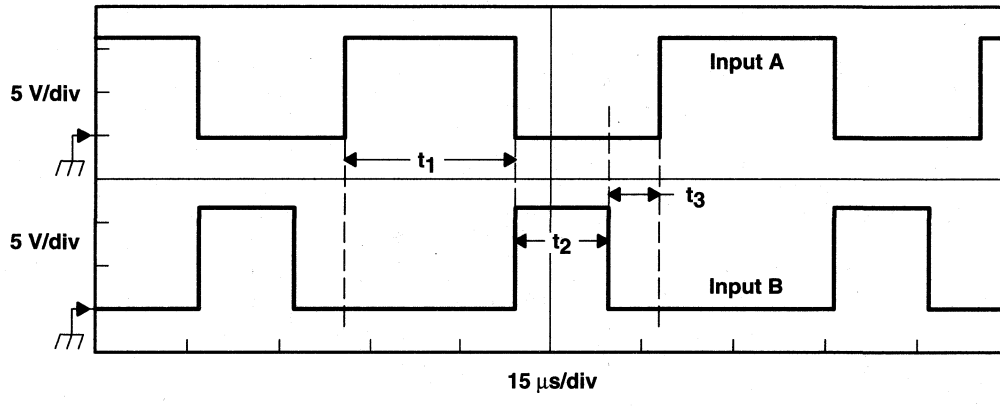
Figure 15. Bidirectional DC Motor Application

Motor Operation

Motor operation is shown in Figure 16. In this example, the motor is driven in the forward direction. The motor speed is controlled by varying the duty cycle of input signal B. While input signal A is high and input signal B is low, there is a net negative voltage across the terminals of the motor and current through the motor ramps up. Once input A goes low, a net positive voltage appears across the motor terminals and the motor current ramps down. When both input signals are low, there is no net voltage across the motor terminals and the H-bridge recirculates a relatively constant current through its upper stages. To drive the motor in the reverse direction, input signal B is held to a 50% duty cycle while the duty cycle of input A is varied.



(a) MOTOR DRIVE CURRENT PATHS



(b) INPUT VOLTAGE WAVEFORMS

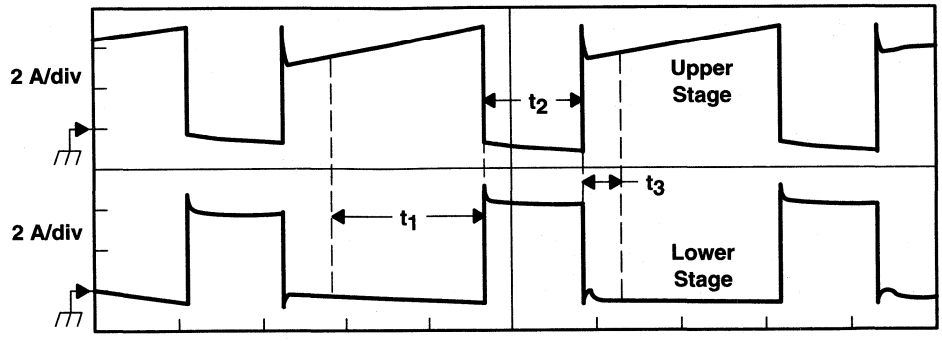
Figure 16. DC Motor Operation

Figure 17(a) shows the current through the transistors on one side of the H-bridge during time periods t_1, t_2, and t_3. Operation of the other side of the H-Bridge is similar. Figure 17(b) shows the motor voltage and currents during the same time periods.

In this example, the pulse width of the input signal is approximately 25 µs at a 50% duty cycle. It is important to note that when switching both the upper and lower transistors on the same side of the H-bridge, a brief delay must occur to allow the conducting transistor to turn off before the non-conducting transistor is allowed to turn on. Without this delay, excessive cross-conduction current may result. Cross conduction is a condition in which the upper and lower FETs on one side of the H-bridge are on simultaneously, providing a low impedance path between the source voltage and ground. While small cross-conductance currents can actually be used to enhance system performance, uncontrolled cross conduction can result in excessive heat dissipation and degradation of the device.

System Power Considerations

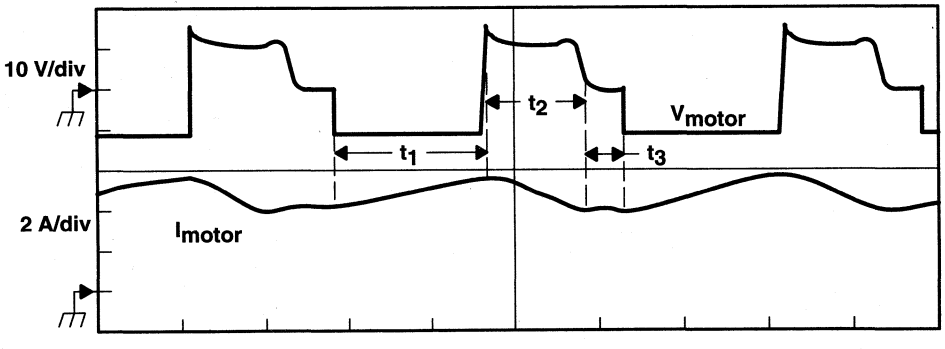
The motor drive current shown in Figure 17(b) has a peak value of slightly less than 6 A with a minimum value of 4 A. Energy calculations must be based on the condition when one of the input signals is at the minimum duty cycle. The motor current during time t_3 is due to back EMF and must be included in power dissipation calculations.



15 μs/div

Current through the upper and lower stages of the H-Bridge, transistors TR2 and TR4

(a) H-BRIDGE CURRENT WAVEFORMS



15 μs/div

Differential motor voltage and current waveforms

(b) MOTOR WAVEFORMS

Figure 17. DC Motor and H-Bridge Currents

Choosing an Output Switch

The device required for this application must be capable of conducting at least 5 A continuously, and as shown in the previous diagrams, must be configured as an H-bridge.

The device chosen for this application is a TPIC5201 Power+ Array as shown in Figure 18. This device contains two totally independent high performance DMOS transistors in a single power package. The independent transistors allow for an H-bridge configuration. The low $r_{DS(on)}$ minimizes the power dissipation.

- **Two independent N-channel enhancement-mode DMOS transistors**
- **7.5-A Continuous current per channel**
- **Low $r_{DS(on)}$ . . . 90 mΩ typ**
- **60-V Maximum output voltage**
- **15-A Pulsed current per channel**
- **High avalanche energy rating . . . 120 mJ**

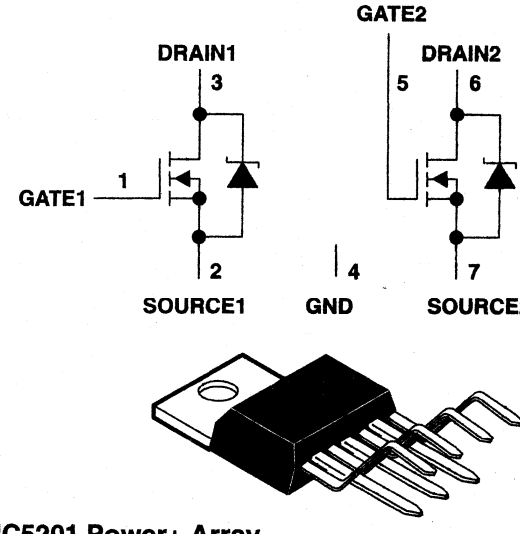


Figure 18. TPIC5201 Power+ Array

Predrive Circuit

In this application, two symmetrical predrive circuits are used to drive the gates of the upper and lower FETs. The predrive circuit schematic is shown in Figure 19. Drive to the upper transistors is achieved through the use of an HCPL2531 optocoupler followed by an emitter-follower stage. The high speed optocoupler isolates and level shifts the upper stage FETs from the input while providing a reference to ground. The emitter-follower provides low impedance drive for fast charging of the intrinsic gate-source capacitor to enhance switching times.

A 0.1-μF bootstrap capacitor is used to allow the gates of the upper FETs to rise above the supply voltage rail. The bootstrap must be at least 10 times larger than the parasitic gate capacitance of the TPIC5201, typically 18 nF. Inclusion of the emitter-follower and the bootstrap capacitors allow the upper transistors to be turned on hard when the input signal transitions high.

The low gate capacitance of the TPIC5201 allows for improved efficiency in the motor control circuit. In a power switching application, as the switching frequency increases, switching losses due to the continuous charge and discharge of the gate capacitor become the dominating component of the power loss. By minimizing typical gate capacitance, the TPIC5201 reduces switching losses, which results in reduced system power consumption and improved system efficiency.

The predrive circuit includes a delay RC network to ensure that cross conduction does not occur. The time constant of this RC network must be greater than the 0.8-μs propagation delay time associated with the switching times of the HCPL2531 optocoupler. By delaying the turn-on drive to the gates of the power MOSFETs, cross-conduction currents are eliminated.

External under-voltage-lockout protection is added to the circuit to keep the lower-stage FETs turned off until a predefined threshold voltage is obtained. This threshold voltage is determined by the threshold of the zener diode coupled with the threshold of the TP4050 buffer. In this circuit, the lower FETs remain off between 2 V and 6.2 V.

Advantages Over Discrete Transistors

Since the two power MOSFETs of each TPIC5201 are fabricated monolithically, the FETs within each device are inherently well matched. As a result, there is little variation in the switching times and transconductance of the upper-stage transistors. This device matching aids in system design by significantly reducing the need for feedback circuitry to compensate for potential switching time mismatches. As a result, the necessary predrive circuitry is greatly simplified.

Each power transistor in the TPIC5201 features a low on-state resistance of 90 mΩ. By minimizing on-state resistance, the power consumption of the H-bridge is reduced increasing the power available to the motor. Motor control systems built with low on-state resistance power switches allow more efficient motor performance.

The energy capabilities of the TPIC5201 have been characterized over its entire range of operation. The specifications for the TPIC5201 include peak avalanche current versus avalanche time-rating curves. Unlike the single-point energy specifications typical of discrete MOSFETs, designers using the TPIC5201 can accurately monitor compliance with active safe-operating-area design constraints.

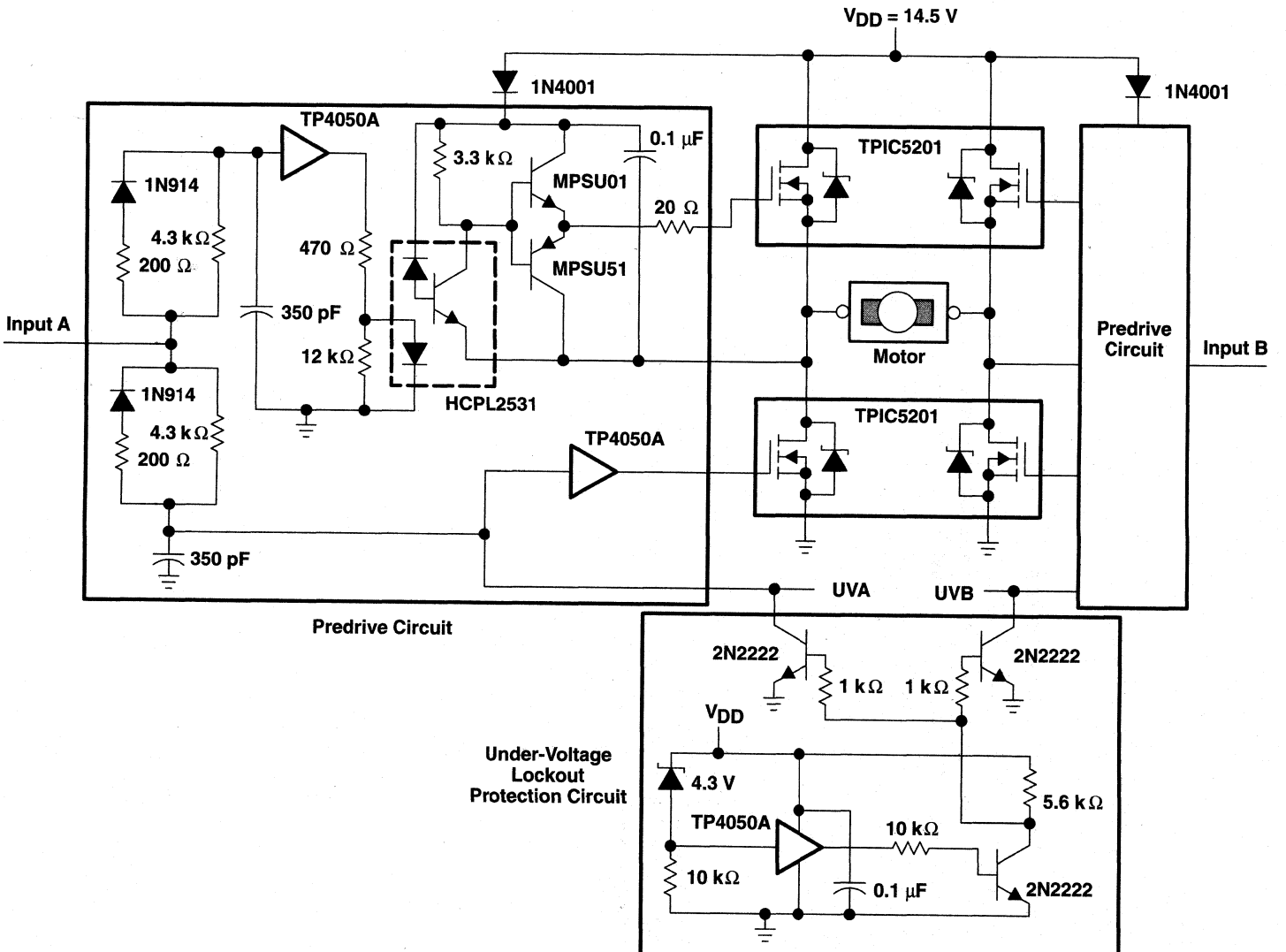


Figure 19. Predrive Circuit Detail

Solenoid Application

Solenoids are used to provide linear motion. Solenoid applications include electric locks on automobiles, mechanism actuators in tape recorders, and air-control valves.

Figure 20 shows a solenoid with a high-side driver. The high-side drive places the control switch between V_{CC} and the load. Selection of a switch device for this application must include an energy evaluation and a device that can operate as a high-side switch. The solenoid load is inductive like the stepper motor; however, instead of having cross-coupled signals, the solenoid has a dynamically changing impedance.

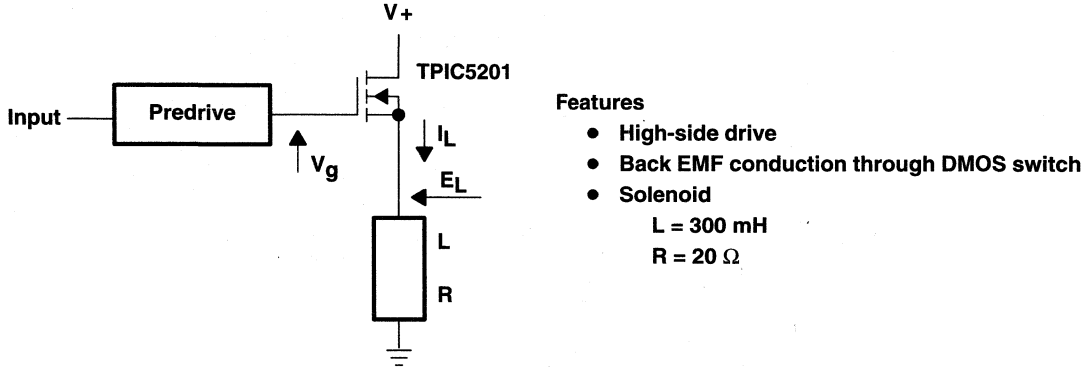


Figure 20. Solenoid High-Side Application

When the current reaches a level sufficient to cause the solenoid to operate, the armature begins to move. When the armature moves relative to the coil, the coil inductance changes. The amount of change is a function of the solenoid design. Conventional relays also exhibit this change in inductance since they are solenoids that operate switches.

Energy and power considerations are similar to the stepper motor. The interface circuit must drive an inductive load with a peak current. The solenoid winding inductance and resistance must be considered when evaluating the avalanche energy. Just as with any inductive load, the total avalanche energy must be considered as well as the peak avalanche current.

Choosing an Interface Device

The voltage and current waveforms for the solenoid are shown in Figure 21. This particular solenoid is chosen because of the drastic inductance change during operation. The inductance change causes the discontinuity seen in the inductor current during t_{on}.

The output from the predrive circuit, V_g, is at –5 V during t_{off}. The circuit as shown relies on the DMOS transistor to provide the conduction path for the back EMF current from the inductor when the drive is turned off (t_{off}), as described in the stepper motor application. When the switch is turned off, the solenoid voltage goes negative. When the solenoid voltage reaches approximately –7.5 V (V_g – 2.5 V), the DMOS transistor is turned on, effectively clamping the inductor voltage. If V_g = 0 V at t_{off}, then the solenoid voltage is clamped at –2.5 V and the time required for the solenoid current to reach zero is longer.

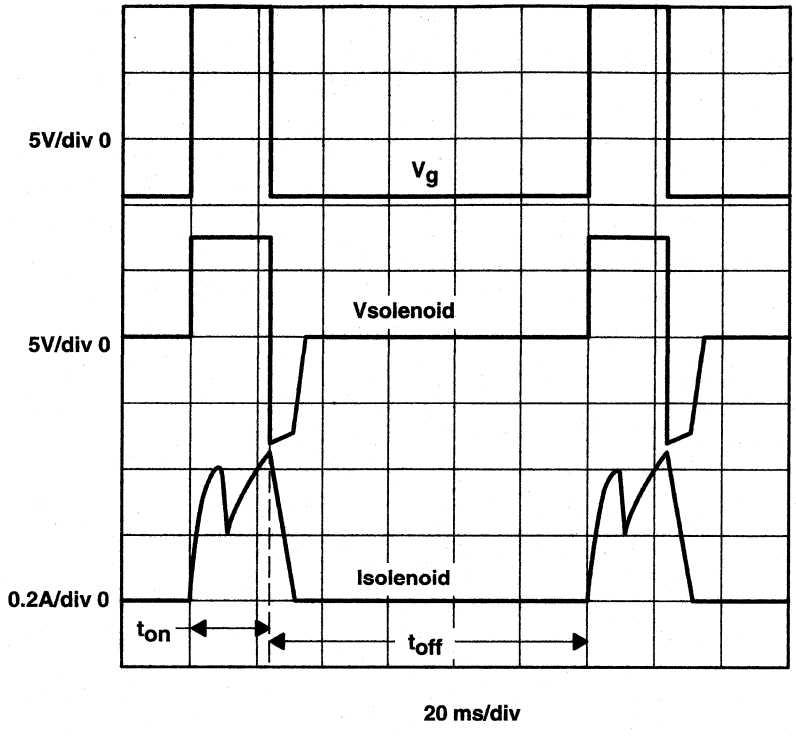


Figure 21. Solenoid Voltage and Current

Power and Energy Calculation

Switching:

$E_T = 113$ mJ

$P_{off} = 940$ mW

$P_{on} = 2$ mW

$P_T = 942$ mW

$$E_T = \frac{3L\ I_P^{\,2}\ V_{CL}}{6\left(V_{CL}-V_{SS}\right) + 4\ R_L\ I_P}$$

$$P_{off} = E_T\ f$$

$$P_{on} = \frac{1}{3}\left(I_P^{\,2}\right)\ r_{DS(on)}\ d$$

$$P_T = P_{off} + P_{on} + P_{quies}$$

Continuous:

$P_{on} = 32.4$ mW

$$P_{on} = I_P^{\,2}\ r_{DS(on)}$$

Where:

$t_{on} = 25$ ms

$t_{off} = 95$ ms

$V_{SS} = 12$ V

$V_{CL} = 8$ V

$L = 300$ mH

$I_P = 0.5$ A

$r_{DS(on)} = 90$ mΩ

$P_{quies} = 0$

Using the current waveforms from Figure 21, the energy dissipated in the switch can be calculated. The TPIC5201 Power+ Array has been chosen as the switch for this application.

Using the calculations presented in the Output System Design section:

$$E_T = \frac{3\left(L \cdot I_P^{\,2} \cdot V_{CL}\right)}{6\left(V_{CL}-V_{SS}\right) + 4\left(R \cdot I_P\right)} = 113\ \text{mJ}$$

$$P_{off} = E_T \cdot f = 0.94\ \text{W}$$

$$P_{on} = \frac{1}{3} \cdot I_P^{\,2} \cdot r_{DS(on)} \cdot d = 7.5\ \text{mW}$$

$$P_{T(av)} = P_{off} + P_{on} + P_{quies} = 0.94\ \text{W}$$

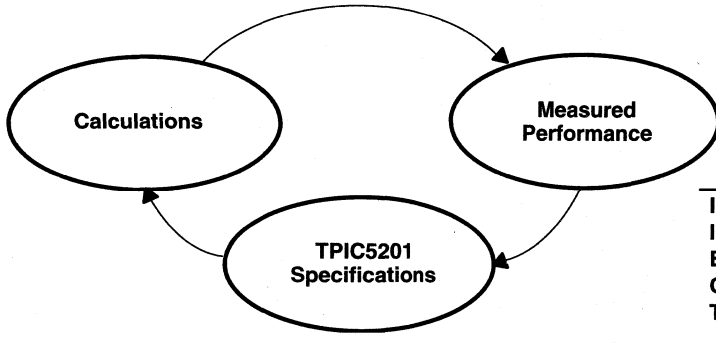
Assuming that the solenoid could be turned on for an extended period of time, the power dissipated in the switch would be:

$$P_T = I^2 \cdot r_{DS(on)}$$

$$I = \frac{V_{CC}}{R} = 0.6 \text{ A}$$

$$P_T = 0.6^2 \cdot 0.09 = 32.4 \text{ mW}$$

Closing the design loop and comparing calculations, results and specifications verify the design and indicate changes when necessary, as shown in Figure 22.



	TPIC5201	Solenoid Application
I_P	15 A	0.5 A
I_{CONT}	7.5 A	0.6 A
E_{AS}	120 mJ	113 mJ
Cont Power	2 W	0.94 W
T_A = 25°C		

Figure 22. Closing the Loop

The results of this comparison are not what might be expected. The avalanche energy is high (113 mJ), while the power dissipation is quite low (0.9 W). This indicates that no heat sinking is required and that a device with a lower power and current rating could be used in this application. It also illustrates the importance of doing thorough energy calculations. In this case, a quick look at current handling alone might suggest the device chosen is overkill; but when avalanche energy is considered, it can be seen that the TPIC5201 is a good match for the application. A similar device rated at a lower peak current value would probably be unable to handle the avalanche energy, possibly resulting in repeated mysterious device failures.

Power+ Product Summary

Power+ products are available in many configurations. Tables 3 through 5 show the key comparisons of Power+ Arrays, Power+ Logic, and Power+ Control, respectively. These tables can serve as a starting point in choosing the product that functionally fits an application.

Table 3. Power+ Array Key Comparisons

Devices V_{DSmax}: 60 V I_{cont}: 0.5 A – 7.5 A $r_{DS(on)}$: 0.09 Ω – 0.6 Ω	TPIC: 2202 2301 2701 5201	TPIC: 2302 3302 5302 5404 5601	TPIC: 2322L 3322L 5322L 5424L 5621L	TPIC: 1301 5203 5303 5401 5403	TPIC: 1321L 5223L 5323L 5421L 5423L
5 V Logic-level interface			X		X
4000 V ESD protection				X	X
Configured for motor drive		X	X	X	X
Solenoids, motors, relays	X				
Surface-mount packaging		X	X	X	X

Table 4. Power+ Logic Key Comparisons

Devices	TPIC6259 TPIC6273 TPIC6595	TPIC62A259 TPIC62A595	TPIC6B259 TPIC6B273 TPIC6B595	TPIC6E175¶ TPIC6E261¶ TPIC6E585¶
Typical $r_{DS(on)}$ (Ω)	1.3	1	5	1
Output clamp voltage (V)	45	50	50	40
Avalanche energy (mJ)	75	75	30	100
Transistor outputs	8	8	8	4
Continuous current (mA)	250	350	150	§
Pulsed current per output (A)	1.5	1.1†	0.5‡	1
Quiescent current, typical (μA)	15	500	20	1600
Packaging	DIP/SO	DIP/SO	DIP/SO	DIP

† Current-limiting capability and short-circuit protection
‡ Current-limiting capability
§ User-programmable PWM from 300 mA–1 A
¶ Preliminary data only

Table 5. Power+ Control Key Comparisons

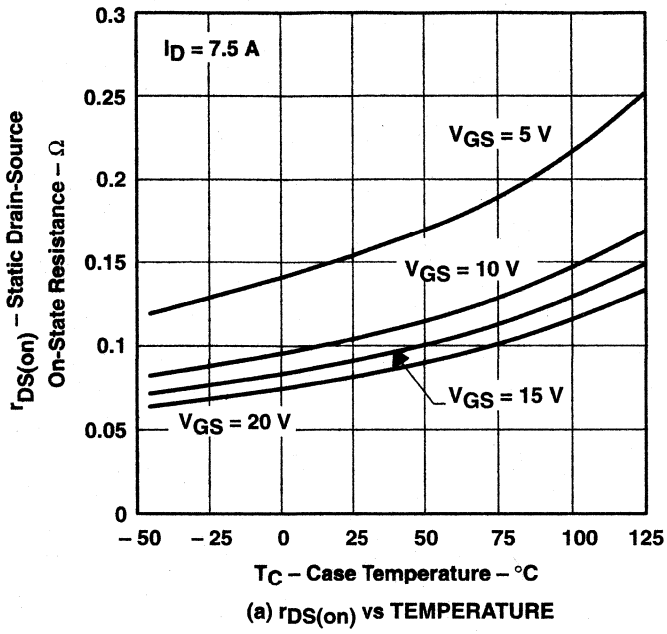
Devices	TPIC2101	TPIC2603†
Number of channel	1	6
Internet FET	No	Yes
Diagnostics	No	Yes
Fault protection	Yes	Yes
Battery supply voltage (V)	8 – 16	5.5 – 25
Frequency, typical (kHz)	20	4000
Quiescent current, max (μA)	200	50
Packaging	DIP/SO	DIP/SO

† Preliminary data only

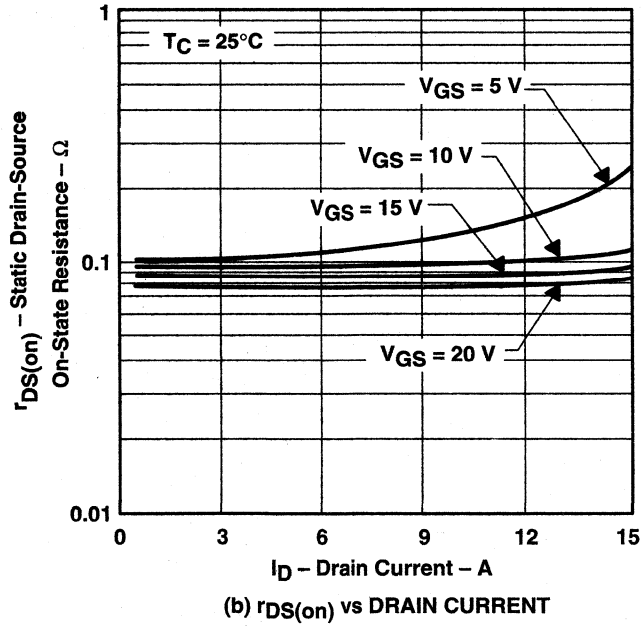
Selecting a Power+ product includes choosing a product that meets the application performance requirements. These tables compare some of the key specifications from both product families. These are the parameters most often used for an initial product selection.

The applications and design information presented in the previous sections have relied on some assumptions about device parameters in order to simplify the analysis while still arriving at a meaningful evaluation.

Figure 23 shows the excellent on-state resistance stability for the Power+ Array DMOS transistors. This also shows the type of device information available in the data sheets; complete device characterization is provided in the data sheets for Texas Instruments Power+ products.



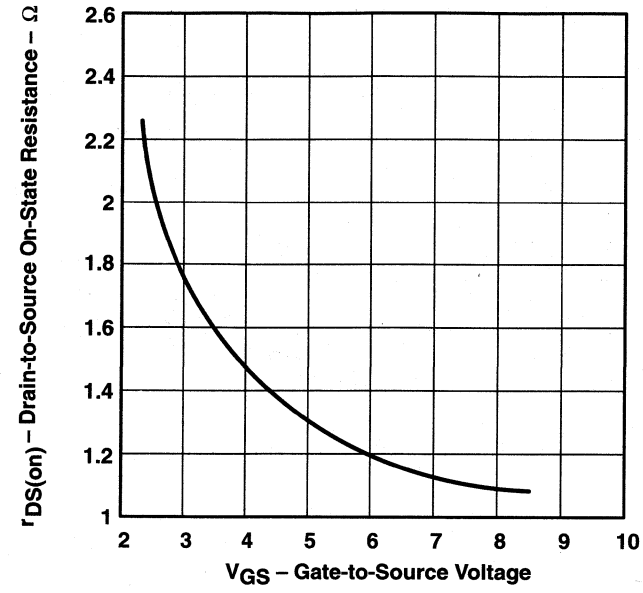
(a) $r_{DS(on)}$ vs TEMPERATURE



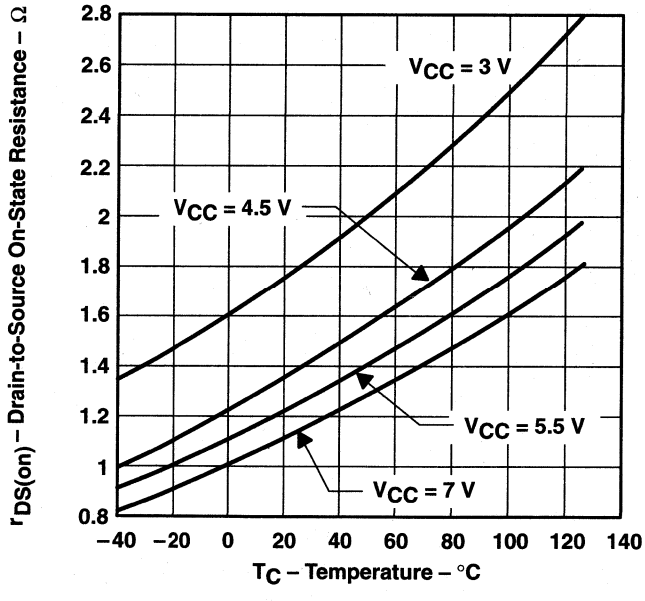
(b) $r_{DS(on)}$ vs DRAIN CURRENT

Figure 23. Power+ Arrays On-Resistance Characteristics

Figure 24 shows device on-state resistance performance for the Power+ Logic family of devices. While the $r_{DS(on)}$ is higher than that of the Power+ Arrays, the power handling for these outputs is still substantial as shown in Table 4.



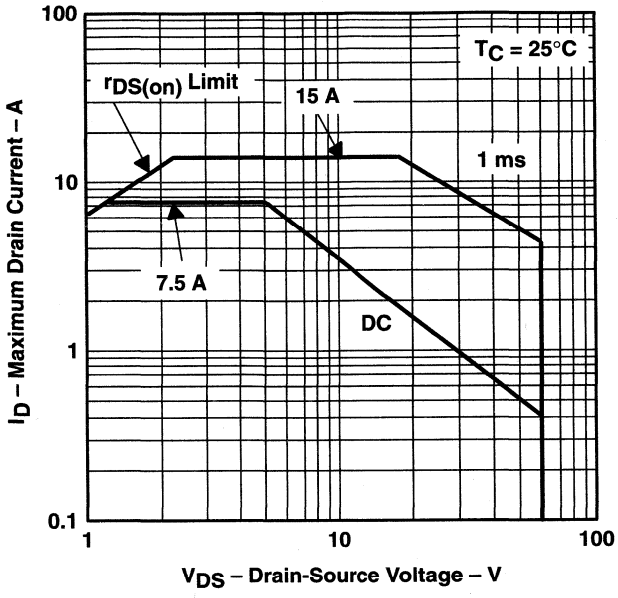
(a) $r_{DS(on)}$ vs GATE-TO-SOURCE VOLTAGE



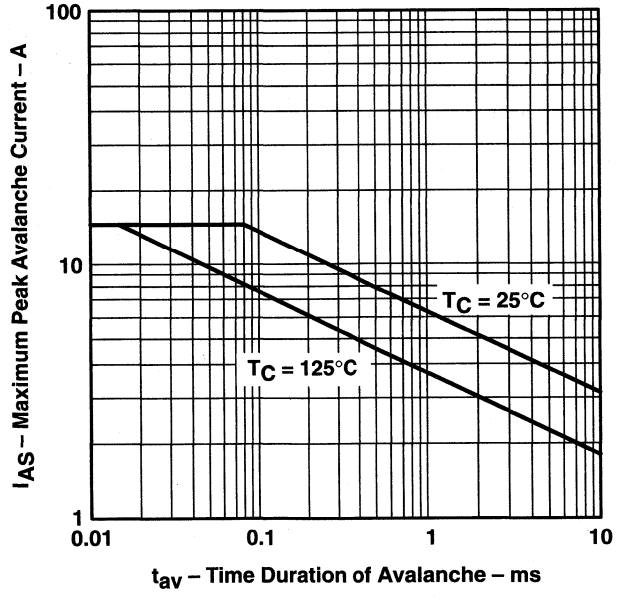
(b) $r_{DS(on)}$ vs TEMPERATURE

Figure 24. Power+ Logic Output Characteristics

The safe-operating-area (SOA) characteristics are presented in graphical form to include peak currents and absolute times. Avalanche energy capability depends on many factors and cannot be adequately described by a single number. Figure 25 indicates the relationship between safe avalanche operating conditions and time, temperature, and current for Power+ Arrays. Similar information is included in the data sheets for Power+ Logic products.



(a) MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE



(b) MAXIMUM AVALANCHE CURRENT vs TIME DURATION

Figure 25. Power+ Arrays SOA Characteristics

TPIC6595 Power+ Logic™ Eight-Bit Shift Register With Low-Side Power DMOS Switches

TEXAS INSTRUMENTS

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Introduction

The TPIC6595 is a monolithic Power+ Logic™ device that contains eight 1.5-A peak/45-V low-side DMOS power switches packaged in a 20-pin dual-in-line plastic package. The logic functions of the TPIC6595 consist of the logic functions existing in the high-speed CMOS (HCMOS) SN74HC595 catalog parts except the outputs are inverted relative to the HCMOS version. The eight DMOS switches are controlled from a single input, SER IN (serial input), and by an 8-bit serial word. Data is transferred through an 8-bit shift register on the rising edge of SRCK. SER OUT is provided at the last bit of the shift register to allow cascading in applications requiring more than eight DMOS switches.

Each of the eight DMOS switches are equipped with an internal 45-V drain-to-gate zener clamp that greatly enhances their capability to switch unclamped inductive loads. Since the zener clamp causes the DMOS switch to be forward biased instead of being avalanched during inductive-load turn off, a power switch avalanche energy rating of 75 mJ maximum is achieved.

This device provides a cost-effective single-chip solution for direct control of motors, relays, solenoids, and other high-energy, high-electrical stress loads including lamps. Since the device implements a direct control link between the microcontroller and the system electrical loads, use of multiple logic integrated circuits and discrete power devices are eliminated. The reduction of discrete devices not only reduces cost, but saves circuit space and improves system reliability by the reduction of active components.

Functional Description

The TPIC6595 is an 8-bit serial-in-to-parallel-out power driver having separate power and logic ground pins. A functional block diagram is shown in Figure 1. Data is transferred through an 8-bit shift register on rising edges on SRCK. The data in the shift register is latched to the outputs by the rising edge on RCK. All outputs are placed in a high-impedance mode with a high level on $\overline{G}$, but the data is not cleared from the storage register latches. $\overline{SRCLR}$ clears all data in the shift register only. SER OUT is provided at the last bit of the shift register to allow for cascading in applications requiring more than eight output bits.

The logic used is specified within the data sheet to operate from 4.5 V to 5.5 V, but it is capable of operation down to 3 V and up to an absolute maximum voltage of 7 V. The CMOS transistors used in the digital logic have small feature sizes and short channel lengths as well as tightly controlled, low threshold voltages. Due to these characteristics, the CMOS gains are high, and the parasitic capacitance is minimized. Because of this, the logic is able to function at greater than 25-MHz operation over the full V_{CC} range of 3 V to 7 V and over the temperature range of −40°C to 125°C. Another result of using primarily CMOS-type transistors in the design of the power logic is a low quiescent current (I_{CC}).

The predrive circuitry is a CMOS buffer stage that provides adequate sink/source drive to the gate of the output power DMOS. A series resistor has been added between the buffer stage and the gate of the DMOS in order to provide a more controlled gate-drain capacitor charging current than could be achieved with a CMOS buffer alone. The current-limit resistor serves two purposes: first, it limits power dissipation in the drain-to-gate zener clamp structure under inductive transient conditions, and second, it controls the voltage rise and fall of the DMOS gate. This reduces radio frequency interference (RFI) during output switching. The rise and fall times at the gate are controlled by the effective RC time constant, which consists of the series resistor and the C_{iss} of the DMOS.

The DMOS outputs are designed to have a typical static drain-source on-state resistance of 1.3 Ω with a continuous output current of 250 mA at 25°C and V_{CC} of 5 V. The DMOS transistors are designed to have

a low threshold voltage. The low threshold voltage along with the high gain of the devices allow the gates to be driven without the aid of any additional supply voltage above V_{CC}. Thus a charge pump or additional level shifting voltage supply is not necessary. The elimination of a charge-pump circuit reduces turn-on times, thereby minimizing power dissipation in the outputs during switching. The use of a charge pump also increases the susceptibility of generating RFI due to the need for an internal oscillator. An oscillator provides little interference due to its low power, but the DMOS may serve as a transconductance amplifier for the oscillator circuit, especially when switching small resistive loads.

Variation of the output characteristics is primarily a function of temperature and V_{CC}. With the CMOS predrive buffer used, the V_{GS} of the output DMOS varies directly with V_{CC}. A typical $r_{DS(on)}$ of 1.8 Ω at 25°C can be achieved with a V_{CC} of 3 V. This low static drain-source on-state resistance is directly attributable to the low DMOS threshold voltage in the process. Output $r_{DS(on)}$ primarily consists of the intrinsic DMOS resistance, the series resistance of the source and drain lead busing, bonding resistance, and lead frame resistance. All of these resistances have a positive temperature coefficient.

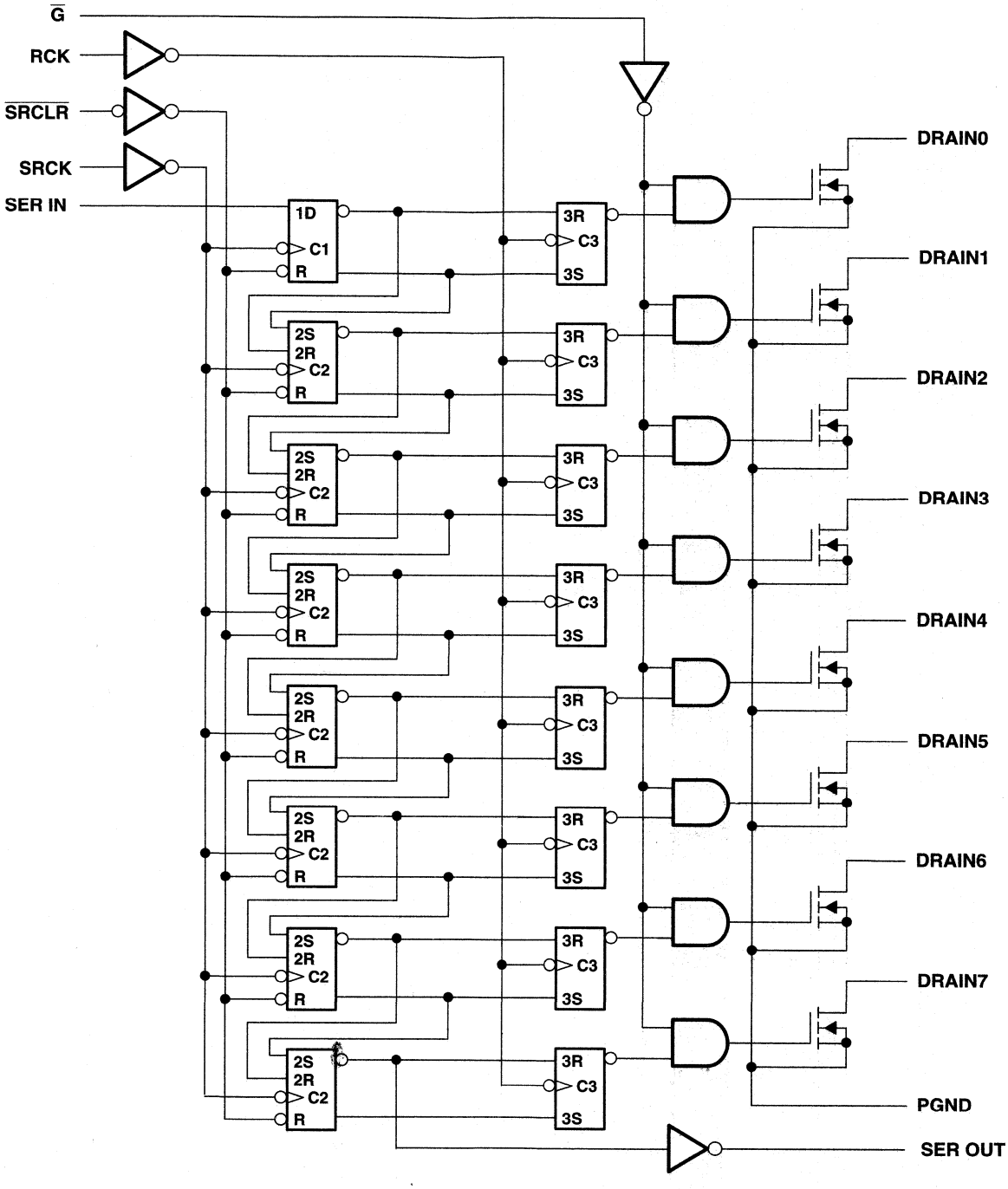


Figure 1. Functional Block Diagram

Application Design Considerations

Power and Thermal Considerations

Three important application considerations for a power device are the power, thermal, and inductive energy ratings with respect to the operational load demands. The following illustrate analytical approaches that ensure that the device is operating within these maximum ratings.

To calculate the current I_D for a single output with n outputs conducting equal current, use equation (1)

$$I_D = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times r_{DS(on)} \times 8}}\ K_n \qquad (1)$$

Where:

K_n = current coefficient for the current of a single output with n outputs simultaneously conducting equal current
$R_{\theta JA}$ = thermal resistance or junction-to-ambient, 90°C/W
$r_{DS(on)}$ = static drain-source on-state resistance at 150°C (worst case) 3.5 Ω
T_J = junction operating temperature, °C
T_A = operating ambient temperature, °C

Table 1. Values for the Current Coefficient K_n

Total Outputs On n	Current Coefficient K_n
1	2.67
2	1.95
3	1.61
4	1.40
5	1.26
6	1.50
7	1.07
8	1.00

The current coefficient values, K_n, shown in Table 1 are derived from the thermal model shown in Figure 2 and the TPIC6595 data sheet thermal resistance values.

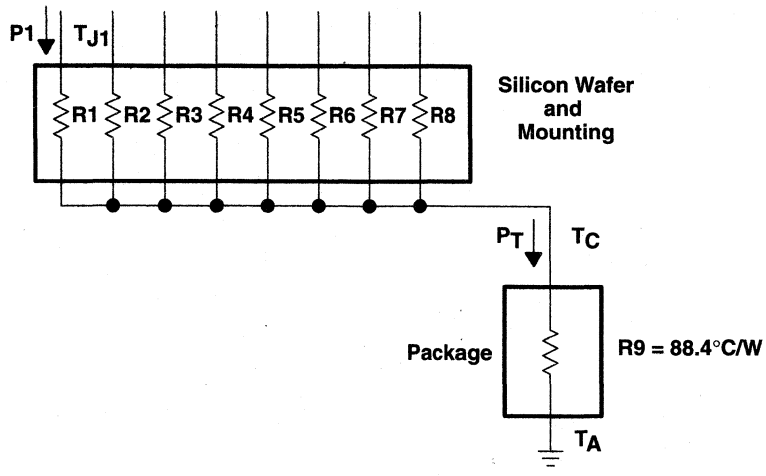


Figure 2. Thermal Model-Thermal Equilibrium, No Heat Sink

The following equations apply for the thermal model in Figure 2:

$R1 \parallel R2 \parallel R3 \parallel R4 \parallel R5 \parallel R6 \parallel R7 \parallel R8 + R9 = 90°C/W$
$R1 \parallel R2 \parallel R3 \parallel R4 \parallel R5 \parallel R6 \parallel R7 \parallel R8 = 1.6°C/W$
$R_{n,\ n = 1–8} = 12.8°C/W$
$R9 = 88.4°C/W$
$T_{J(n)}$ = junction temperature of an individual output with n outputs conducting equal current
$P1 = P2 = P3 = P4 = P5 = P6 = P7 = P8$

Therefore:

$$T_{J(n)} = P1R1 + nP1R9 + T_A$$

From the thermal model in Figure 2, P1 can be calculated using equation 1.

$$P_1 = \frac{T_{J(n)} - T_A}{R1 + nR9} = I_D^2\, r_{DS(on)} = I_D^2\, 3.5\ \Omega \qquad (2)$$

Switching Unclamped Inductive Loads and Turn-Off Power Dissipation, P_{OFF}

The data sheet shows an energy rating of 75 mJ. This energy rating is a specific point on the curve shown in Figure 5 on the data sheet, which is repeated here as Figure 3 for clarity.

The energy capability of the device in Figure 3 is not described in a traditional manner but as a graph of peak-switching current versus avalanche time for a starting junction temperature of 25°C.

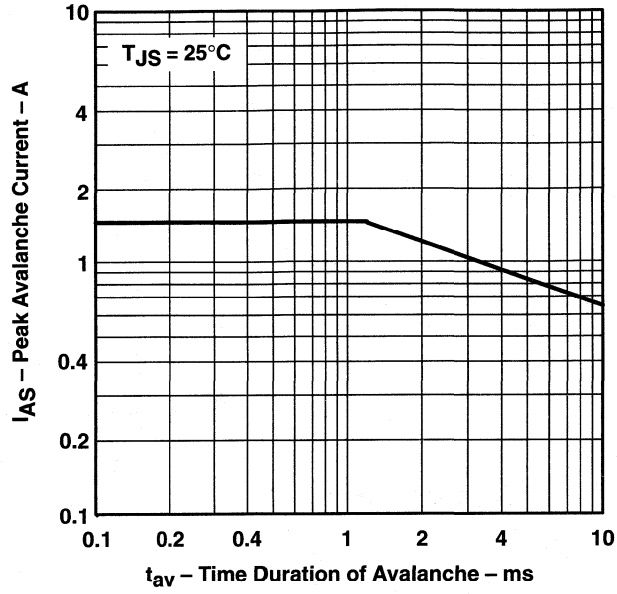


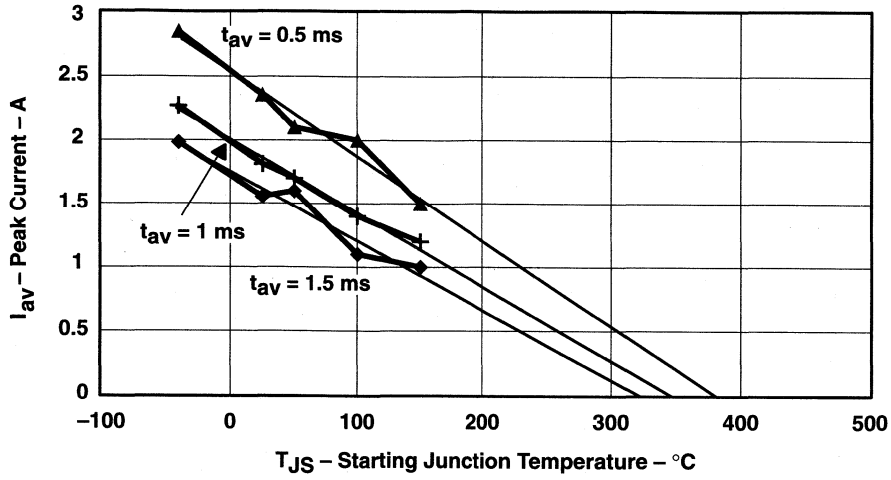
Figure 3. Peak Avalanche Current Versus Time Duration of Avalanche

It has been established that the energy limitations of these devices during inductive switching is due to the self heating of the silicon structure. Figure 4(a) shows the measurements of the peak-switching current versus starting junction temperature and idealized inductive switching waveforms. The power absorbed by the device during switching is proportional to the peak switched current, I_{av}. If the failure mechanism is thermal, the power capability of the device is related to the transient thermal impedance, starting temperature of the device, and maximum physical temperature that the silicon can withstand. It is well known[1] that for the typical resistivities used in the manufacture of these devices, the maximum temperature that silicon can operate at is in the range of 400°C. Therefore, if the peak switching temperature is plotted as a function of starting temperature, the relationship should be linear and intercept the temperature axis at 400°C. Study of Figure 4(a) shows that the 0.5-ms line has an intercept with the starting temperature is directly attributable to the zener diode that has been integrated between the drain and the gate of the device. The zener diode forces the whole DMOS structure to be active during voltage clamping and therefore gives the maximum possible energy absorption capability.

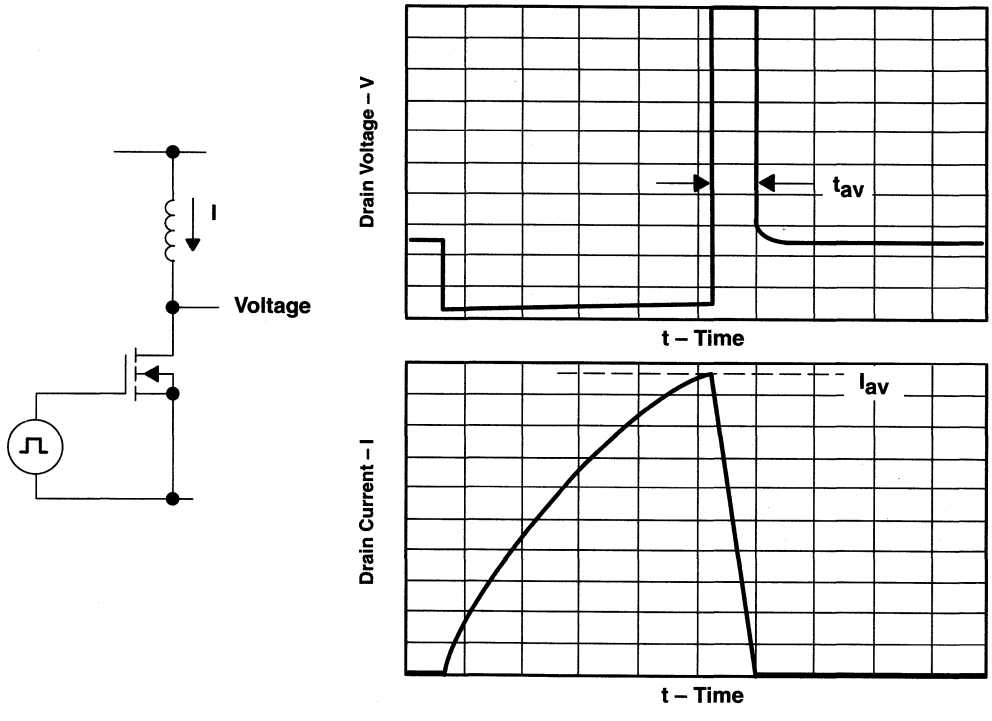
As a consequence of a thermally-limited failure mechanism, the concept of a single energy rating for the device does not fully characterize its capabilities, since the maximum energy capability is related to the time duration over which the energy is absorbed. Consequently, the inductive switching energy characterization of the TPIC6595 has been expanded to show peak switching current, I_{as}, versus avalanche time for the device, t_{av}.

The equation, $|V| = L\,di/dt$, can be used to relate this curve to a practical application circuit. Given a supply voltage, V_{DD}, and an internal clamp voltage of $V_{BR(DSX)}$ the avalanche time, t_{av}, is given by $(V_{(BR)DSX} - V_{DD})/L$, and the peak switching current I_{av} is simply the maximum current at switch off.

[1]Physics of Semiconductor Devices, Second Edition. Sze. John Wiley & Sons, pp. 19–26.



(a) PEAK SWITCHING CURRENT VERSUS JUNCTION TEMPERATURE



(b) IDEALIZED INDUCTIVE SWITCHING WAVEFORMS

Figure 4. Peak Switching Current Versus Starting Junction Temperature

If the maximum power dissipation of the device is not exceeded, it is possible to drive an inductive load by operating a number of the devices in parallel. This is due to the close matching of the gate-drain zener diodes.

Figure 5(a) shows four switches operating in parallel while driving a 105-mH/11.5-Ω load at 1 A. The power absorbed during switching is often greater than the power dissipated during the on period.

$$E_{off} = \frac{3L_H I_{DM}^2 BV_{(BR)DSX}}{\left[6(V_{(BR)DSX} - V_{DD}) + 4R_L I_{DM}\right]} \quad (3)$$

Where:

E_{off}	Total energy absorbed by TPIC6595 during turn-off transient	59.6 mJ
f	Switching frequency	25 Hz
L_H	Load inductance	105 mH
I_{DM}	Peak output load current	1 A
P_{off}	Turn-off power dissipation	1.26 W
R_L	Inductor resistance	11.5 Ω
$V_{(BR)DSX}$	Clamp voltage	45 V
V_{DD}	Load supply voltage	13 V

$$P_{off} = E_{off} f = 1.49 \text{ W} \quad (4)$$

In the above example, switching frequency of only 25 Hz can result in a power dissipation that is greater than the package rating device. If it is assumed that T_A = 25°C and T_J = 150°C, the maximum power dissipation, P_{max}, is given by

$$P_{max} = (T_{Jmax} - T_A)/R_{\theta JA}$$

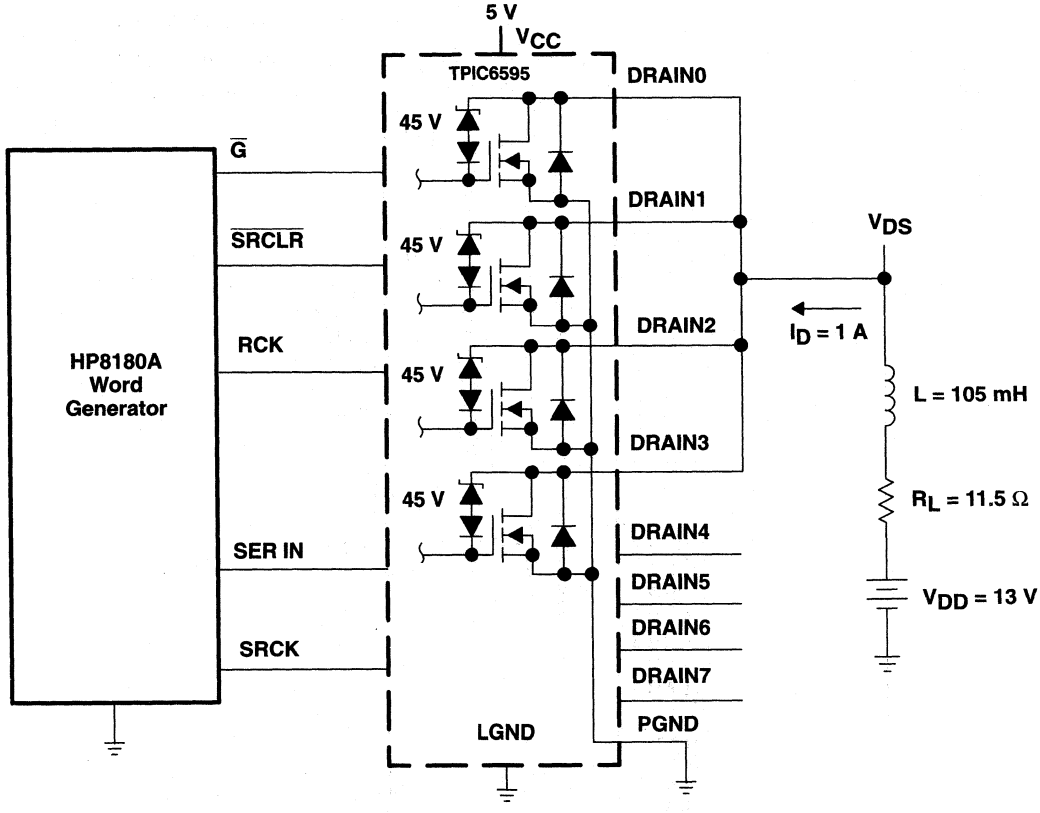
Where:

T_{Jmax} is the maximum junction temperature,
T_A is the ambient temperature, and
$R_{\theta JA}$ is the thermal resistance.

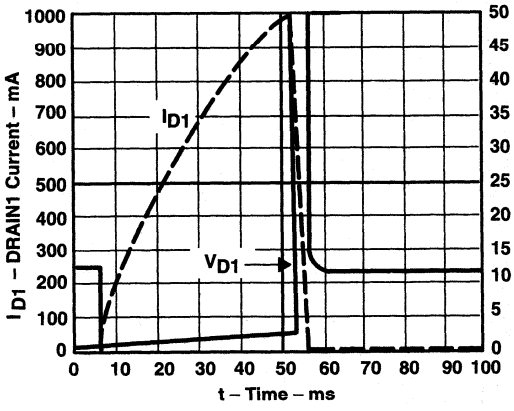
Thus,

P_{max} = (150−25)/90 = 1.39 W and at a switching speed of 25 Hz,
P_{off} = 59.6 mJ × 25 Hz = 1.49 W

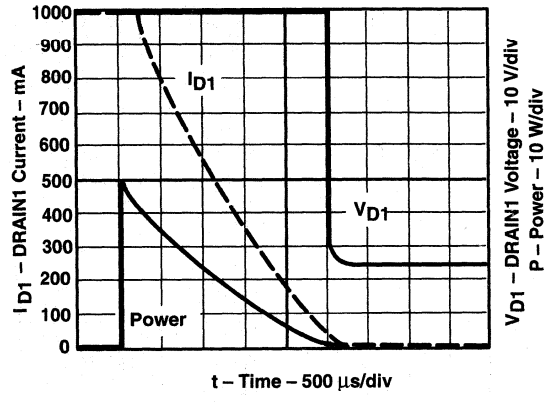
The above example demonstrates that the power dissipation associated with load turn off is often significantly greater than during the on period.



(a) POWER SWITCHES CONNECTED IN PARALLEL



(b) FULL CYCLE INDUCTIVE LOAD SWITCHING



(c) TURN-OFF INDUCTIVE LOAD SWITCHING

Figure 5. Power Switches Connected in Parallel

Parallel Operation of Output Switches for Extended Current Capability

If all eight output switches are not needed for an application and a continuous output load current greater than 0.25 A is required, the switches can be connected in parallel for extended current capability. The current-sharing capability of the switches is demonstrated in a circuit while operating at $T_A = 40°C$ (see Figure 6). The individual switch current, I_D, is determined by equation (5).

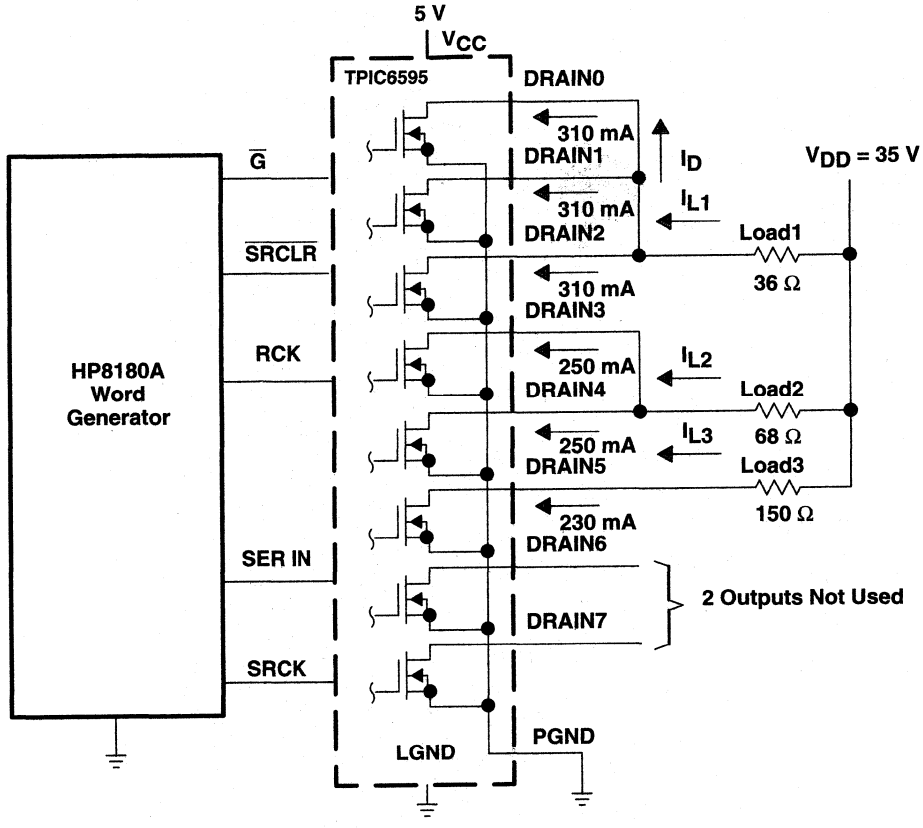


Figure 6. Parallel Operation of Output Switches for Extended Current Capability

$$I_D = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times r_{DS(on)} \times 8}}\ K_n \qquad (5)$$

K_n = current coefficient = 1.5, 6 outputs on

Where:

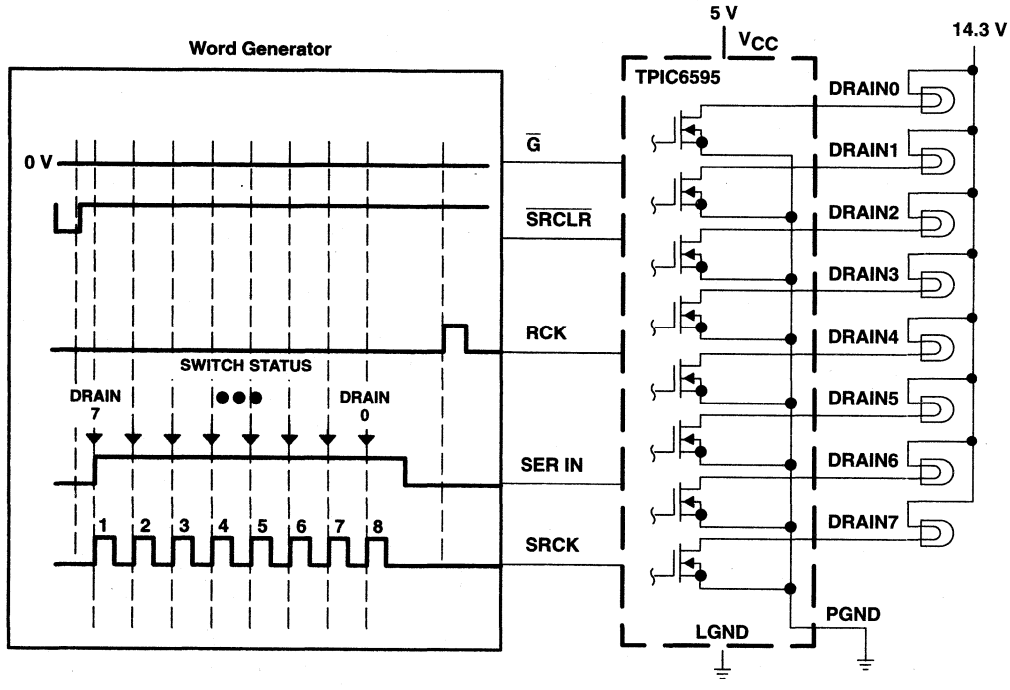
$$I_D = \sqrt{\frac{150°C - 40°C}{90°C \times 3.5\ \Omega \times 8}}\ K_n$$

I_D = 0.209 A × 1.5 = 0.313 A each switch
I_{L1} = 3 X I_D = 0.940 A max current for Load1
I_{L2} = 2 X I_D = 0.627 A max current for Load2
I_{L3} = 1 X I_D = 0.313 A max current for Load3

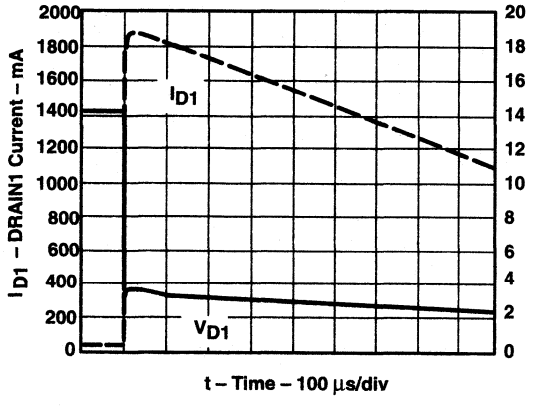
Application Design Examples

Direct Drive of Eight Lamps

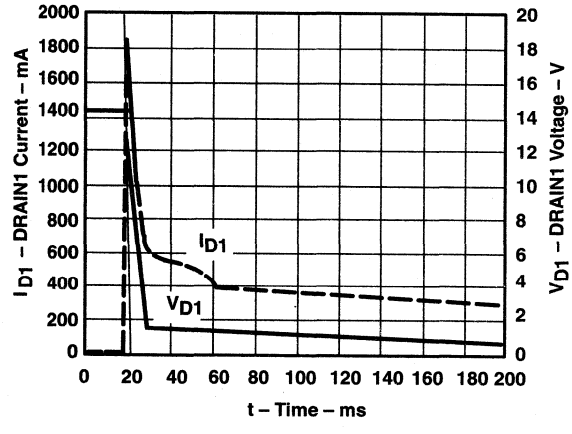
Figure 7 shows the TPIC6595 circuit simultaneously switching eight No. 194 automotive lamps from a 14.3-V source and various waveforms, which demonstrate the internal current limiting at approximately 1.8 A.



(a) LAMP SWITCHING TEST CIRCUIT



(b) INITIAL LAMP IN-RUSH CURRENT



(c) HOT FILAMENT LAMP CURRENT

Figure 7. Simultaneous Switching of Eight Lamps

The nature of an incandescent lamp is capacitive during turn on and represents an instantaneous short circuit. Previous measurements have indicated that the in-rush current (peak switching current) of the incandescent bulbs shown in Figure 7 is typically 2.6 A. As shown on the previous page, the TPIC6595 limits this current to approximately 1.8 A.

Direct Drive of Eight Relays

The worst-case power dissipation for continuous operation of all outputs is calculated as 0.438 W based on the device measurements.

$$\text{Maximum } r_{DS(on)} = 3.5\ \Omega\ (T_J = 150°C):$$
$$I_{rms} \approx 0.125\ \text{A (see Figure 9)}$$
$$P = I_{rms}^2 \times r_{DS(on)} \times 8\ \text{outputs on}$$
$$P = (0.125\ \text{A})^2 \times 3.5\ \Omega \times 8 = 0.438\ \text{W}$$

The power dissipation created by inductive energy is insignificant in this case because the resistance component of the load is large compared to the inductance. Based on $R_{\theta JA} = 90°C / W$ and $T_J = 150°C$, the maximum permissible ambient operating temperature (T_J) for driving the eight relays at continuous operation is 110°C.

$$T_A = T_J - PR_{\theta JA} = 150°C - 0.438 \times 90°C$$
$$= 110°C$$

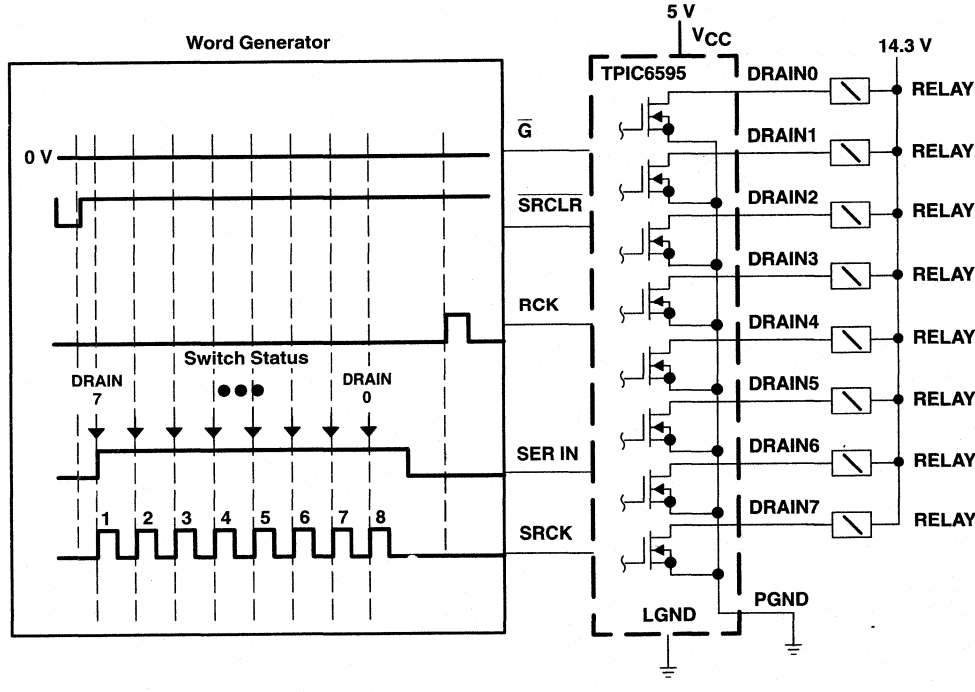


Figure 8. Simultaneous Switching of Eight 12-V, 10/20-A Relays

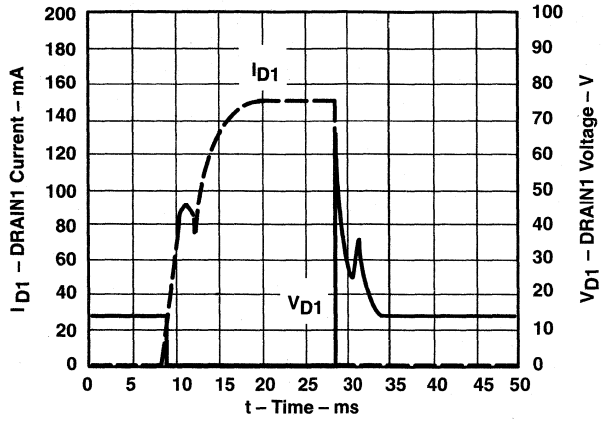


Figure 9. DRAIN1 Voltage and Current Waveforms of Figure 8 Application Circuit

Unipolar Stepper Motor Drive

Stepping motors, due to their digital drive requirements, are natural motion providers for microprocessors or ASIC-based systems. The TPIC6595 provides a simple solution to the problem of translating logic-level timing to high-voltage and current requirements of stepping motors.

The permanent magnet stepping motor has two types of stator winding. The bipolar type has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar type, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux polarity is generated. By passing current through the other winding, the opposite flux polarity is produced. The overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by devices with open-drain outputs such as the TPIC6595.

Printers are one major application of stepping motors because the stepping motor is ideally matched to the needs of paper feeding. In this application, the paper is required to move in well-defined increments, which through gearing equate to fixed numbers of motor steps. Since the paper position is initialized by the user or at paper loading, there is no need for positional feedback. Therefore, the motion system is an open loop, and the paper is advanced by stepping the motor's rotor a given amount.

The system clock is set for a frequency of 4 kHz. This is based on time per motor step of 2.5 ms and a total of ten clock pulses required per each motor step. This is seen in equation (6), i.e., eight clock pulses for the data word plus one additional clock pulse before and after the data word.

$$t_{CLK} = \frac{2.5 \text{ ms/step}}{10 \text{ clock pulses step}} = 0.25 \text{ ms or } f_{CLK} = 4 \text{ kHz} \quad (6)$$

Figures 10, 11, and 12 illustrate two different techniques for driving a unipolar stepping motor with the TPIC6595. The motor is driven at its rated 1-A peak by operating two output DMOS transistors in parallel. In these examples the input logic, which would normally be provided by the system's microprocessor, is generated by a Hewlett Packard HP8180A Data Generator; the logic steps are shown in Table 2 and illustrated in Figure 10.

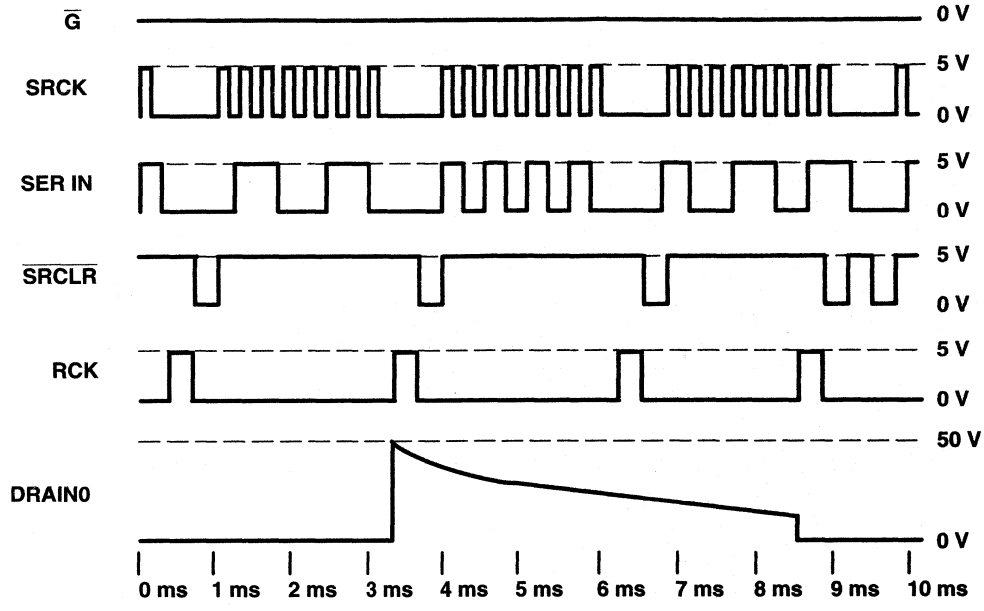


Figure 10. Logic and DRAIN0 Output Waveforms

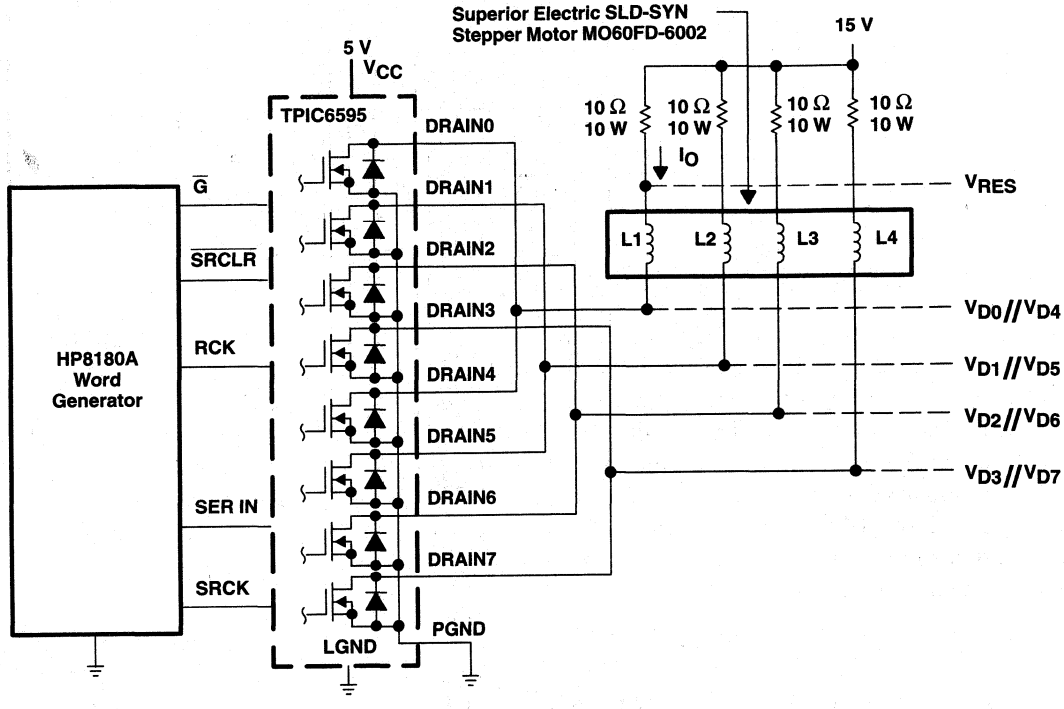
Table 2. Word Generator Program (Four-Step Sequence)

CW STEP†	SER IN INPUT DATA WORD	TPIC6595 SWITCHES ON
1	01010101	DRAIN0 ‖ DRAIN4, DRAIN2 ‖ DRAIN6
2	01100110	DRAIN1 ‖ DRAIN5, DRAIN2 ‖ DRAIN6
3	10101010	DRAIN1 ‖ DRAIN5, DRAIN3 ‖ DRAIN7
4	10011001	DRAIN0 ‖ DRAIN4, DRAIN3 ‖ DRAIN7
1	01010101	DRAIN0 ‖ DRAIN4, DRAIN2 ‖ DRAIN6

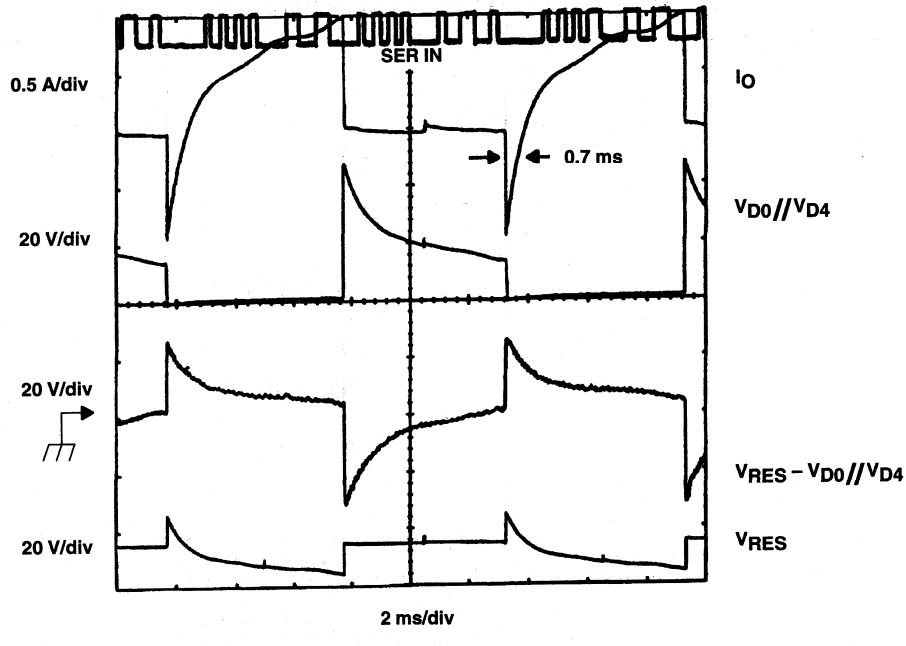
† For CCW rotation, read step sequence up from bottom.

In Figure 11(a), the construction of a stepper motor results in strong magnetic coupling between the stator windings. Consequently, a change in magnetic flux that occurs when the current in winding L1 is interrupted results in an induced current within winding L2. The timing of this motor is such that when D1 parallel with D5 are switched off, D0 parallel with D4 are switched on. The current that is induced in winding L1 is in the negative direction and first flows through the body-drain diode of the DMOS transistors, decays to zero, and then increases in a positive manner. The voltage and current waveforms are shown in Figure 11(b), where it can be seen that the decay time for the negative current is approximately 700 µs. Consequently, the nature of a stepper-motor load causes both positive and negative current to flow through the DMOS power transistor.

It is possible to block the recirculating negative current by placing a diode in series with each pole winding. This is shown in Figure 12(a). In this circuit, the drain is allowed to fly to its clamp voltage, since no current is induced in another motor pole winding. The decay time of the current is now reduced to approximately 310 µs, which is considerably faster than in the previous example. However, since the energy of the pole winding is not transferred to another pole, it must be absorbed by the DMOS transistor. The device then runs considerably warmer than in the previous case. This technique can only be used in an application that does not result in the device's thermal rating being exceeded.

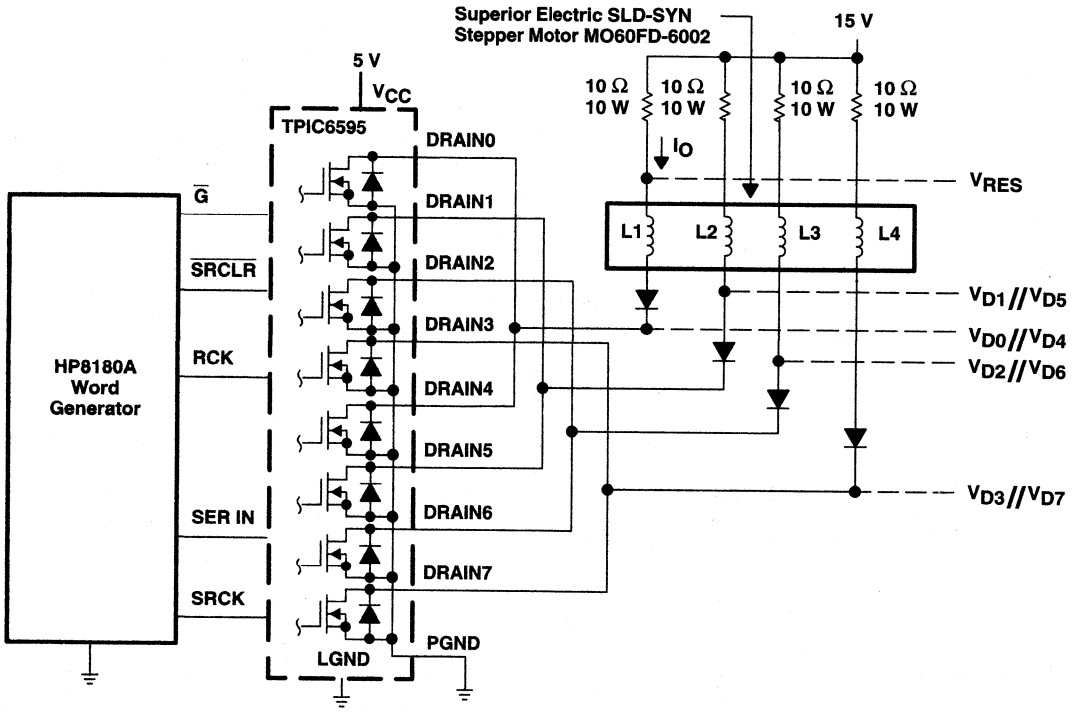


(a) MOTOR DRIVE CIRCUIT

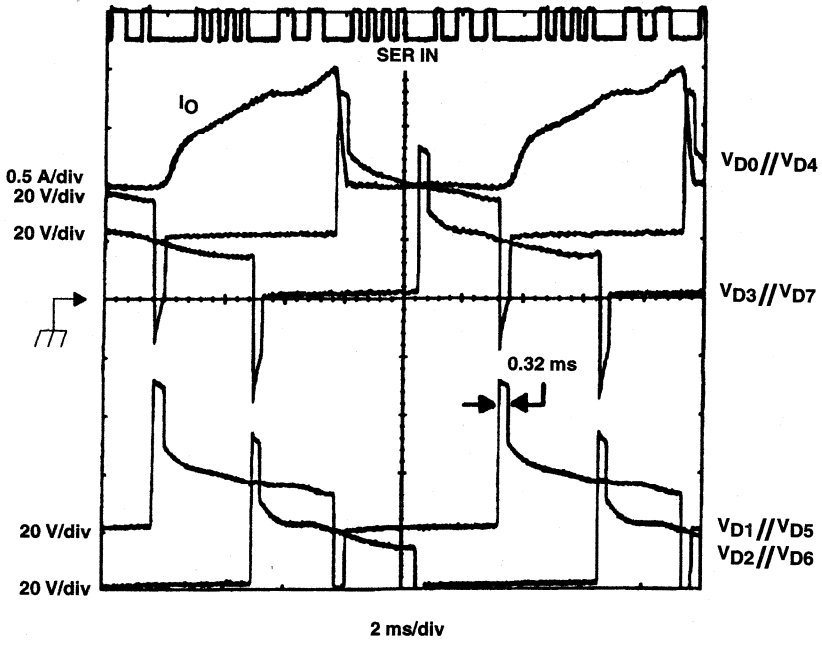


(b) VOLTAGE AND CURRENT WAVEFORMS AT NODES SHOWN IN FIGURE 11(a)

Figure 11. Unipolar Stepper Motor Drive Circuit



(a) MOTOR DRIVE CIRCUIT



(b) VOLTAGE AND CURRENT WAVEFORM AT NODES SHOWN IN FIGURE 12(a)

Figure 12. Current and Voltage Waveforms That Occur in the Winding L1

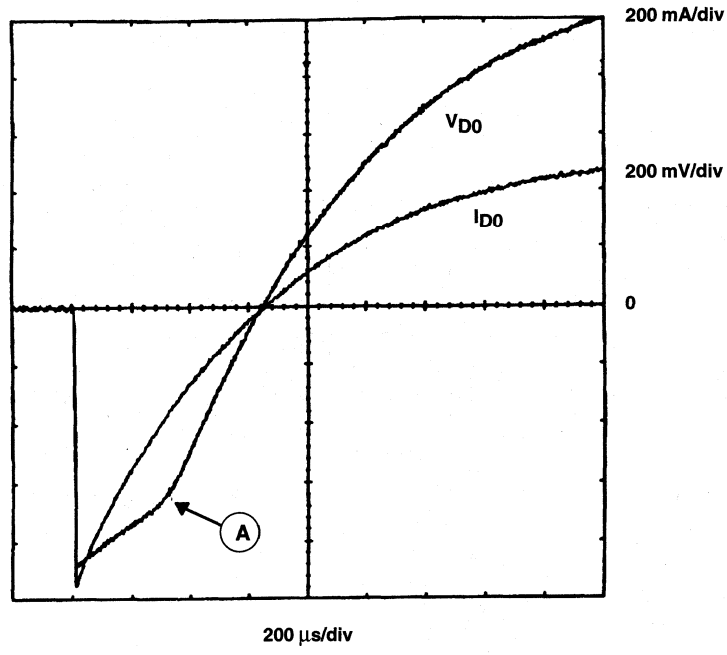


Figure 13. Expansion of Body Diode Reverse-Current Waveform From Figure 10(b)

The current waveform shown within Figure 11 shows that during each winding pulse, both negative and positive current flows through the power switch. A time expansion of the negative current flow region is given in Figure 13.

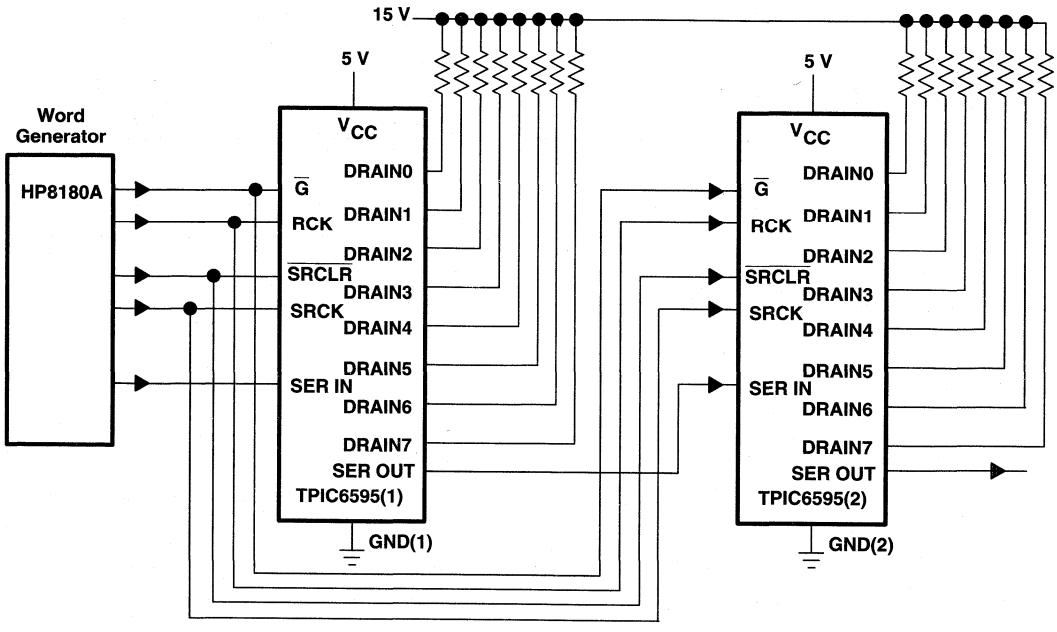
Figure 13 reveals an inflection point (denoted as point A) in the voltage waveform at approximately −700 mV. When the voltage across the device is less than 700 mV, the DMOS transistor is conducting in the reverse direction, and the power dissipation is given by the product of $R_{DS(on)}$ and the square of the drain current. When the voltage across the device is greater than 700 mV, the current flow is split between the source-drain diode and the power DMOS transistor.

A feature of power integrated circuits that is often neglected is their ability to conduct current in the reverse direction. When driving inductive loads, the body drain diode is forced to conduct in the reverse direction and the resulting current flow through this device can have effects on the integrated drive logic, causing functional problems within the device. Special consideration to these problems has been given during the design phase of the TPIC6595, and no susceptibility to this type of problem has been found to exist.

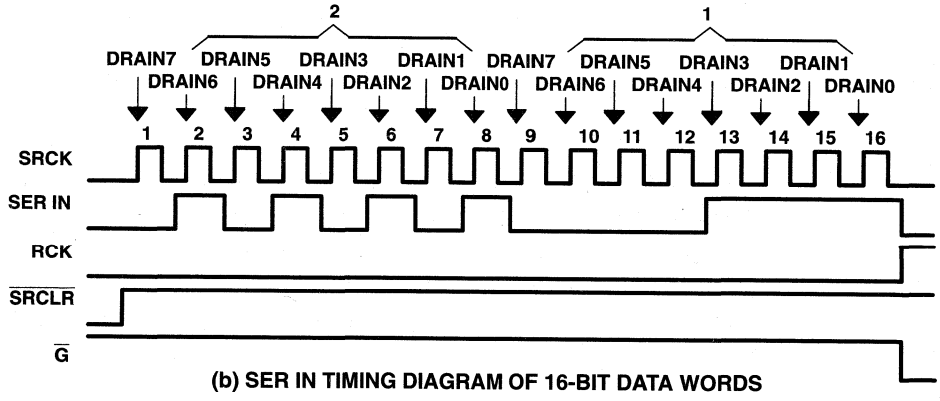
Cascade Operation of Multiple TPIC6595s

By shifting data into SER IN and out SER OUT, TPIC6595s can be connected in cascade. Figure 14 shows two TPIC6595s connected in cascade including an example SER IN timing diagram of the 16-bit data word for turning on the device number 2's output switches DRAIN6(2), DRAIN4(2), DRAIN2(2), and DRAIN0(2) and the device number 1's output switches DRAIN3(1), DRAIN2(1), DRAIN1(1), and DRAIN0(1). Also, Figure 14(b) is an oscilloscope waveform of device number 1's operation per the conditions described.

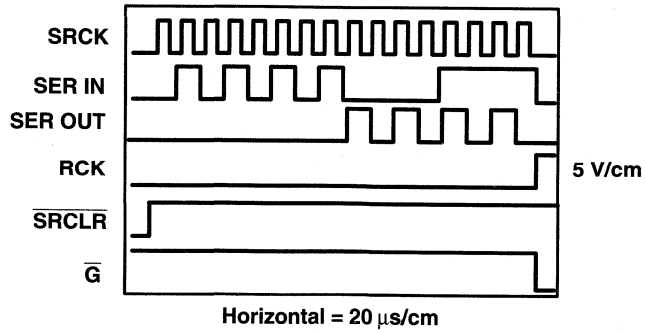
The HP8180A data generator data page for generating the example 16-bit timing diagram explained above is listed in Table 3.



(a) TWO TPIC6595s CONNECTED IN CASCADE



(b) SER IN TIMING DIAGRAM OF 16-BIT DATA WORDS



Horizontal = 20 μs/cm

(c) WAVEFORMS OF FIGURE 14(a) AND SER OUT

Figure 14. Cascade Operation of Multiple TPIC6595s

Table 3. HP8180A Data Generator Data

ADDRESS	STR	DATA (for generator outputs)				
		1–0 Out NRZ RCK	0–3 Out NRZ $\overline{\text{SRCLR}}$	0–2 Out RZ SRCK	0–1 Out NRZ $\overline{\text{G}}$	0–0 Out NRZ SER IN
0000	1	0	0	0	1	0
0001	0	0	1	0	1	0
0002	0	0	1	1	1	0
0003	0	0	1	1	1	1
0004	0	0	1	1	1	0
0005	0	0	1	1	1	1
0006	0	0	1	1	1	0
0007	0	0	1	1	1	1
0008	0	0	1	1	1	0
0009	0	0	1	1	1	1
0010	0	0	1	1	1	0
0011	0	0	1	1	1	0
0012	0	0	1	1	1	0
0013	0	0	1	1	1	0
0014	0	0	1	1	1	1
0015	0	0	1	1	1	1
0016	0	0	1	1	1	1
0017	0	0	1	1	1	1
0018	0	1	1	0	0	0

† The width is equal to 50 µs, delay 0.20 µs.
NOTE: The frequency is equal to 20 kHz.

Simultaneous Turn-on/Turn-off of Eight Inductors That Simulate Driving Solenoids Under Worst-Case Conditions

Figure 15 shows the test circuit and oscilloscope waveforms switching eight high-inductance inductors (R = 60 Ω and L = 250 mH) from a 15.6-V source. The device provides 0.25-A current to each inductor and dissipates 1.12 W as seen in equation (10), which is a safe-operating condition based on the 1.39-W continuous dissipation rating.

$$E_T = E_L + E_s - E_R = \frac{3L_H I_{DM}^2 V_{(BR)DSX}}{6\left[V_{(BR)DSX} - V_{DD}\right] + 4R_L I_{DM}} = 9 \text{ mJ} \quad (7)$$

The calculated power dissipation P_{OFF} is 1.58 W as seen in equation (5).

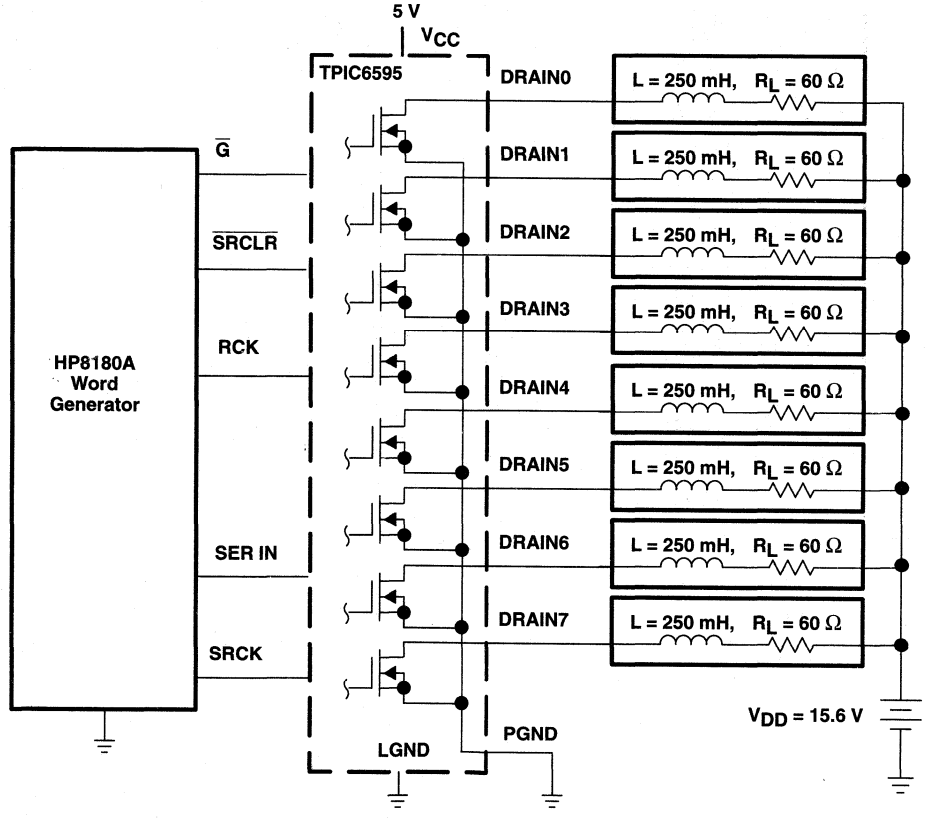
$$P_{OFF} = E_T \times f = 0.009 \text{ J} \times 10 \text{ Hz} = 0.087 \text{ W} \quad (8)$$

$$P_{ON} = I_{DM}{}^2 \times r_{DS(on)} = (0.25 \text{ A})^2\ 3.5\ \Omega = 0.219 \text{ W} \quad (9)$$

$$\begin{aligned} P_{T(AV)} &= P_{OFF} \times n + P(QUIES) + P_{ON} \times d \times n \\ &= 0.087 \times 8 + 0.0001 \times 5 + 0.219 \times 0.24 \times 8 \\ &= 1.12 \text{ W} \end{aligned} \quad (10)$$

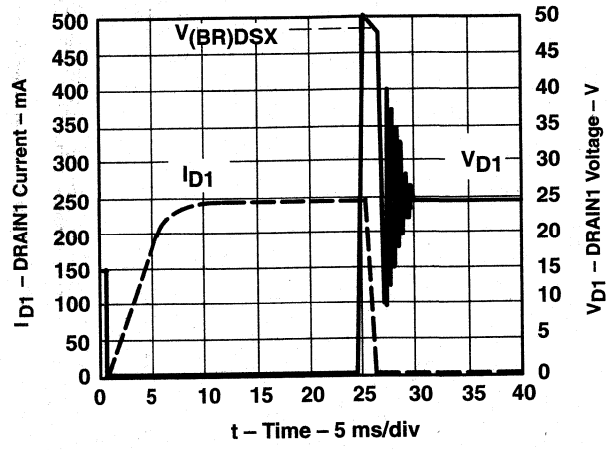
Where:

E_L	Inductive energy stored in inductor	7.7 mJ
E_R	Energy absorbed by resistance during turn-off transient	1.7 mJ
E_S	Energy from power supply during turn-off transient	2.7 mJ
E_T	Total energy absorbed by each switch during turn-off transient	8.7 mJ
f	Switching frequency	10 Hz
d	Duty cycle	0.24
L_H	Load inductance	250 mH
I_{DM}	Peak output load current	0.25 A
N	Number of switches operating	8
P_{OFF}	Turn-off power dissipation each switch	0.087 W
P_{ON}	On-state power dissipation each switch (see Equation 9)	0.219 W
P(QUIES)	Bias power dissipation	0 W
$P_{T(AV)}$	Average total power dissipation	1.12 W
R_L	Inductor resistance	60 Ω
$V_{(BR)DSX}$	Clamp voltage [measured, see Figure 15(b)]	50 V
V_{DD}	Load supply voltage	15.6 V
$r_{DS(on)}$	Static drain-source on-state resistance, T_J = 150°C	3.5 Ω



(a) SIMULTANEOUS TURN-ON/TURN-OFF CIRCUIT

Figure 15. Driving Solenoid Under Worst-Case Conditions



(b) SWITCHING EIGHT HIGH INDUCTIVE LOADS

Figure 15. Driving Solenoid Under Worst-Case Conditions (continued)

Circuit Mechanical Layout Considerations

As in any application where power is being controlled by digital and/or analog signals, it is recommended that special attention be given to the circuit layout. There are a few standard layout techniques that eliminate false triggering of the logic inputs due to noise coupling from the power components. A suggested layout is given in Figure 16.

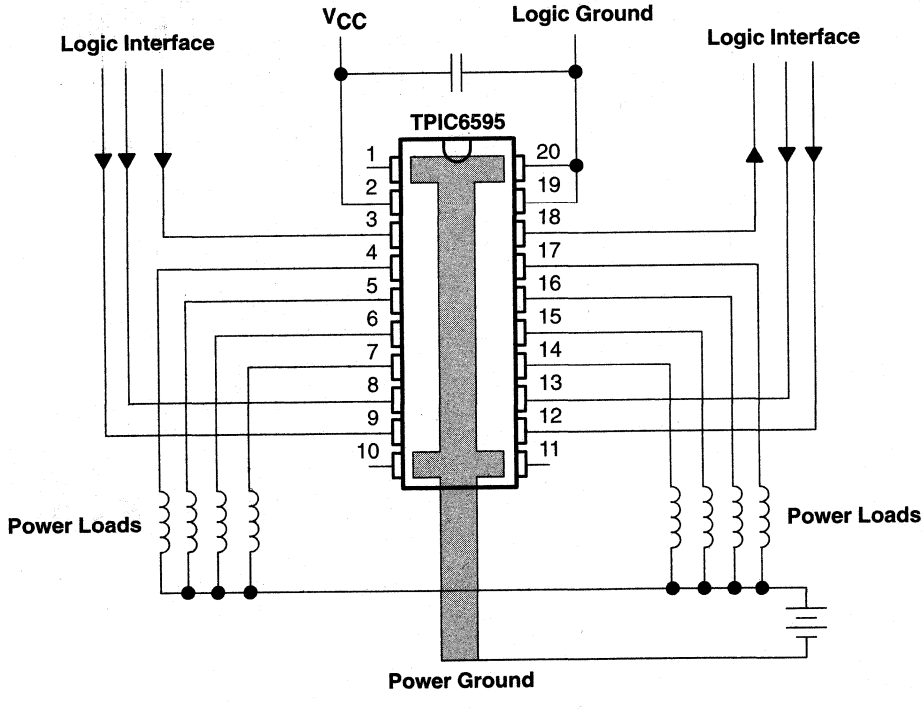


Figure 16. Mechanical Layout

A 0.1-μF ceramic bypass capacitor should be connected across V_{CC} and LGND and placed physically close to the TPIC6595.

A power ground bus should be created on the circuit board that is the return ground for the power loads. The PGNDs connect to the power ground bus.

The ground for the logic interface circuits should be routed separately from the power ground bus. The logic ground and power ground runs should tie in common at only one point; this one connection pin should be placed close to LGND.

The logic components that drive the TPIC6595 should be placed close to the IC.

Conclusion

The TPIC6595 is a monolithic power logic device that contains eight 1.5-A peak/45-V low-side DMOS power switches packaged in a 20-pin dual-in-line plastic package (DIP) and wide-body surface-mount package (DW). Control of the eight power switches is accomplished from a single input by an 8-bit serial word that independently controls each of the eight power switches. All inputs accept standard TTL- and CMOS-logic levels.

The TPIC6595 is a cost-effective single-chip solution for direct control of motors, relays, solenoids, and other high energy, high electrical stress loads. Since the device implements a direct control link between the microcontroller and the system electrical loads, use of multiple logic ICs and discrete power devices are eliminated. The reduction of discrete devices not only reduces cost but saves circuit space and improves system reliability by the reduction of active components.

Acknowledgment

The authors Joe Mings and Dave Cotton wish to acknowledge the contribution of Ross Teggatz and Joe Devore for the report section Functional Description, to Dale Skelton for the section Circuit Mechanical Layout Considerations, and to Ken Echelberger for building the application circuits described and preparing report artwork.

DC Brush Motor Control Using the TPIC2101

TEXAS INSTRUMENTS

In many applications, a key design goal is to minimize variations in power delivered to a load as the supply voltage varies. This application brief describes a simple DC brush motor control circuit using the Texas Instruments TPIC2101 to maintain a constant effective voltage across the motor.

The TPIC2101 is a pulse-width-modulated (PWM) power FET predriver used for speed control of DC brush motors. It can also be used for other applications requiring PWM. The device has three states: Sleep state, Run state, and Fault state.

The Sleep state is the power conserving state. The Run state is the normal operating state of the device. Fault state is entered when the device detects an over voltage or over current condition. The device features two input modes (Manual and Auto), soft start, over/under voltage protection, and the ability to limit the power dissipation of an externally driven device.

Theory of Operation

Figure 1 illustrates a fan motor circuit used in an automobile application. The TPIC2101 generates a pulse width drive to an external power NMOS transistor which is proportional to the input signal while also compensating for supply voltage changes. For a detailed description of each pin, refer to the TPIC2101 data sheet.

Operation Modes

Auto Mode

To assert the Auto mode, an open collector PWM signal is used to pull the AUTO pin low while the MAN (Manual) pin is open. The input PWM frequency required is approximately 100 Hz. This signal is conditioned by the internal circuitry and becomes an output at the SPEED pin. An external RC integrates this signal, which then becomes the input for the INT (integrator) pin. At the INT pin a DC voltage of 0.72 V to 4 V corresponds to an input pulse width from 100% to 0% as seen at pin 3, and will generate an output PWM drive signal at the GD (gate drive) pin varying from 18% to 100% depending on the supply voltage, (V_{bat}). The output gate drive frequency is approximately 20 kHz. The output pulse width in Auto mode is determined by the formula, PWMout = ((2.88 + 13.12 (1–input duty cycle))/V_{bat})*100%. Figures 2 and 2A demonstrate the Auto mode operation.

Figure 2 shows the input configuration for Auto mode. Figure 2A shows the relationship between PWM in (input

SYSTEM BENEFITS

- Constant Load Voltage
- Over Voltage/Current Protection
- Low Power Consumption During Sleep State
- Built-In Soft Start

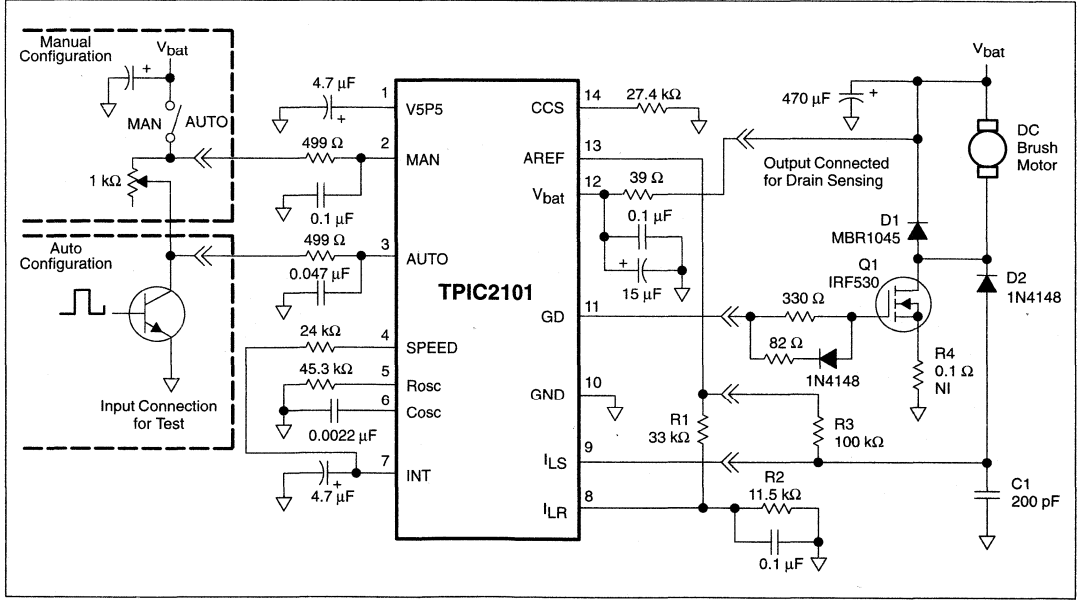


Figure 1. Fan Motor Schematic with PWM Speed Control

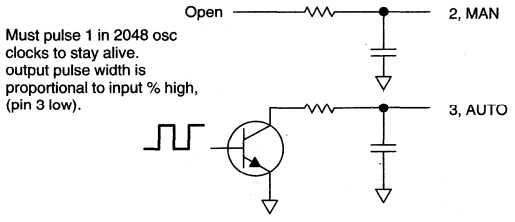


Figure 2. Auto Mode Input

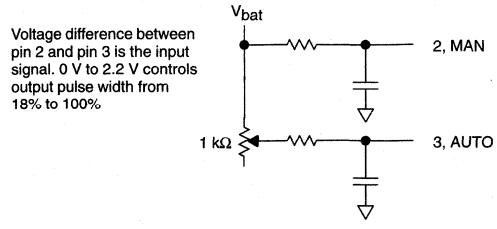


Figure 3. Manual Mode Input

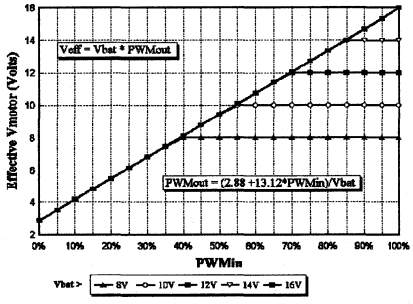


Figure 2A. Auto Mode Effective Voltage

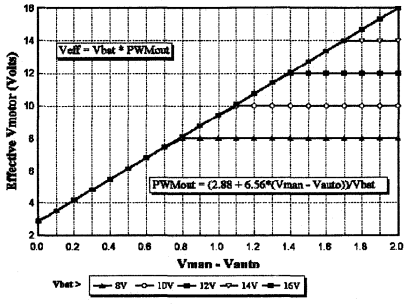


Figure 3A. Manual Mode Effective Voltage

PWM at the base of the NPN transistor) and V_{eff} (effective motor voltage).

Manual Mode

To assert Manual mode, the MAN pin is pulled high, and the voltage difference between the MAN and AUTO pins, 0 V to 2.2 V, determines the IC's output PWM drive signal of approximately 18% to 100% depending on V_{bat}. Just as in Auto mode, the input signal is conditioned by the internal circuitry, output at the SPEED pin, and via an external RC becomes an input of 0.72 V to 4 V DC at the INT pin. Both the MAN and AUTO pins sink 2 mA in the Manual mode. Therefore, simply placing a resistor between the two pins will generate the required input signal. For example, a 1 kΩ potentiometer can be used to generate the 0 V to 2.2 V required for a full range output. The output pulse width in Manual mode is determined by the formula, PWMout = ((2.88 + 6.56) (Vman −Vauto)/V_{bat})* 100%.

Figure 3 shows the input configuration for the Manual mode of operation. Figure 3A illustrates the relationship between the differential voltage (Vman−Vauto) and the effective motor voltage.

Note: In both Auto and Manual modes, the INT pin actually controls the output pulse width by comparing V_{COSC} and V_{INT}. When V_{COSC} is greater than V_{INT}, the GD output is turned off. These waveforms are illustrated in Figure 5. The INT pin could be used as an input for some special applications not requiring the input signal conditioning by floating the SPEED pin and applying the input signal directly to the INT pin as shown in Figure 4.

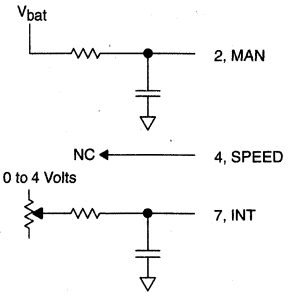


Figure 4. Aux Mode Method

Sleep State

When the integrated circuit is not in Run state, it is in Sleep state. In this condition, the supply current for the IC is reduced from a maximum of 10 mA to less than 200 mA. The purpose of Sleep state is to preserve battery life when applicable.

Soft Start

In order to prevent abrupt application of power to the motor, the TPIC2101 includes a soft start feature that gradually ramps the output signal. When Run state is asserted, the output GD is increased in width from 0 to the commanded percent width over approximately 1 second. As previously discussed, the SPEED pin outputs the conditioned input signal, and the INT pin controls the IC's output pulse width. The resistor between the SPEED and INT pins has a minimum value of 20 kΩ, and the capacitor is selected for the start up time desired, usually 4.7 µF for approximately 1 second to full on.

Figure 5 demonstrates the soft start feature for Manual mode. For this illustration a, 1 kΩ resistor was placed between the MAN pin and the AUTO pin to command a 100% output pulse width. The INT capacitor was reduced to 680 pF for a start up time of approximately 350 µs (this short time is used to make the waveform more visible). On the top trace, the rising edge shows when Manual mode is asserted.

The second trace shows the oscillator which generates the output PWM frequency. The third trace is an overlay of trace two, and illustrates the rise time of the INT pin. The bottom trace shows the GD pulse width increasing from 0% to 100% as the INT pin voltage rises.

Under Voltage

Under voltage occurs when V_{bat} falls below 8 V. Under voltage conditions will cause the device to enter Sleep state with the gate drive held low. Recovery is automatic when V_{bat} increases approximately 1 V above the under voltage threshold. Hysteresis prevents the device from toggling in and out of Sleep state.

Fault States

Over Voltage

Over voltage is sensed by the V_{bat} pin internally and is not user adjustable. Over voltage occurs when V_{bat} rises between 17 V and 20 V. During over voltage condition, GD will be turned off and the device will enter Fault state. Recovery is automatic when V_{bat} decreases 0.5 V to 1 V below the over voltage threshold. Hysteresis will ensure that the condition does not toggle off and on near the threshold.

Over Current (limit)

If while the GD pin is high, I_{LS} (current limit sense) pin is higher than I_{LR} (current limit reference) pin, the internal circuitry will pull the INT pin low, thereby reducing the commanded output GD pulse width. This is on a pulse by pulse basis. This limits the power dissipation of the output device in the short term.

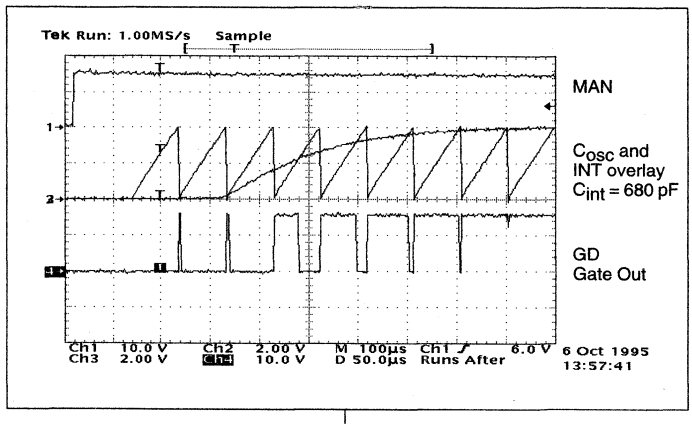


Figure 5. Soft Start

Over Current (fault)

If the above condition persists during the next 64,000 pulses, the IC will enter Fault state with the GD held low for 64,000 pulses. At that time, one automatic restart will be attempted. If the over current condition occurs a second consecutive time, the IC will remain in Fault state until the device is cycled through a Sleep state to a Run state. This is accomplished when the input command is removed and re-established. Note that 64,000 pulses at 20 kHz is approximately three seconds. The actual time will be proportional to the PWM frequency in use. For a more detailed description of the internal circuit, refer to the TPIC2101 data sheet.

Figures 6–8 illustrate the device's response to overload conditions using a drain sense configuration. Refer to Figure 1 for the detailed schematic. Figure 6 demonstrates normal operation without overload. The top trace shows the current in the lead to the INT capacitor. The second trace shows the voltage at the I_{LS} pin. The voltage at the I_{LS} pin rises from zero at the beginning of each pulse at a rate determined by R3 and C1 until it reaches one diode drop above the drain voltage of the external transistor. This is compared by the internal circuitry to the voltage set at the I_{LR} pin. This reference voltage is set by the voltage divider R1/R2 from V_{AREF}. The third trace shows the drain current of the external transistor well under the threshold setting determined by the reference voltage. The bottom trace shows the GD voltage.

In Figure 7, the load has been increased to the threshold setting. The top trace shows that the internal circuit is pulling current out of the INT capacitor which lowers the demand voltage at the INT pin. The second trace is reaching the threshold set by the I_{LR} pin. The third trace shows the drain current at the higher level, and the bottom trace reflects the narrower drive signal, as compared to Figure 6.

Figure 8 illustrates the effect of an additional load increase. As the load continues to increase, the pulse width is substantially reduced. If the load continues to increase until the pulse width is less than the rise time of the sensing voltage at the I_{LS} pin (determined by R3 and C1), overload detect is no longer functioning, and a minimum pulse width has been reached. Therefore, the components should be selected to obtain the minimum width required for starting the motor, within the 64,000 pulses

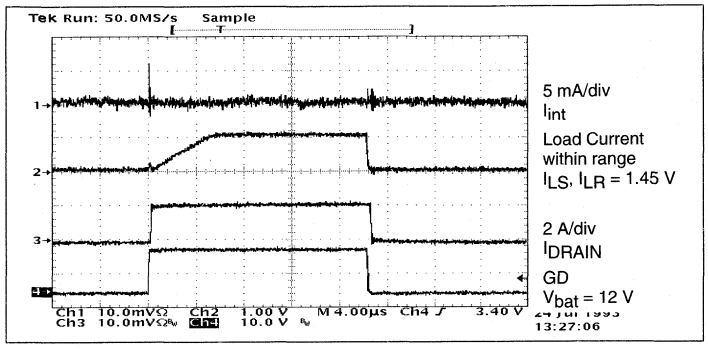


Figure 6. Normal Run State

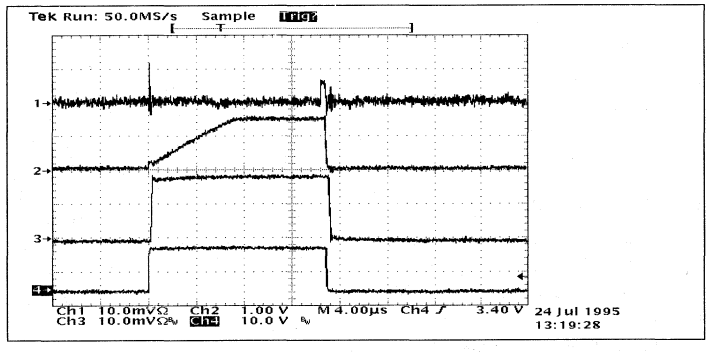


Figure 7. Run State at Threshold

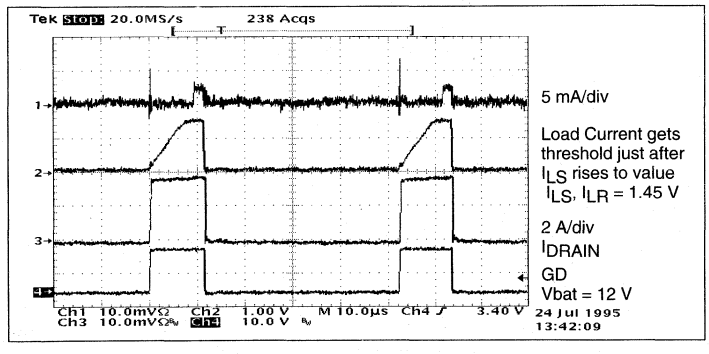


Figure 8. Run State Over Threshold

(approximately 3 seconds), or a fault will be sensed. On the other hand, the pulse cannot be so wide that it allows the external transistor to exceed its power rating.

Run State

Although other output methods can be used, this brief summarizes Run state using the drain voltage sensing method. Referring to the overall schematic Figure 1, the GD pin goes high turning the external transistor full on for a time equal to the commanded pulse width. During that time, current flows through the motor and transistor. When GD goes low, the transistor turns off, but the current in the motor continues to flow by way of the recirculation diode, D1, using the energy stored in the motor inductance.

When GD is low, the I_{LS} pin is held low internally. When GD goes high, capacitor C1 starts charging through R3 from AREF, and the voltage at I_{LS} rises until it is clamped by forward biasing diode D2 to the drain of the external transistor Q1. Therefore, during the on time, the voltage at the I_{LS} pin becomes:

$V_{ILS} = I_D * (R5 + R_{DS(on)}) + VF_{D1}$,

I_D = drain current = 3.6 A (at desired trip point),

R4 = 0.1 Ω (This non-inductive resistor is used for monitoring the current. It is not required for this connection, but must be considered if there),

$R_{DS(on)}$ = 0.1 Ω (On-resistance at 3.6 A from IRF530 data sheet),

VF_{D1} = 0.7 V (Diode forward voltage).

Using these component values, V_{ILS} = 1.42 V.

Also, if the bias at the I_{LR} pin is set by divider R1, R2 from AREF to a value of 1.45 V, overload will trip at 1.45 V +/– 10 mV.

The advantage of drain sensing is that the output device is power dissipation limited. As power dissipation increases, the temperature of the external FET also increases. This rise in temperature results in a higher $R_{DS(on)}$. Therefore, since $V_{DRAIN} = I_{DRAIN} * R_{DS(on)}$, V_{DRAIN}, which is being sensed, responds to that increase. The disadvantage of this method is that the characteristics of the external transistor, such as V_{SAT} drain-to-source, must be considered when selecting the FET.

Conclusions

The TPIC2101 provides a cost effective means of maintaining a constant effective voltage in DC motor applications.

Bidirectional Motor Drive Using the TPIC5201

TEXAS INSTRUMENTS

Since motors play an important role in a wide variety of electronic systems, efficient control of motor speed and torque is an important issue for many system designers. Discrete power MOSFETs, with their low on-state voltages and intrinsic anti-parallel diodes, are a natural choice over bipolar transistors for many motor control circuits. Texas Instrument's new family of Power+ Arrays™ integrates multiple high-performance power MOSFETs on a single chip. These cost-effective devices provide several additional advantages over discrete MOSFETs which make them very well-suited for motor control applications which require pulsed currents of 15 A or less.

Figure 1 shows a bidirectional dc motor being driven from a 14.5 V supply by two TPIC5201 devices arranged in a full H-bridge configuration. This circuit uses two 20 kHz PWM input signals that are 180 degrees out of phase. In most systems, these signals would be supplied by a microcontroller. A 50% duty cycle on both input signals produces a net zero voltage across the motor. Control of the motor's speed and direction of rotation is achieved by varying the duty cycle of one of the input signals while keeping the other fixed at 50% duty cycle. This variation between the input signals results in a net dc voltage across the motor, providing the drive current needed to meet the torque requirements of the motor.

Motor Operation

Typical motor operation is shown in Figure 1 and Figure 2. In this example, the motor is driven in the forward direction, and the motor speed is controlled by varying the duty cycle of input signal B. While input signal A is high and input signal B is low, there is a net negative voltage across the terminals of the motor and current through the motor ramps up. Once input A goes low, a net positive voltage appears across the motor terminals, and the motor current ramps down. When both input signals are low, there is no net voltage across the motor terminals, and the H-bridge recirculates a relatively constant current through its upper stages. To drive the motor in the reverse direction, input signal B is held to a 50% duty cycle, while the duty cycle of input A is varied.

In this example, the pulse width of the input signal is approximately 25 µs at a 50% duty cycle. It is important to note that when switching both the upper and lower transistors on the same side of the H-bridge, a brief delay must occur to allow the conducting transistor to turn off before the nonconducting transistor is allowed to turn on. Without this delay, excessive cross conduction current may result. Cross conduction is a condition in which the upper and lower FETs on

System Benefits

- ▼ Improved power efficiency
- ▼ Reduced pre-drive requirements
- ▼ Improved switching performance
- ▼ Reduced system cost

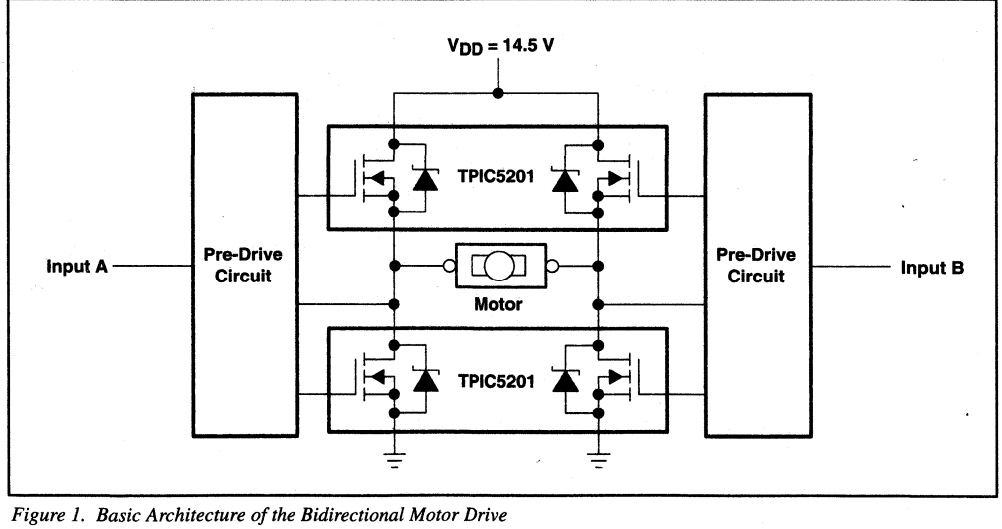
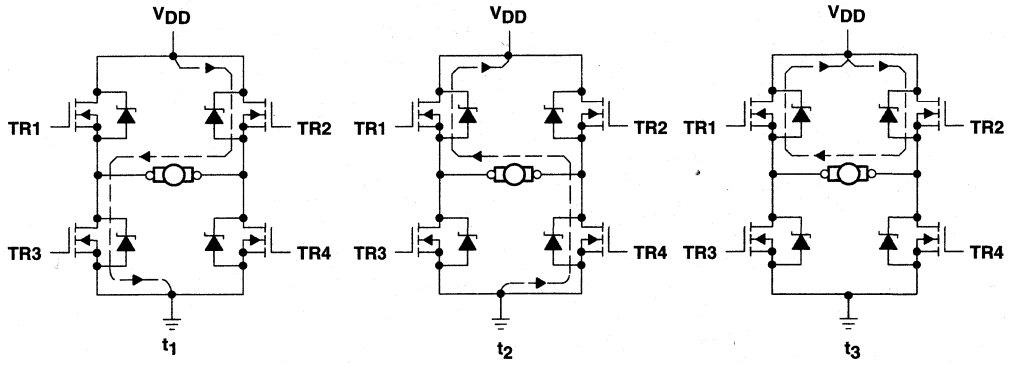
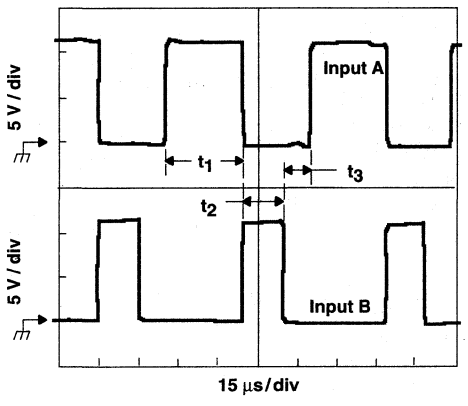


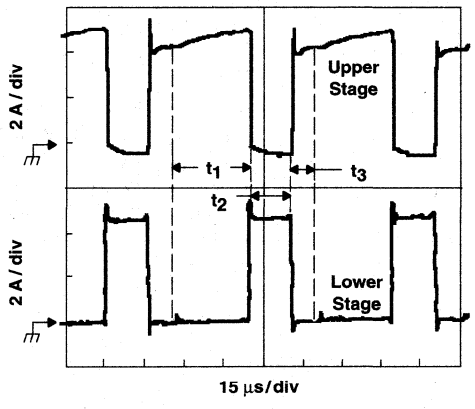
Figure 1. Basic Architecture of the Bidirectional Motor Drive



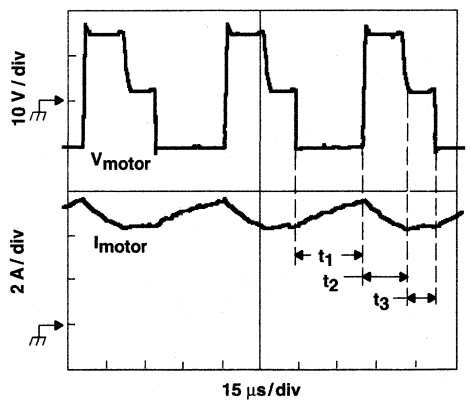
(a) CURRENT PATH THROUGH THE MOTOR AND H-BRIDGE DURING TIME PERIODS t_1, t_2, t_3



(b) INPUT VOLTAGE WAVEFORMS



(c) CURRENT THROUGH THE UPPER AND LOWER STAGE OF THE H-BRIDGE, TRANSISTORS TR2 AND TR4



(d) DIFFERENTIAL MOTOR VOLTAGE AND CURRENT WAVEFORMS

Figure 2. Typical Motor Operation Characteristics

one side of the H-bridge are on simultaneously, providing a low impedance path between the source voltage and ground. While small cross conduction currents can actually be used to enhance system performance, uncontrolled cross conduction can result in excessive heat dissipation and degradation of the device.

Pre-Drive Circuit

In this application, two symmetrical pre-drive circuits are used to drive the gates of the upper and lower FETs. The pre-drive circuit schematic is shown in Figure 3. Drive to the upper transistors is achieved through the use of an HCPL2531 optocoupler followed by an emitter-follower stage. The high-speed optocoupler isolates and level-shifts the upper stage FETs from the input, while providing a reference to ground. The emitter-follower provides low impedance drive for fast charging of the intrinsic gate-source capacitor to enhance switching times.

A 0.1 µF bootstrap capacitor is used to allow the gates of the upper FETs to rise above the supply voltage rail. The bootstrap must be at least 10 times larger than the parasitic gate charge of the TPIC5201, typically 18 nC. Inclusion of the emitter-follower and the bootstrap capacitor allow the upper transistors to be turned on hard when the input signal transitions high.

The low gate capacitance of the TPIC5201 allows for improved efficiency in the motor control circuit. In a power switching application, as the switching frequency increases, switching losses due to the continuous charge and discharge of the gate-source capacitor become the dominant component of the power loss. By minimizing typical gate capacitance, the TPIC5201 reduces switching losses, which results in reduced system power consumption, and improved system efficiency.

The pre-drive circuit includes a delay RC network to insure that cross conduction does not occur. The time constant of this RC

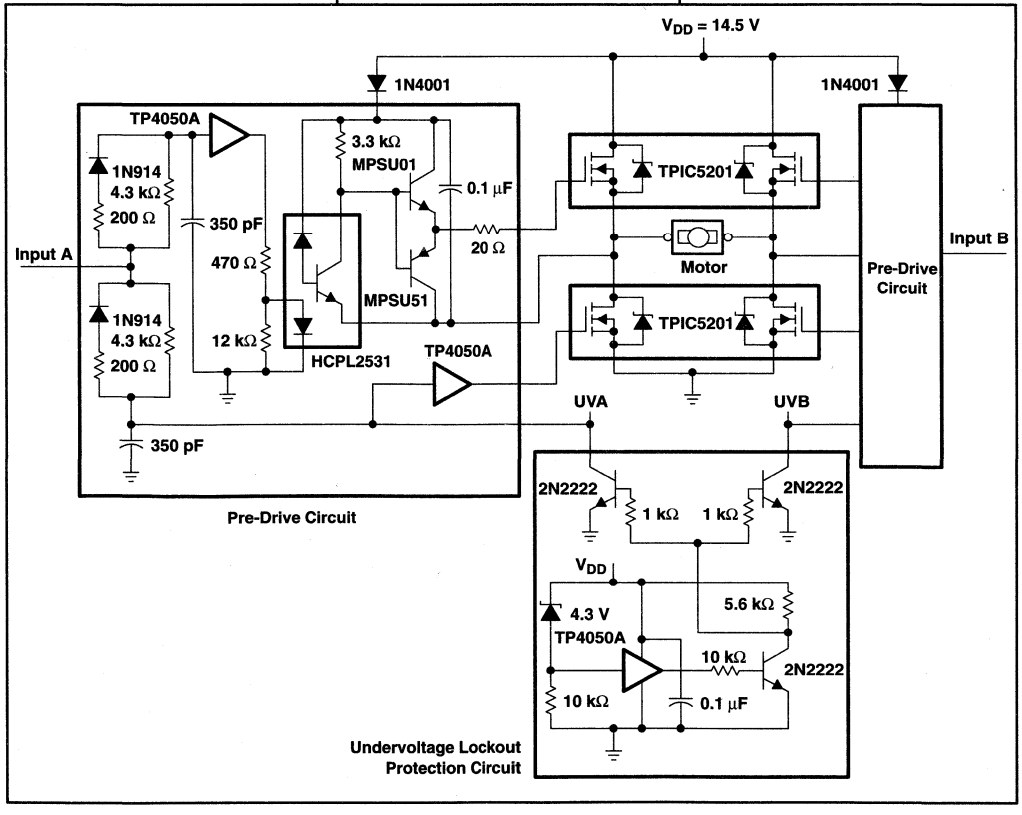


Figure 3. Pre-Drive Circuit Detail

network must be greater than the 0.8 µs propagation delay associated with the switching times of the HCPL2531 optocoupler. By delaying the turn-on drive to the gates of the power MOSFETs, cross conduction currents are eliminated.

External undervoltage lockout protection is added to the circuit to keep the lower stage FETs turned off until a predefined threshold voltage is obtained. This threshold voltage is determined by the threshold of the zener diode coupled with the threshold of the TP4050 buffer. In this circuit, the lower FETs remain off between 2 V and 6.2 V.

Advantages Over Discretes

Since the two power MOSFETs of each TPIC5201 are fabricated monolithically, the FETs within each device are inherently well-matched. As a result, there is little variation in the switching times and transconductance of the upper stage transistors. This device-matching aids in system design by significantly reducing the need for feedback circuitry to compensate for potential switching time mismatches. As a result, the necessary pre-drive circuitry is greatly simplified.

Each power transistor in the TPIC5201 features a low on-resistance of 90 mΩ nominal. By minimizing on-resistance, the power consumption of the H-bridge is reduced, increasing the power available to the motor. Motor control systems built with low on-resistance power switches allow more efficient motor performance. While discrete MOSFETs can offer equivalent on-resistance performance, the integrated TPIC5201 provides low on-resistance more cost-effectively and in less board space than discretes.

The energy capabilities of the TPIC5201 have been characterized over its entire range of operation. The specifications for the TPIC5201 include peak avalanche current versus avalanche time rating curves. Unlike the single point energy specifications typical of discrete MOSFETs, designers using the TPIC5201 can accurately monitor compliance with active safe operating area design constraints.

The TPIC5201 Power+ Array is one of the first devices to provide true integration of discrete power MOSFETs. TI's Power+ Array family of products offer the advantages of integrated circuits with the robustness of traditional discrete power MOSFETs. Excellent device performance, transistor matching, and savings in component cost, board, and heat rail space combine to give the system designer new options for highly-efficient motor control.

Bidirectional DC Brush Motor Control Using the TPIC5404

TEXAS INSTRUMENTS

Motors are pervasive in a variety of electronic systems covering a broad scope of both function and complexity. As trends toward increased automation expand across commercial, industrial, and consumer equipments, the efficient control of motor speed and torque is an increasingly important concern for many system designers.

Developing a motor control system often begins with creating a simple circuit to perform the basic motor drive functions; such a circuit allows the system designer to quickly evaluate the suitability of the selected interface FET's for the motor being driven. This initial evaluation circuit can then be expanded to include additional functionality to fine-tune the control of the motor for the system requirements at hand. This application brief describes a simple, effective circuit using Texas Instrument's TPIC5404 Power+ Array™ to drive a fractional horsepower dc brush motor.

DC brush motors are one of the most frequently selected motor types in use today. Their ease of control and cost-effectiveness account for their popularity. Figure 1 shows a bidirectional dc brush motor being driven from a 10 V supply by a TPIC5404 which has been configured as a full bridge. The specific motor used draws 1 A of current when unloaded, which is within the continuous current rating of the TPIC5404 when two channels are in conduction. The motor drive circuit includes pre-FET drivers to condition the gates of the motor driver FET's. As the transistors array in the TPIC5404 are N-channel structures, a simple charge pump is featured to provide the necessary upper stage gate voltage. A variable duty cycle square wave generator is also included to allow speed control of the motor. The resulting circuit, which can be built from five standard IC's, provides a self-contained, bidirectional, variable-speed motor controller.

Circuit Details

Figure 2 shows the complete schematic for the bidirectional motor controller. The TPIC5404, configured as an H-bridge, creates an effective, single-chip, motor driver. The low on-resistance of the TPIC5404, coupled with its SOIC footprint, results in increased motor operating efficiency and in board space savings.

The FET predrive is accomplished by two SN75372 dual MOSFET drivers. Using integrated FET drivers with an integrated transistor array provides excellent performance matching with minimum skew. The dead time needed between PWM transitions to prevent cross-conduction can be minimized. As a result, the system can be operated at higher frequencies without additional feedback circuitry. Resistors are included between the outputs of the SN75372 devices and the gates of the TPIC5404 motor driver FET's. These resistors, in this example 100 Ω, are sized to control the dV/dt of the motor drive. This slew rate limiting helps reduce potential RF interference.

A charge pump is developed using a TLC555 timer to provide the gate voltage for the upper stage motor drive FET's. Since the charge pump produces a voltage greater than the positive rail, care must be taken to ensure that the maximum transistor gate voltages are not exceeded. In this example, the charge pump generates a voltage approximately 2× the V_{DD} supply voltage. By limiting the V_{DD} supply to a maximum of 10 V, the charge pump provides a V_{GS} of approximately 10 V to the high side transistors when they are in conduction.

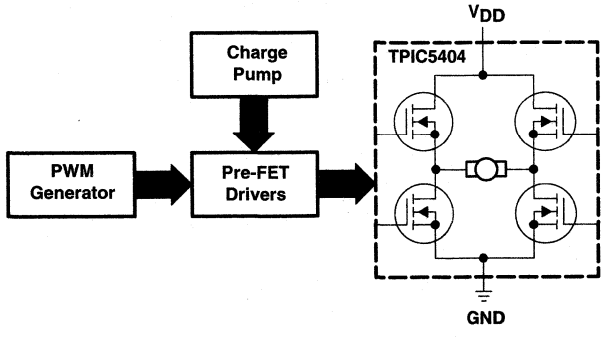


Figure 1. Simplified DC Brush Motor Controller Schematic

System Benefits

- ▼ Simple, cost-effective motor control scheme
- ▼ Enhanced motor operating efficiency
- ▼ Improved switching performance

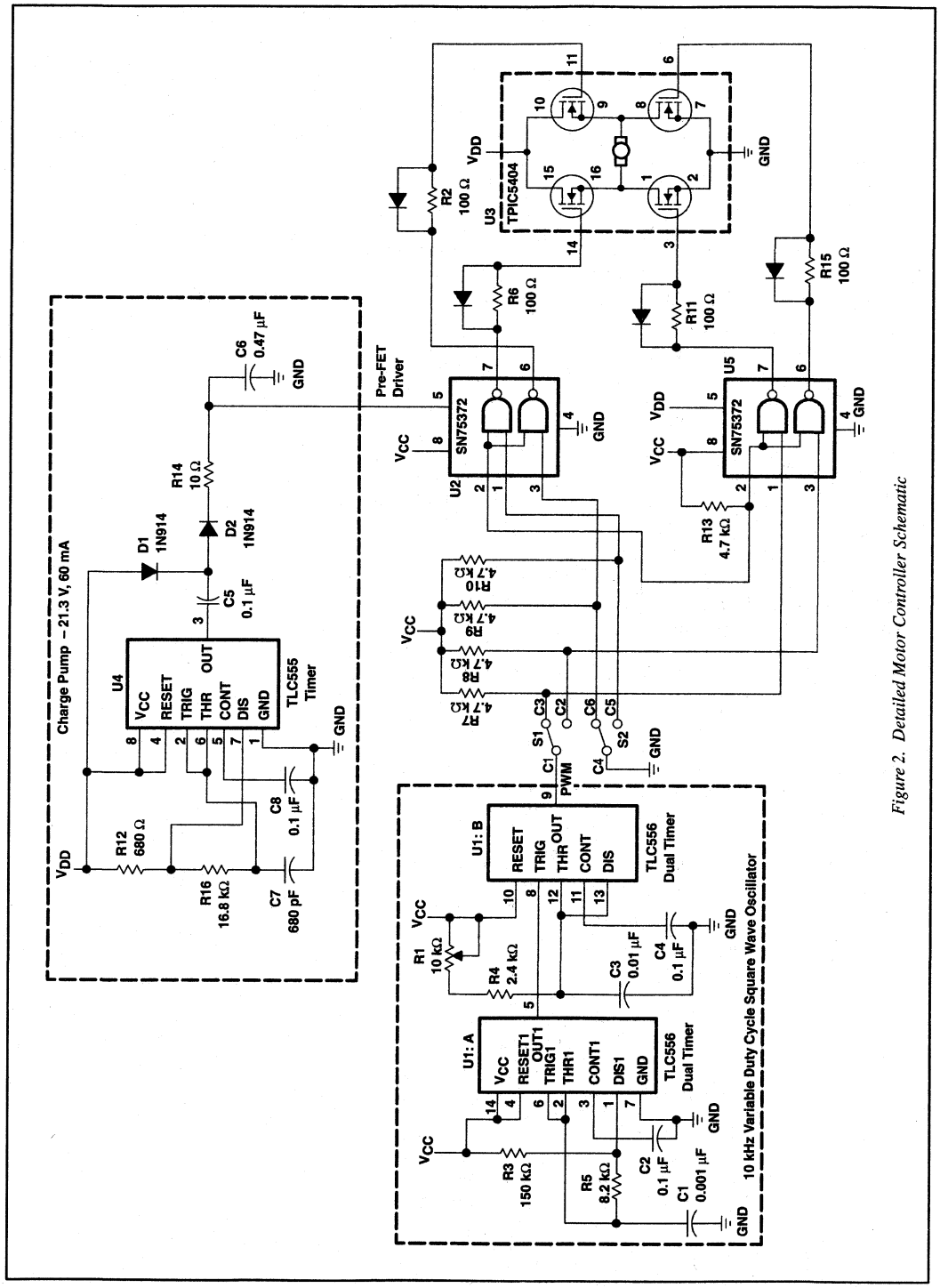


Figure 2. Detailed Motor Controller Schematic

PWM Control

A 10 kHz variable duty cycle square wave oscillator is designed using a TLC556 dual timer. This oscillator generates a pulse width modulated (PWM) output which is used to vary the motor speed. This technique relies on the inertia of the motor averaging the PWM pulses.

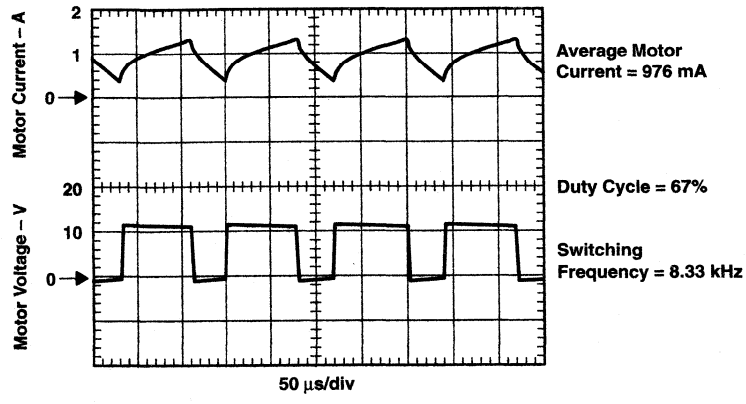


Figure 3 Typical Motor Operating Waveforms

This circuit uses a simple scheme in which the PWM pulses are delivered via switch S1 to the lower stage of the H-bridge, while the upper stage of the H-bridge is connected to a direction switch S2 which controls whether the motor operates in forward or reverse. This scheme has the advantage that at 0% and 100% PWM, the motor sees the full supply voltage (less the on-state transistor voltage drops). A disadvantage of this scheme is that the PWM pattern must be inverted when the motor direction is changed, otherwise the control sense will be reversed – maximum speed becomes 0% rather than 100% duty cycle.

A major concern when using a PWM control technique is that the rapid, repeated switching of the motor driver FET's does not allow a condition in which the right or left pair of transistors is turned-on simultaneously for a significant time. Were this cross-conduction or shoot-through condition to occur, the supply rails would be connected via the transistor bridge, resulting in either severe stress to the H-bridge or unwanted power supply current surges. It is important, therefore, that either the turn-off time of the driver FET's is faster than the turn-on time, or that a dead-time be built into the control circuitry. To help facilitate the design of the turn-on/turn-off dead-time circuitry, detailed gate charge characteristics are included in the Power+ Array data sheets which allow easy calculation of the intrinsic delay time. Nevertheless, including provisions for dead-time adds complexity to the circuit design and slows the system response.

Shoot-Through Elimination

Conventionally, when seeking to push the limits of PWM design, feedback circuitry is used to determine the state of the outputs and control the switching of the motor driver transistor gates. This implementation can be complex, but when using discrete MOSFET's, it is a workable solution which enables a system to switch faster than would otherwise be possible. When using an integrated Power+ Array, such as the TPIC5404, the transistor gate characteristics are closely matched. As a result, a much simpler scheme for eliminating shoot-through may be used.

The example circuit uses a resistor and diode at each gate to control shoot-through. The resistor reduces the turn-on time of the motor drive FET's by limiting current to the gate. The diode provides a bypass for the resistor when turning-off, thereby giving a faster transistor turn-off than turn-on. This means that near-simultaneous transitions can be generated by the control logic, without risk of destroying the FET's through simultaneous conduction. Combining this simple scheme for preventing shoot-through with the simplified control logic previously discussed, a worthwhile reduction in system size and cost can be realized when combined with the up-integration benefits of the TPIC5404 Power+ Array.

Four-Wire 16-Lamp Remote Power and Brightness Control With Power+ Logic™

TEXAS INSTRUMENTS

The two devices, TPIC6A595 and TPIC6595, are Power+ Logic™ shift registers. They can be loaded remotely by means of clock and data signals and cascaded in long chains suitable for (e.g.) video display systems. The input logic function follows the SN74HCxxx numbering convention so that SN74HC595 and TPIC6595 are both shift registers.

The eight outputs are well-specified lateral double-diffused MOSFETs (LDMOS FETs) with excellent avalanche energy characteristics. These ensure that it is possible to predict their performance in inductive circuits which return energy to the switch. This can prevent the mysterious field failures often encountered with unsnubbed bipolar devices in similar applications. At the time of writing, other members of the family of Power+ Logic devices include the TPIC6273, TPIC6259, and TPIC6A259.

The Demonstrator

The demonstrator described here provides two cascaded devices and the schematic shows them driving incandescent lamps (and/or LEDs), Figure 1. The principal features of the two devices are shown in the Power+ Logic block. Figure 2 shows the common device diagram. The input format is a data clock and data signal with a transfer clock pulse to load the holding registers. Figure 3 illustrates the output structure which integrates a substantial protection network. This enhances the avalanche energy capability which in turn helps dissipate the energy returned by (e.g.) inductive loads.

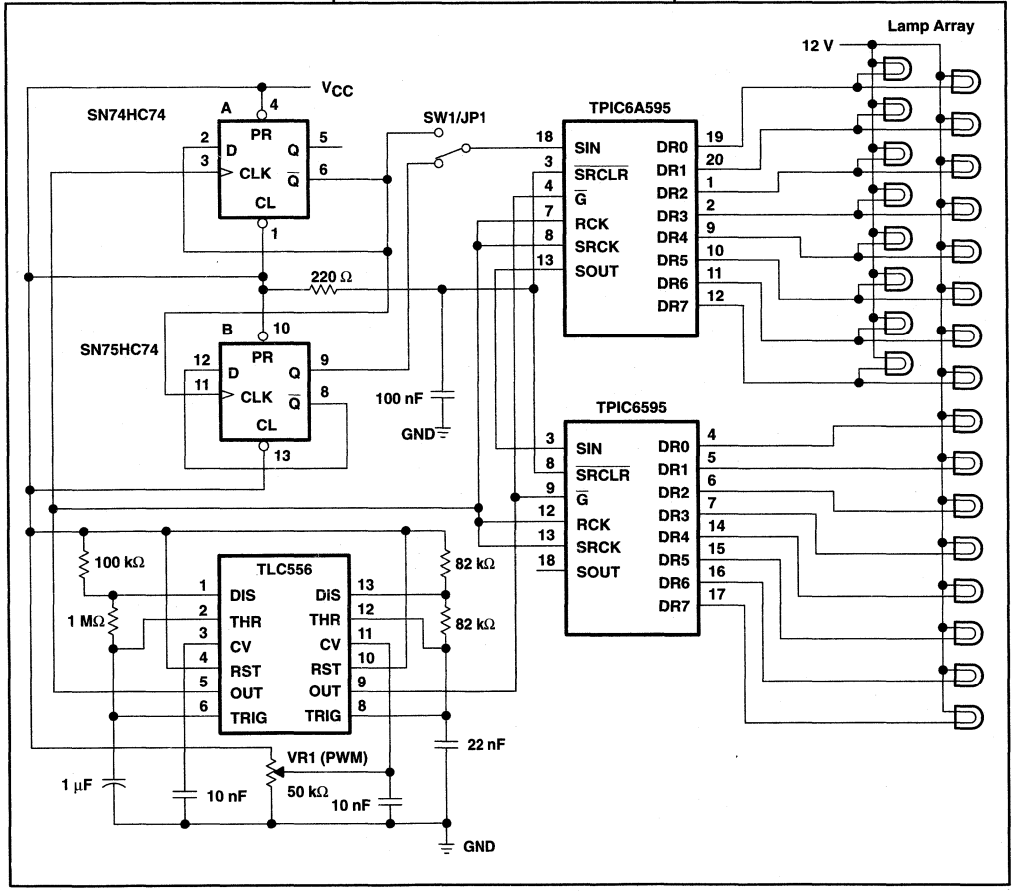


Figure 1. Circuit Schematic

Power+ Logic

- TPIC6xxx series – 0.25 A, 1.5 A pk, 45 V, 1.3 Ω, 75 mJ, 20-pin DIP or 20-pin SO package
  - TPIC6259 – 8-Bit addressable latch
  - TPIC6273 – Octal D-type latch
  - TPIC6595 – 8-Bit SIPO (shift register)
- TPIC6Axxx series – 0.35 A, 1.1 A limit, 50 V, 1 Ω, 75 mJ, 20-pin DIP or 24-pin SO package
  - TPIC6A259 – 8-Bit addressable latch
  - TPIC6A595 – 8-Bit SIPO (shift register)

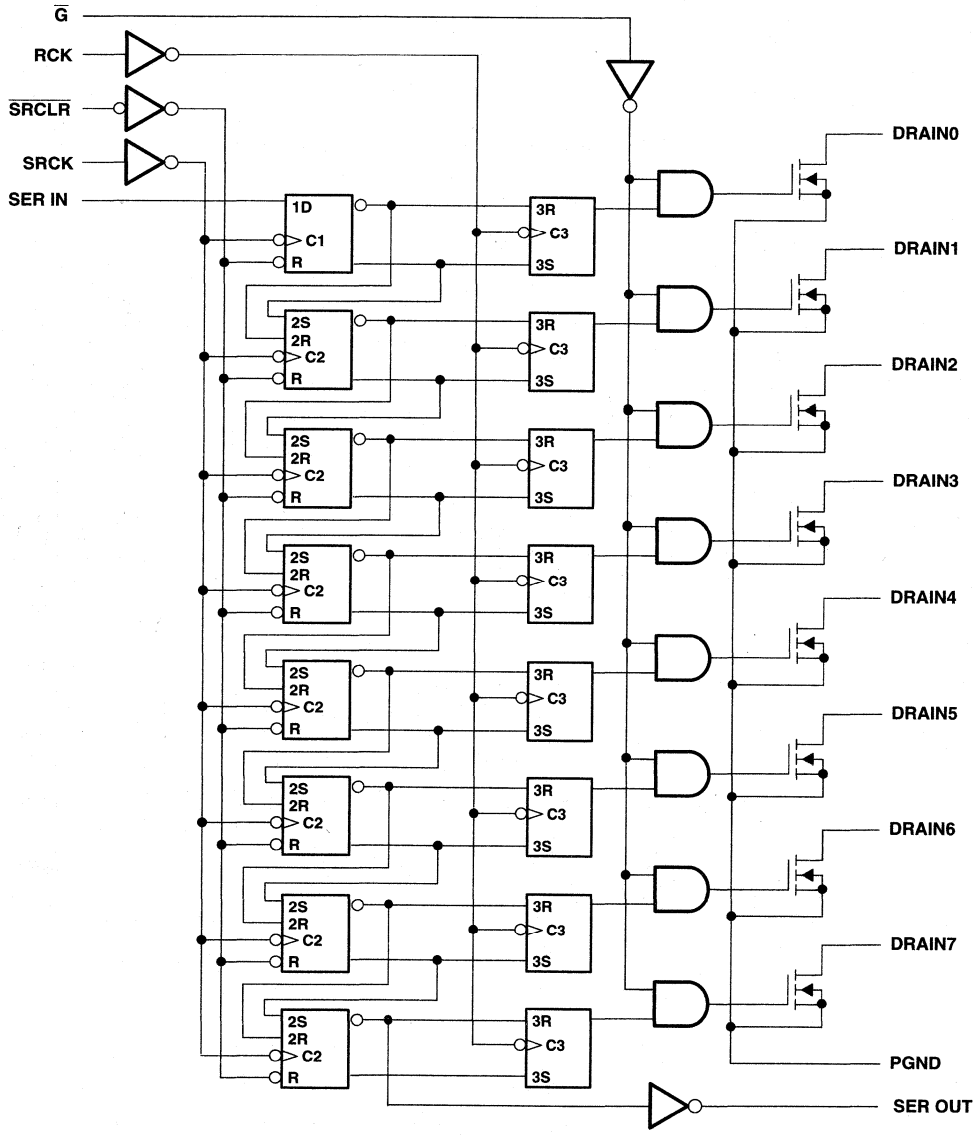
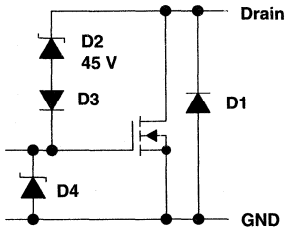


Figure 2. Common Block Diagram of TPIC6595 and TPIC6A595



- D1 is an integrated body drain diode
- D2 and D3 are added to provide improved unclamped energy capability
- D4 is added to prevent gate oxide damage

Figure 3. Power+ Logic Output Structure (Typical Schematic – All Drain Outputs)

PWM and Incandescent Lamps

The pulse-width-modulated (PWM) output current limit on the TPIC6A595 is particularly useful when driving incandescent lamps. These lamps exhibit current surges many times greater than the continuously rated figure when first turned on.

These current surges are due to the considerable change in temperature of the incandescent filament and a corresponding change in its resistance. Figure 4 illustrates a typical current characteristic where a nominally 190 mA lamp takes an initial current of over 2 A from a 15 V supply.

Other advantages to the current limit include immunity from failures due to short circuits at the output and the ability to start larger motors than an unlimited part. It can also be of use when driving stepper motors whose resonance problems are greatly reduced when the motor is current controlled.

The TPIC6595 has been configured to drive either eight incandescent lamps or four lamps and four LEDs. The TPIC6A595 has sixteen lamp positions arranged as eight parallel pairs to reflect its greater current capability (and PWM current limit). When only eight lamps are to be used, the parallel positions are convenient for evaluating the short-circuit capability or attaching test probes.

The TPIC6A595 has built-in short-circuit protection. The TPIC6595 does not and care should be taken to avoid shorting unprotected outputs.

output holding registers. In a more conventional system, the data would be loaded into all the shift registers using SRCK, then a single pulse of RCK would transfer the data to the holding registers.

The clear input $\overline{\text{SRCLR}}$ is held high at all times and does not affect the data in either register bank. In another system, it might be used to clear the shift registers before reloading.

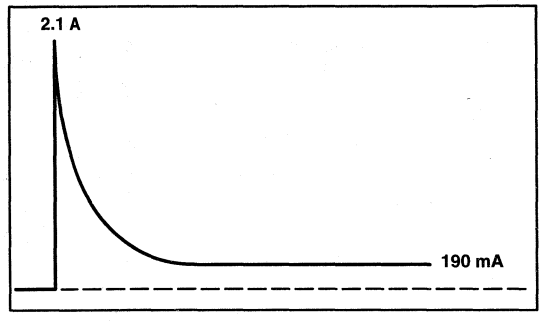


Figure 4. Lamp Inrush Characteristic

System Logic

The clock and data generator logic is reduced to a minimum; half of the TLC556 dual timer is used to generate a slow clock signal (around 1 Hz). This is used to drive both shift-register (SRCK) and holding register (RCK) clocks, as shown in the block diagram, Figure 5.

Data is therefore clocked into the shift register on the rising edge and is also transferred from there to the

PWM Brightness Control

The output enable $\overline{G}$ is used in conjunction with the other half of the TLC556 to provide a common brightness control for both TPIC devices. This works with the TLC556 configured as an astable PWM generator whose pulse width is altered by VR1. As this is altered, the duty cycle of the TPIC's output enable $\overline{G}$ changes. This provides a range of brightness control from very dim to full on.

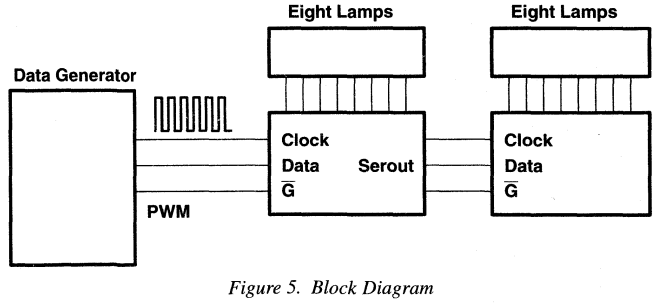


Figure 5. Block Diagram

Data Generator

Serial data for the TPIC devices is generated by dividing the clock by 2 or by 4 using an SN74HC74. A moving pattern will travel down the two shift registers. The serial data output of the TPIC6A595 is connected to the data input of the TPIC6595. This can be extended to suit the application and is particularly useful with large video LEDs or lamp arrays.

A switch (or jumper) is used to select the data division ratio which causes a change in the pattern of lamp illumination. Should all 1s or all 0s be needed for test purposes, a jumper is recommended rather than a switch. A connection to V_{CC} or GND can then be made to the center pin.

Three-Wire, Four-Wire, or Five-Wire Interface

The total connection between the TPIC devices and their control logic is therefore four wires, combined clock (SRCK and RCK), data, output enable ($\overline{G}$), and ground. In a system requiring transparency in the loading of the data, a separate RCK line would be justified. In a minimal system lacking a brightness control, the $\overline{G}$ wire could be omitted, reducing it to a three-wire interface.

PCB Layout

The printed circuit board layout is intended to minimize noise problems due to switching high currents adjacent to high-impedance logic inputs and care is taken to decouple V_{CC} locally on both devices. The short, wide tracking from logic and power grounds to the supply point minimizes the inductive and resistive EMFs generated when switching high currents, as shown in Figure 6. The PCB overlay is shown in Figure 7.

Although the clock in this system is slow, extensive use is made of ground and supply planes. Since the Power+ Logic parts are high speed CMOS logic devices, they can be clocked at over 20 MHz. This speed is invaluable when driving large arrays such as emulating a video screen with an array of LEDs or even incandescent lamps, see Figure 8.

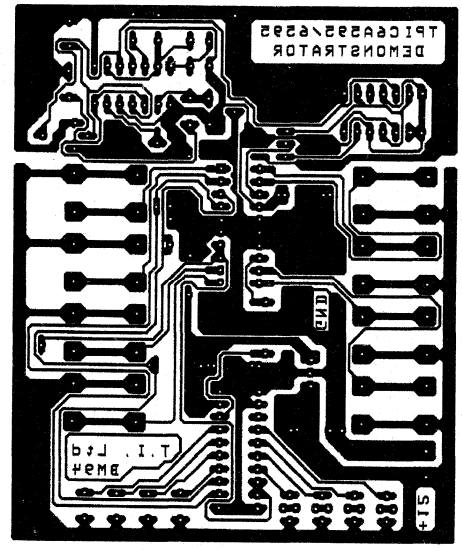


Figure 6. PCB Track Layout (Single-Sided)

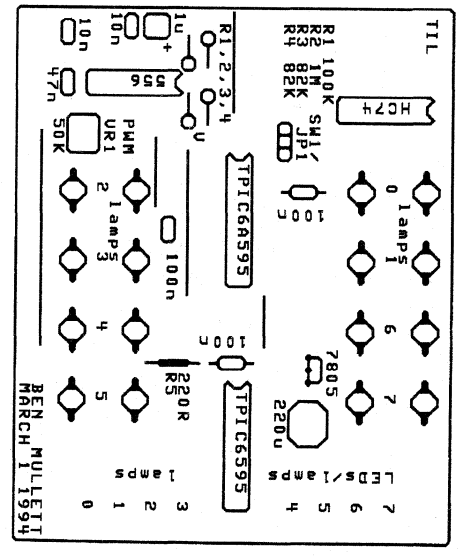


Figure 7. PCB Component Overlay

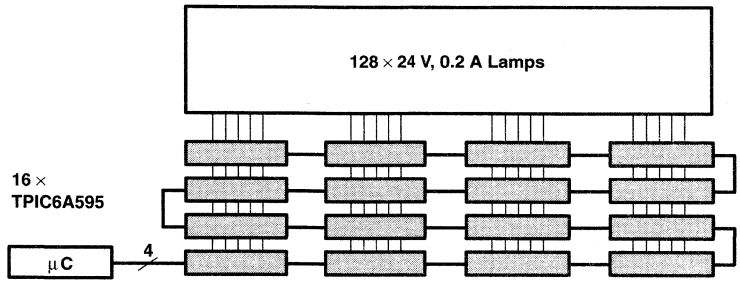


Figure 8. Driving Large Lamp Arrays

Load Problems

Matching a device to a load can cause problems when the load is as variable as an incandescent lamp. There are limitations even to PWM current limit schemes. For example, the TPIC6A595 PWM current limit is specified in the data sheet to deliver an approximate 2% duty cycle current limited to a peak value of typically 0.8 A.

Should a lamp (or lamps) require more than this to move up the resistance/temperature curve, the output PWM will remain in 2% duty cycle mode indefinitely as in a partial short circuit. It is wise to check what a given type of lamp requires as a start-up current and to remember that this is also temperature dependent. It should be remembered that if the earlier example (the 190 mA lamp) were used with a 250 mA switch, the initial current surge of over 2 A would in all probability destroy a bipolar switch.

To estimate this surge without recourse to dynamic testing of each device, the value of the cold resistance will indicate the size of the initial surge on a given supply voltage. It can be revealing to do this on an existing piece of equipment. Since cold resistance has not always been taken sufficiently into consideration, this may be the underlying cause behind sporadic field failures.

Summary

In conclusion, the demonstrator shows the ease of driving lamps and LEDs with these Power+Logic products over a minimal 3-wire interface with improved benefits when additional signal wires are added. Remote control of lamp brightness is one of these benefits, such as using a PWM control signal on the $\overline{G}$ enable line.

Parts List

Integrated Circuits

uA7805C	Voltage regulator –5 V, TO-220
TLC556N	Timer IC
SN74HC74N	Dual D-type
TPIC6595N	8-Bit shift register with 250 mA output
TPIC6A595NE	8-Bit shift register with 350 mA output and PWM current limit

Passives

1 MΩ	Resistor, 1/8 Watt
100 kΩ	Resistor, 1/8 Watt
82 kΩ (2)	Resistor, 1/8 Watt
220 Ω	Resistor, 1/8 Watt
50 kΩ	Resistor, variable
220 μF	Electrolytic capacitor, 16 V or better
1 μF	Electrolytic capacitor, 16 V or better
100 nF	Non-polarized capacitor, 6 V or better
47 nF	Non-polarized capacitor, 6 V or better
10 nF (2)	Non-polarized capacitor, 6 V or better

SPDT switch or jumper as preferred (see text).

Lamps

TPIC6595:	8–14 V, 55 mA, sub-miniature lamps or similar, or 4 lamps and 4 LEDs with 4 current-limiting resistors to suit.
TPIC6A595:	8–14 V, 190 mA, 10 mm lamps or similar.

Contents

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as shown in the following example.

Example: **TPIC** **1301** **DW**

Prefix

MUST CONTAIN ONE TO FOUR LETTERS

SN ..... TI Special Functions or Interface Products
TPIC ..... TI Power IC Products

STANDARD SECOND-SOURCE PREFIXES

DS ..... National
L ..... SGS
ULN ..... Sprague

Unique Circuit Description

MUST CONTAIN THREE OR MORE CHARACTERS
(From Individual Data Sheets)

Examples: 293 6B595
2701 754410
2322L 75437A

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DW, FK, JG, KC, KV, N, NE, P
(From Pin-Connection Diagram(s) on Individual Data Sheets)

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (JG, N, NE, P)
– A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW)
– Tape and Reel
– Antistatic or Conductive Plastic Tubing

Chip Carriers (FK)
– Antistatic or Conductive Plastic Tubing

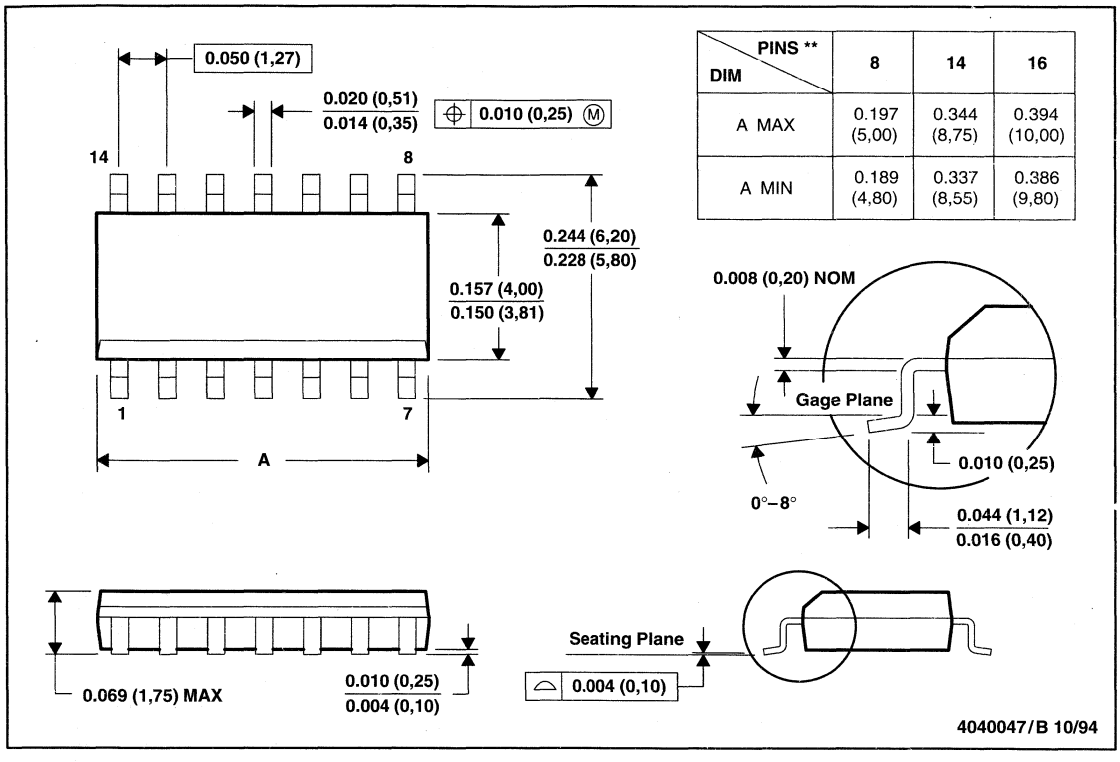
Power Tab (KC, KV)
– A-Channel Antistatic or Conductive Plastic Tubing

JANUARY 1996

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

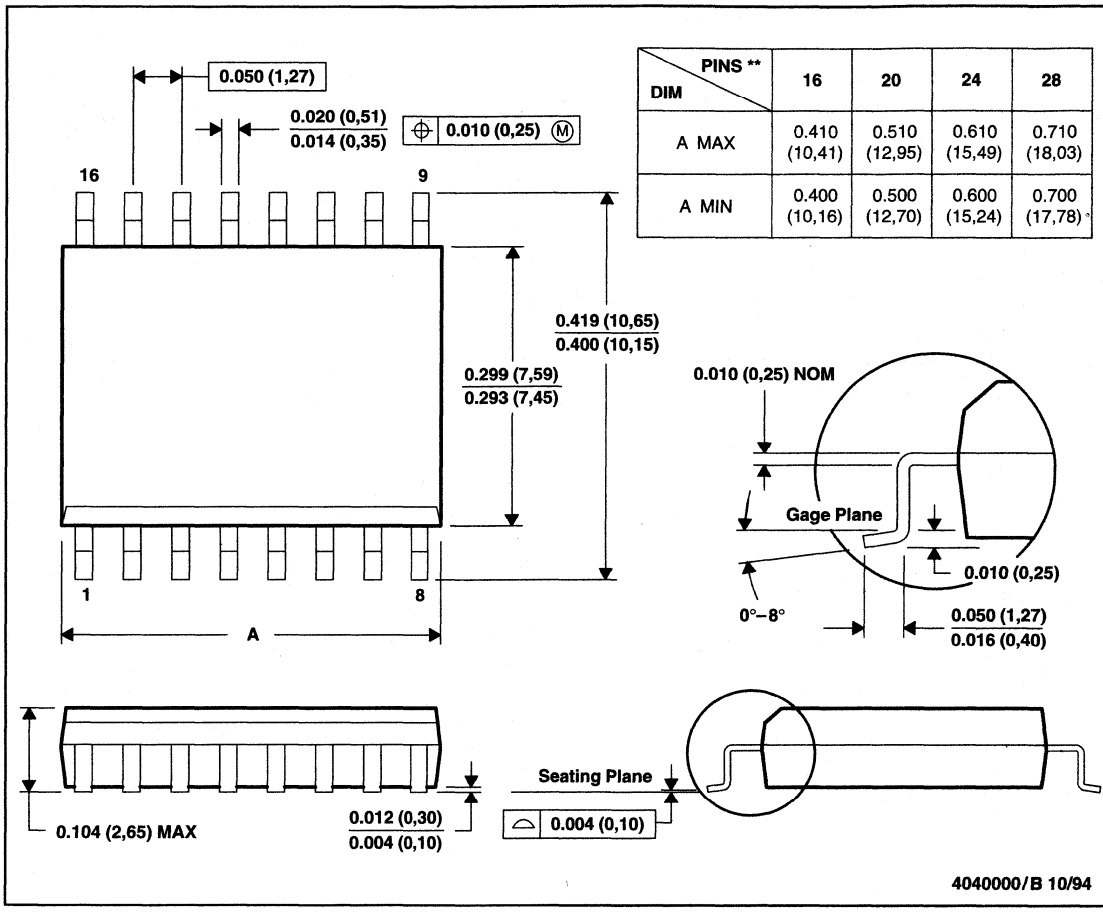
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

JANUARY 1996

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



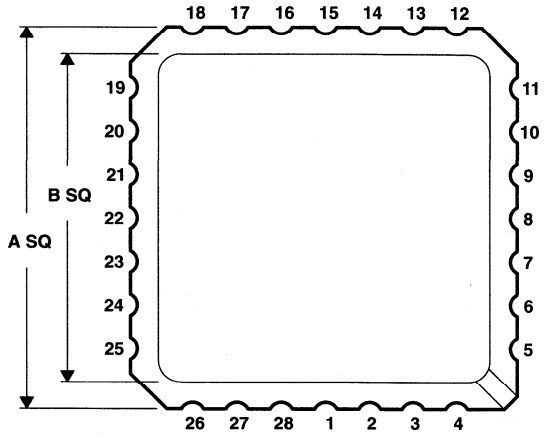
DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

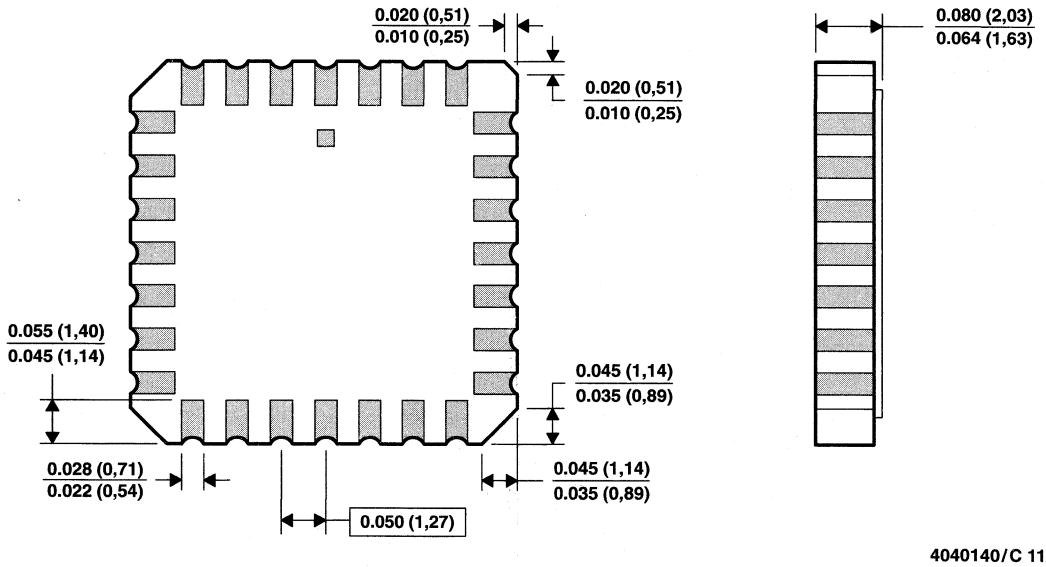
JANUARY 1996

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

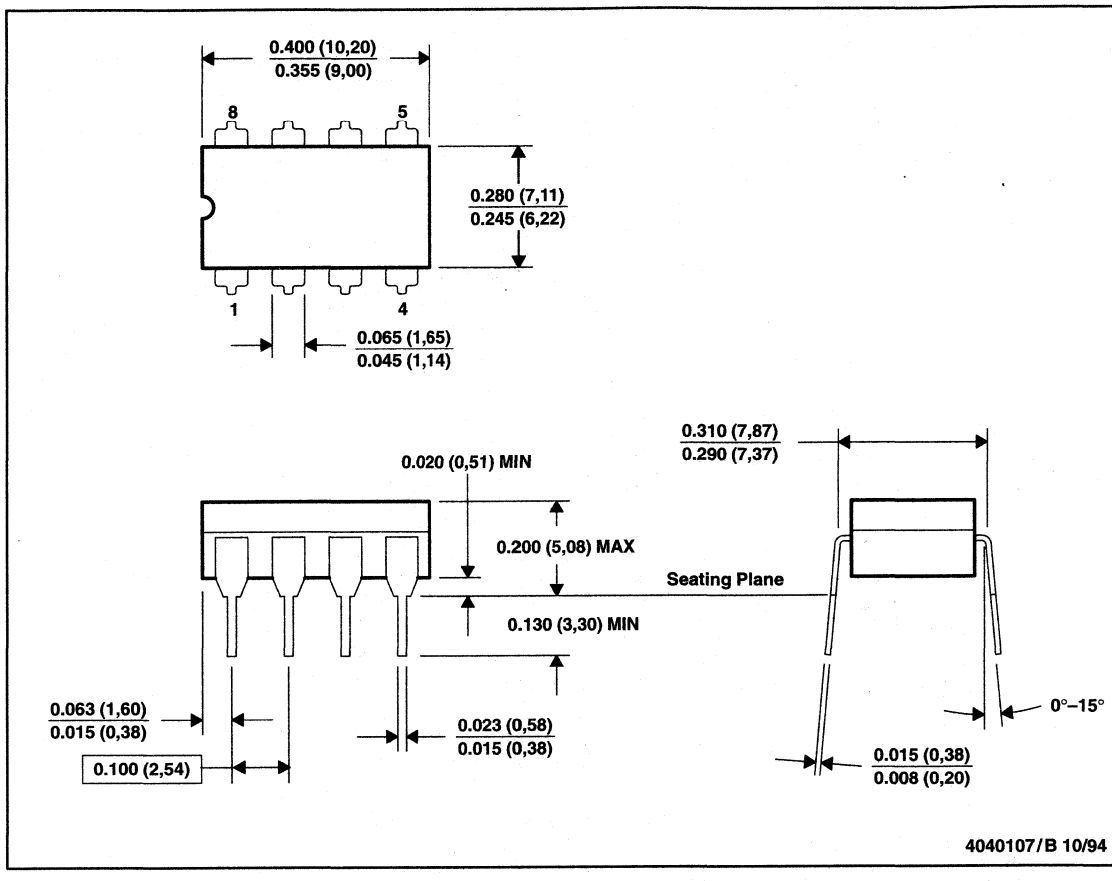


4040140/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

JANUARY 1996

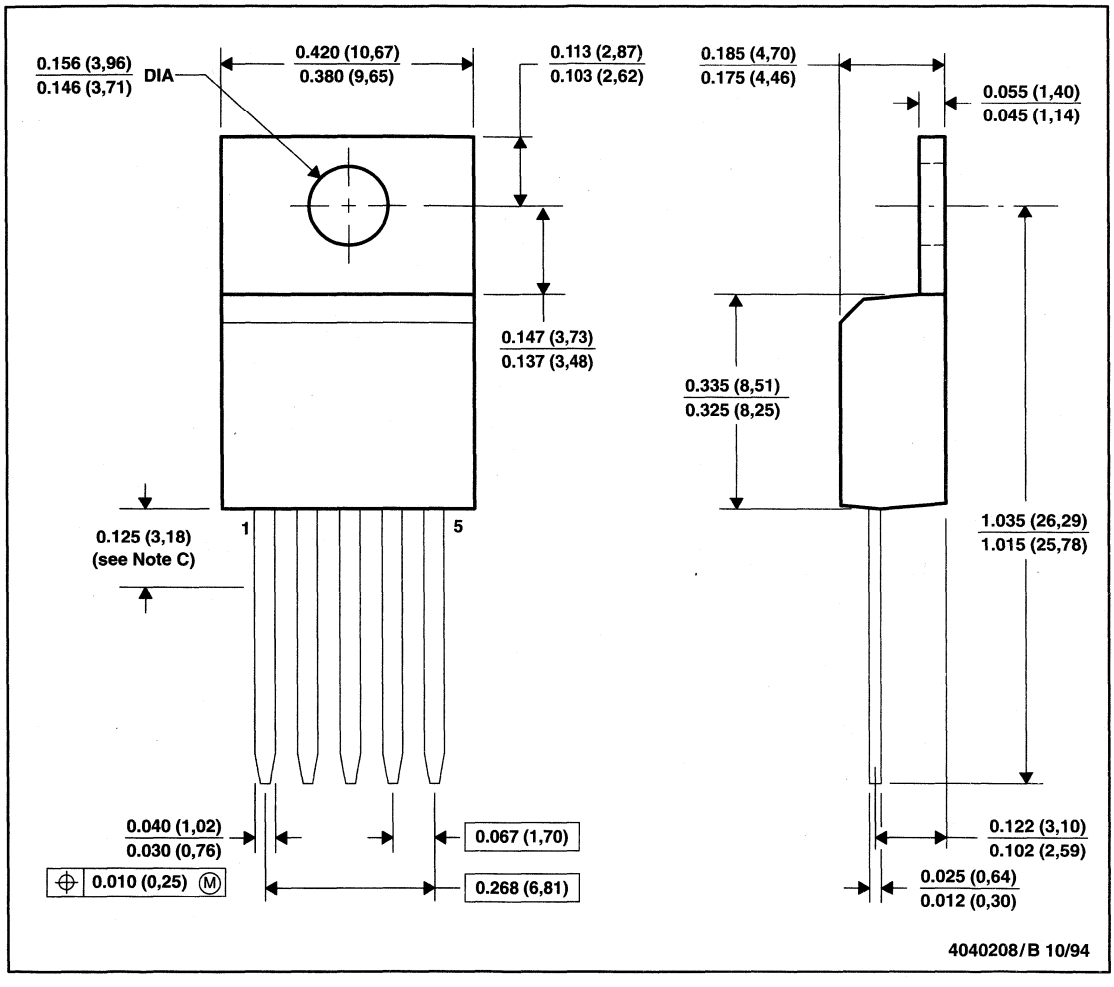
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

JANUARY 1996

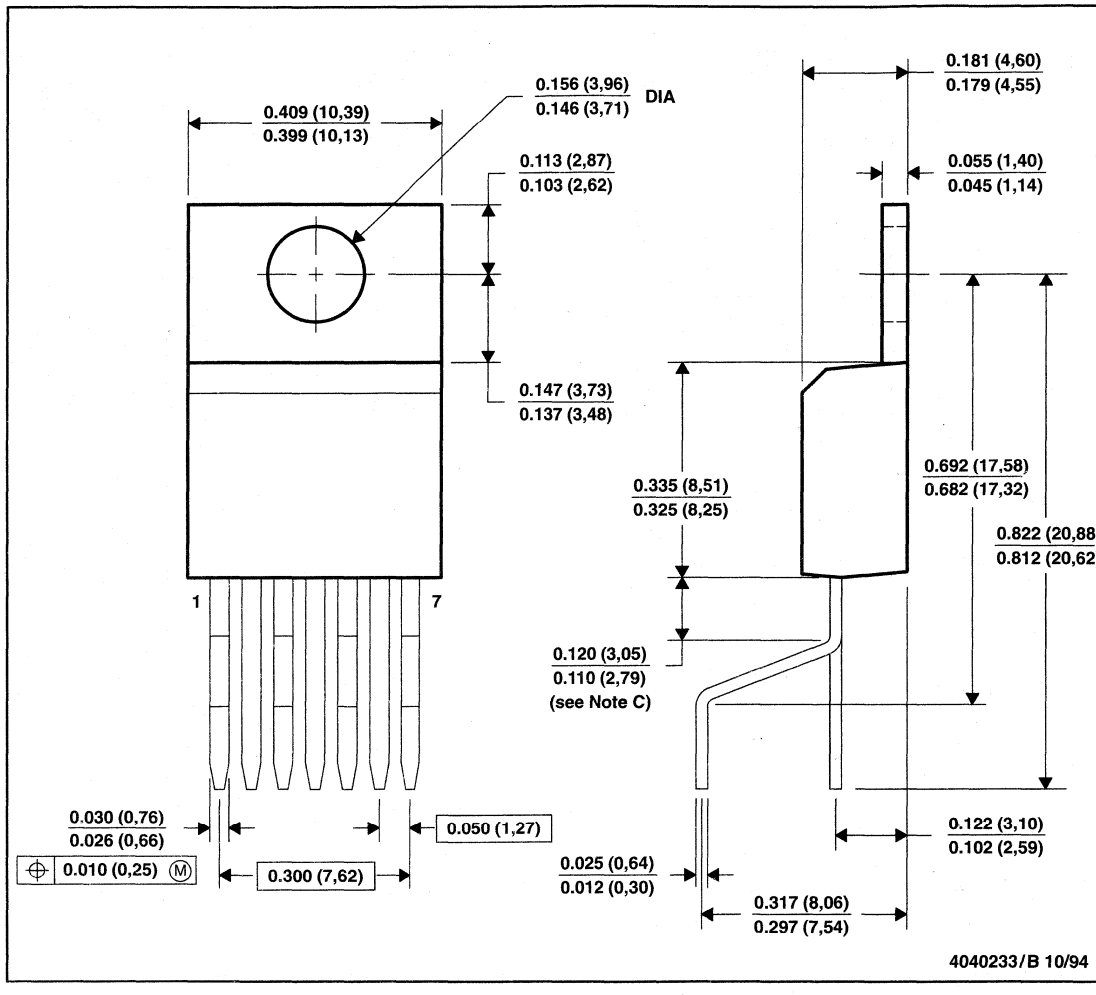
KC (R-PSFM-T5) **PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.

JANUARY 1996

KV (R-PZFM-T7) **PLASTIC FLANGE-MOUNT PACKAGE**



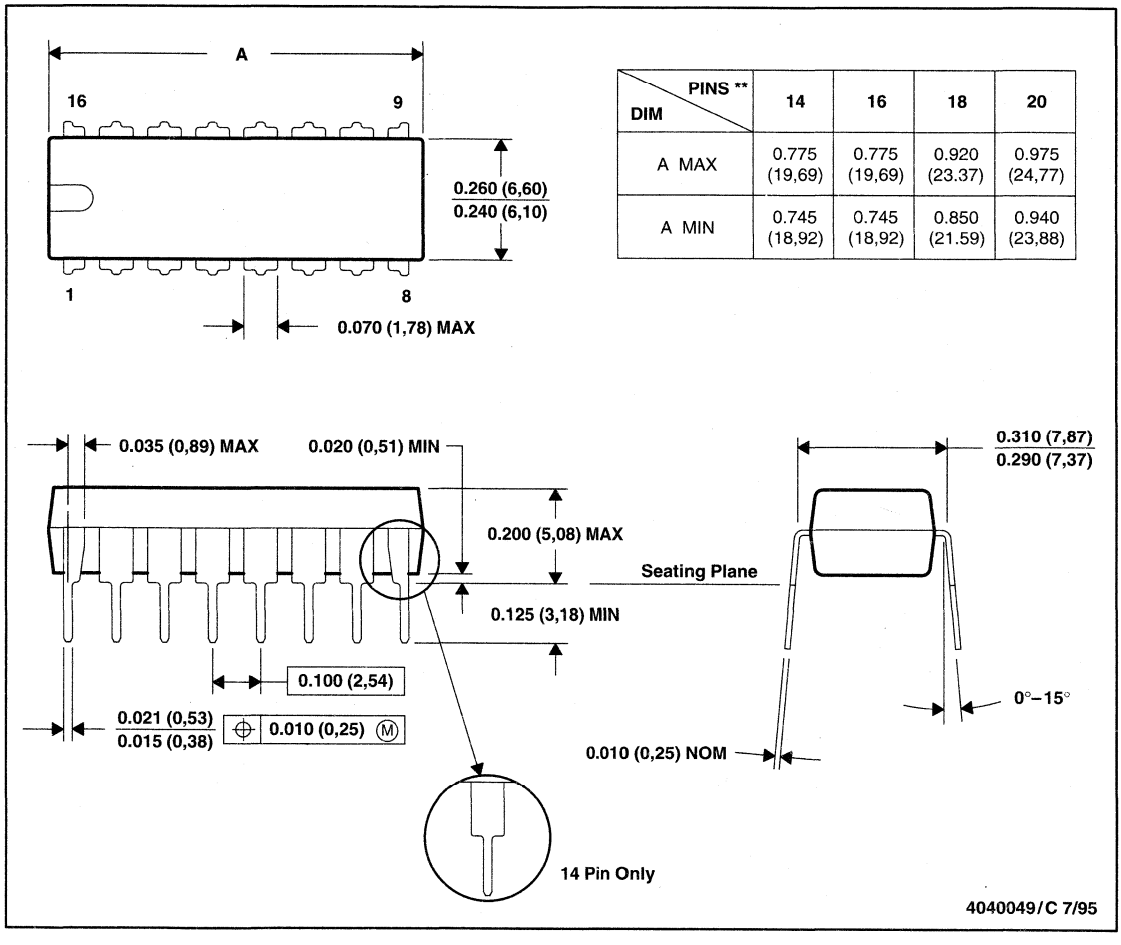
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.

JANUARY 1996

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

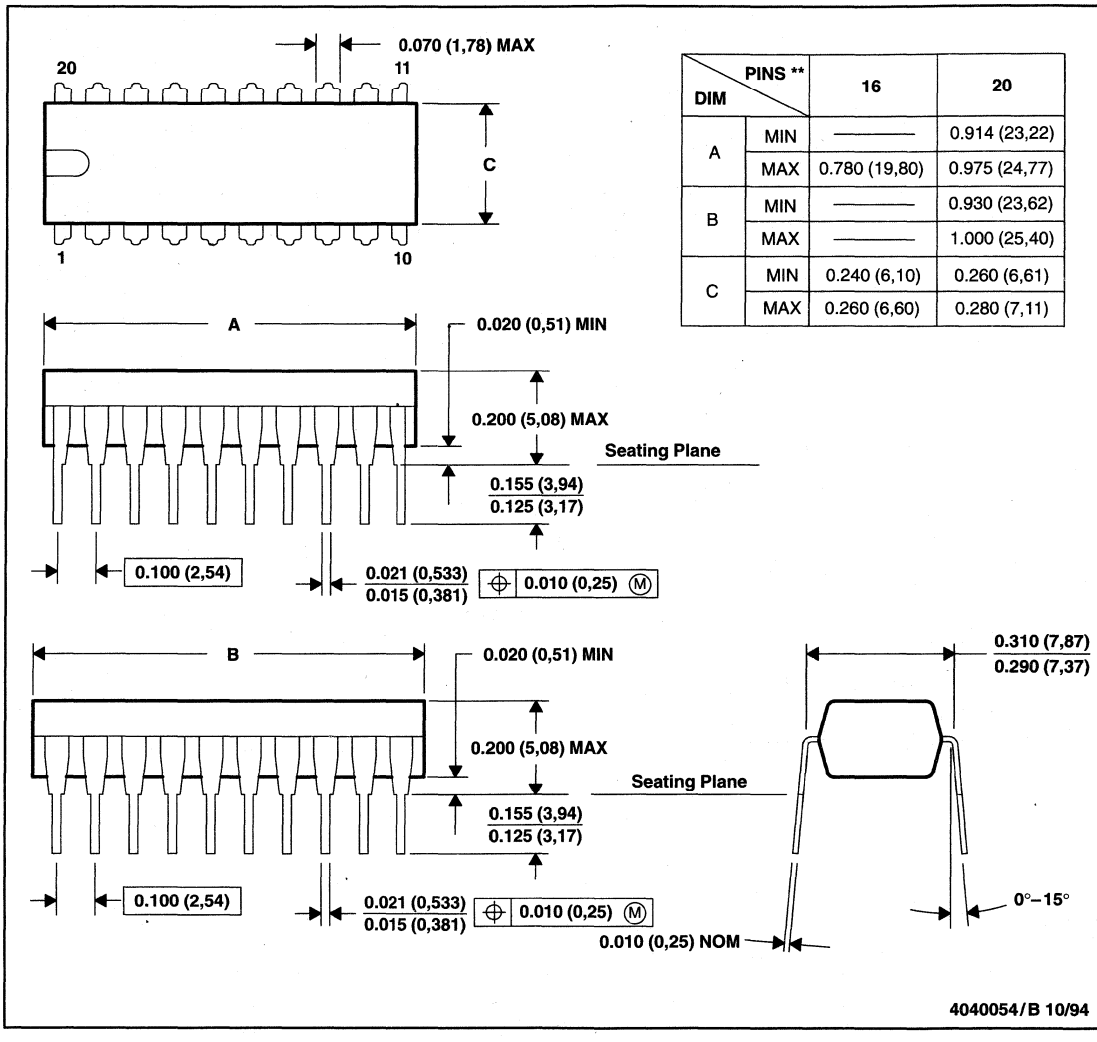
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

JANUARY 1996

NE (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN

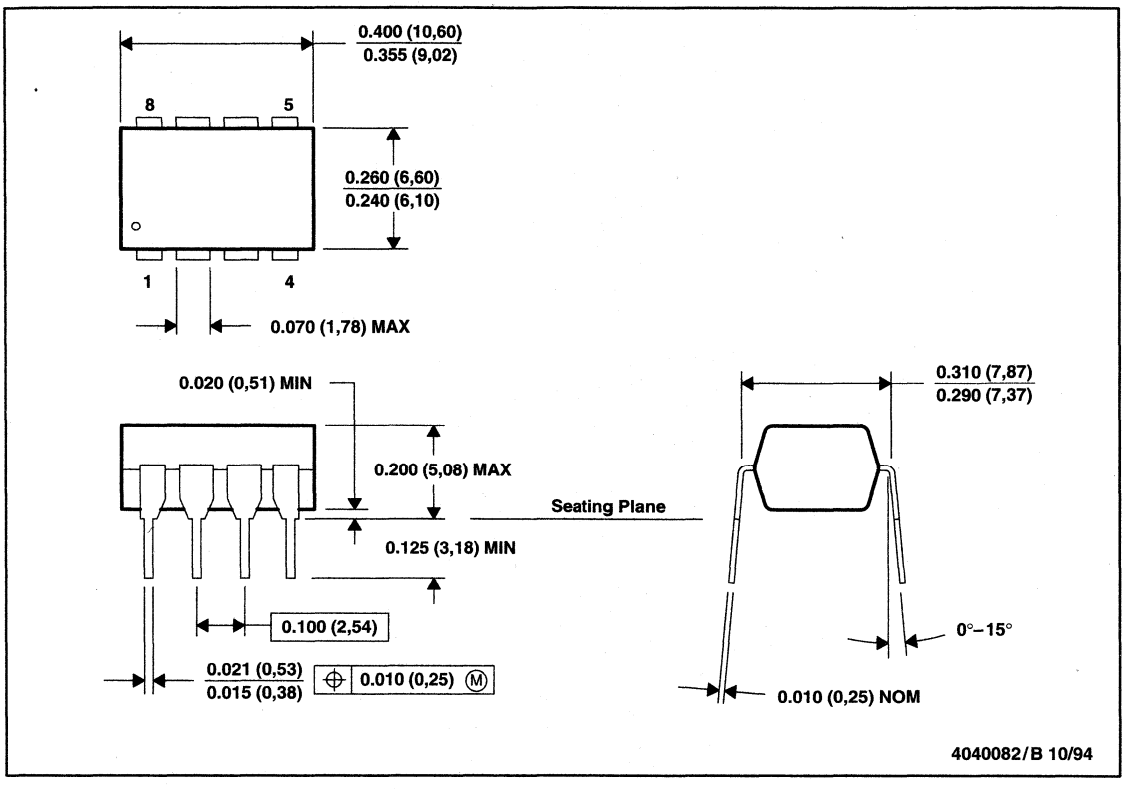


DIM \ PINS **		16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

JANUARY 1996

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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